5. **Design and Analysis of a Novel Mixed Mode FD SOI MOSFET**

A new structure of FD SOI MOSFET is proposed, which combines the advantages of inversion mode and accumulation mode devices: its transconductance performance is better than the inversion mode device, and its latch-up/breakdown voltage, threshold voltage rolling-off as well as leakage current better than the accumulation mode device. Moreover, the new device results in better hot carrier reliability.
5.1 Review of Previous Work

Compared to the partially depleted SOI MOSFET, fully depleted (FD) device provides higher transconductance, nearly ideal subthreshold slope and improved short channel effects [60]. However, the threshold voltage of the conventional inversion mode FD device tends to be too low for the practical applications or the channel doping has to be too high in order to obtain useful threshold voltage, which unfortunately gives rise to a degradation of the channel mobility and transconductance [61]. By using a p-type poly-silicon gate with lightly doped n-type silicon film, the threshold voltage is then determined by the gate work function other than the channel doping. Device working under this kind of operation is called accumulation mode FD SOI MOSEFET. 40%-improved mobility has been claimed compared to the bulk CMOS device [62]. However, accumulation mode device is not free from floating-body-related SOI problems (which are better known to occur in inversion mode devices), such as single transistor latch-up and early breakdown as it might at first be excepted [63]. In fact, according to our measurements as well as the PISICES simulation, the latch up voltage of the accumulation mode devices (especially for shorter channels) tends to be lower than its inversion counterpart. There is thus a tradeoff between performance (i.e. transconductance) and latch up (breakdown) voltage with inversion mode and accumulation mode devices. In this chapter, a new device is proposed and analyzed which mixes the above two modes, and suppress their shortcomings: lower driving current
in the inversion mode device and lower breakdown in accumulation mode device. In addition, the new device results in better hot carrier reliability compared to both modes.

5.2 The New Structure

Based upon our experience on the latch-up voltage measurements on inversion mode (INV) and accumulation mode (ACC) devices, latch-up voltage of INV is about 3-4 V higher than that of ACC. To analyze this, simulation was carried out to reveal their electric potential and field. The results does not show big difference of the electric field in these two modes and ACC does not necessarily have a smaller field than INV, depending on the bias condition (Figure 5.1). Yet the potential profiles do show an interesting difference of the two modes. Shown in Figure 5.2 (a) and (b), ACC has a deeper and steeper potential valley: the lowest point of potential is at the source/BOX corner as compared to the INV which has a more softened one with its lowest point sitting in the silicon film. Since the holes generated from the impact ionization will accumulate at the lowest electric potential, denser hole accumulation can be expected in ACC, which (following [63], the generated holes act as the p-type base of the parasitic bipolar transistor) implies the more bipolar action and easier latch up. It is thus interesting to see if this sharp valley can be “smoothed” by inserting a thin p-type layer along the back interface. A mixed accumulation/inversion mode (MIX) structure in the sense that the front channel works under accumulation mode whereas the back under inversion mode is thus proposed. By the aid of the SUPREM process simulator the new device can be virtually fabricated (shown in Figure 5.3(a)) with the following structural parameter: front gate oxide $t_{ox1}=20\text{nm}$, buried oxide $t_{ox2}=400\text{nm}$, silicon film
thickness $t_{Si}=100$nm, and gate length $L=0.8 \mu$m. The silicon film was initially n-doped at $1 \times 10^{16}$ cm$^{-3}$. The buried p-layer was implanted with boron with a dose of $7 \times 10^{11}$ cm$^{-2}$ at 50 keV after the gate oxide formation. After the p$^+$-poly gate formation, the drain was implanted with phosphorus in a dose of $3 \times 10^{13}$ cm$^{-2}$ at 20 keV (before the spacer formation), followed by an arsenic implantation with a dose of $5 \times 10^{15}$ cm$^{-2}$ at 50 keV (after spacer formation). The drive-in anneal was done at 900°C for 30 minutes. The achieved doping profile (Figure 5.3 (b)) shows an excellent separate doping profile of front and back channel.

5.3 Performance

PISECES device simulations have been carried out to get the performance of the new structure, as compared to its inversion (INV) and accumulation (ACC) counterparts. All three devices have the same physical parameters except the doping levels (donor concentration of $1 \times 10^{15}$ cm$^{-3}$ for accumulation mode and acceptor concentration of $1 \times 10^{17}$ cm$^{-3}$ for inversion mode are chosen so as to keep the same threshold voltage for the three modes). Figure 5.4 compares the transconductance ($G_m$) of the three structures. As expected, the $G_m$ of the mixed mode sits in between the other two modes, and for the case in hand the maximum transconductance of the new device (MIX) is about 30% higher than that of INV device. Figure 5.5 compares the latch up and breakdown behaviors of the three devices. The latch-up voltages (drain voltage taken at $I_D=1 \mu$A/\mu m) are 4, 5.5 and 7.2V and the breakdown voltages (drain voltage taken at $I_D=1 \mu$A/\mu m) 9, 10 and 10.7V for the ACC, MIX and INV device respectively. Also can be seen from Figure 5.5 that there is over an
order of magnitude improvement on leakage current in MIX as compared to that in ACC. The electric fields of the three structures (Figure 5.1), are also in agreement with the above results. The poor rolling-off character of $V_T$ in ACC was also improved in MIX (Figure 5.6).

Finally the three structures were compared in terms of hot carrier reliability by calculating the hot electron and hot hole injection currents into front and back oxide. The injection currents were calculated from the resulting electric field and impact ionized carrier generation rate with the lucky-electron-model methodology described in Chapter 2. It is seen from Figure 5.7 that $I_{e1}$, $I_{h1}$, $I_{h2}$ are highest for INV and $I_{e2}$ for ACC, in fair agreement with experiments [64], [65], and that the overall injection currents of MIX are the lowest.

### 5.4 Future Work

According to our simulation, the new structure seems to work fine. Yet it is more persuading if it can be made in the real Fab and tested, especially its hot carrier resistance characteristics. We are now discussing with our colleagues of Honeywell to arrange for the fabrication of prototypes.
Figure 5.8: Comparison of maximum lateral electric fields. $V_D=3V$. 
Figure 5.9 Potential profiles of (a) the inversion mode and (b) accumulation mode FD SOI MOSFET
Figure 5.10 (a). New device structure obtained by SUPREM simulation (b). Doping profile in the channel region.
Figure 5.11 Comparison of transconductance
Figure 5.12 $I_D$-$V_D$ characteristics of the three devices. Both gates are grounded during the simulation.
Figure 5.13 Comparison of threshold voltage dependence on channel length.
Figure 5.14 Comparison of hot electron and hole injection current into the front and back oxide of the three modes. Devices biased at $V_{D}=3$ V and back gate grounded. (Subscript e and h symbol electron and hole injection, 1 and 2 the front and back oxide respectively. For example, $I_{e1}$ indicates electron injection into the front oxide.)