ERC Retreat Stanford: New Chemistries & Tools for $scCO_2$ Processing of Thin Films

Overview of Dual Damascene Cu/Low-k Interconnect

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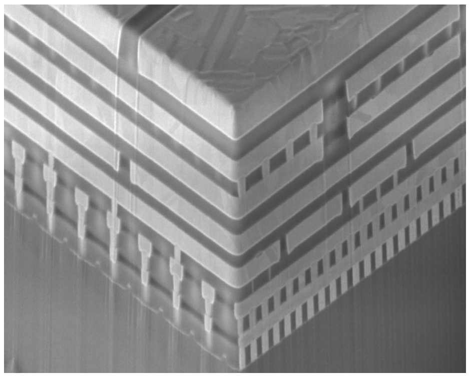
Presentation Outline

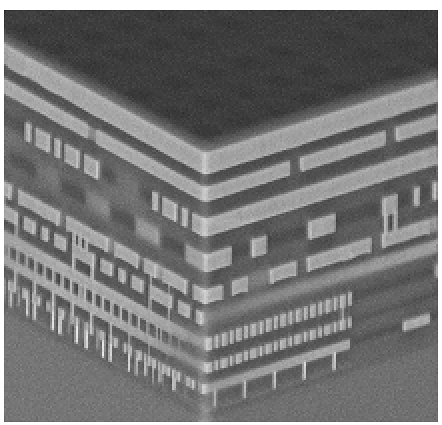
- **Interconnect**
  - Why ultra low-k?
  - Properties and challenges of porous low-k materials
  - Dual damascene structure
- **Dual damascene process flow**
- **Low-k integration issues & potential solutions**
- **Conclusion**

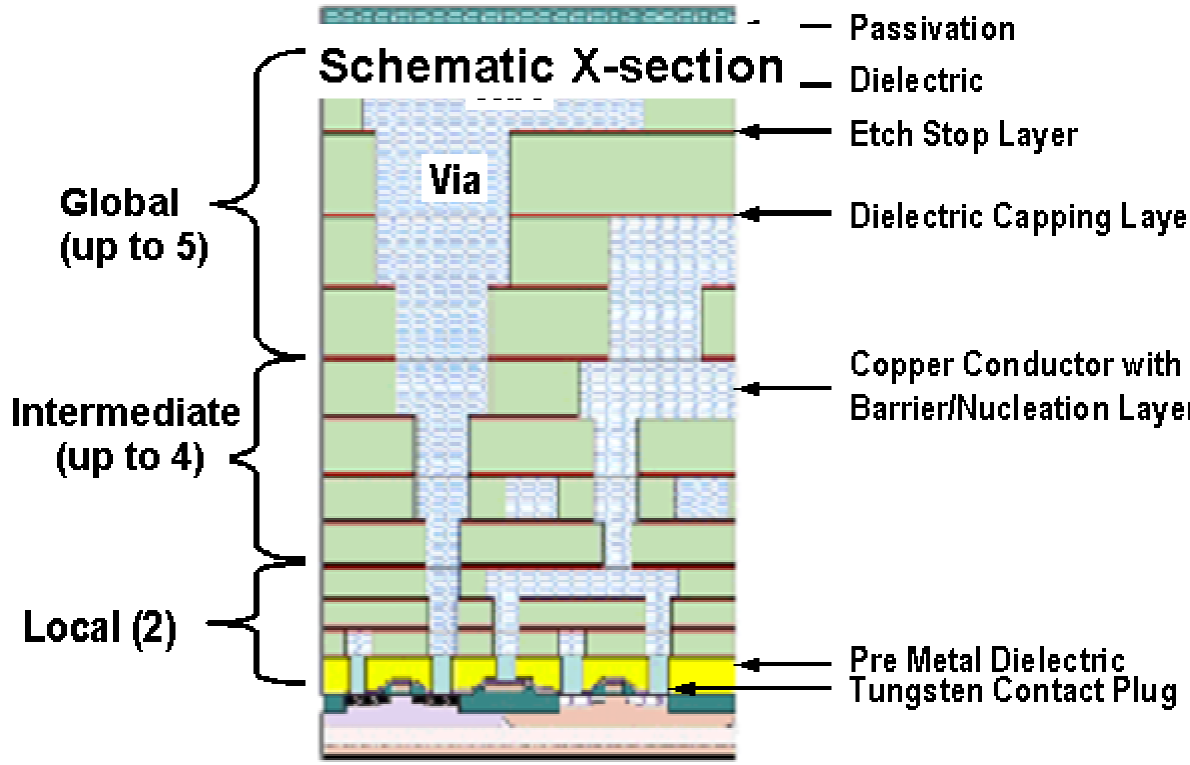
Interconnect Structure

130nm – 6LM



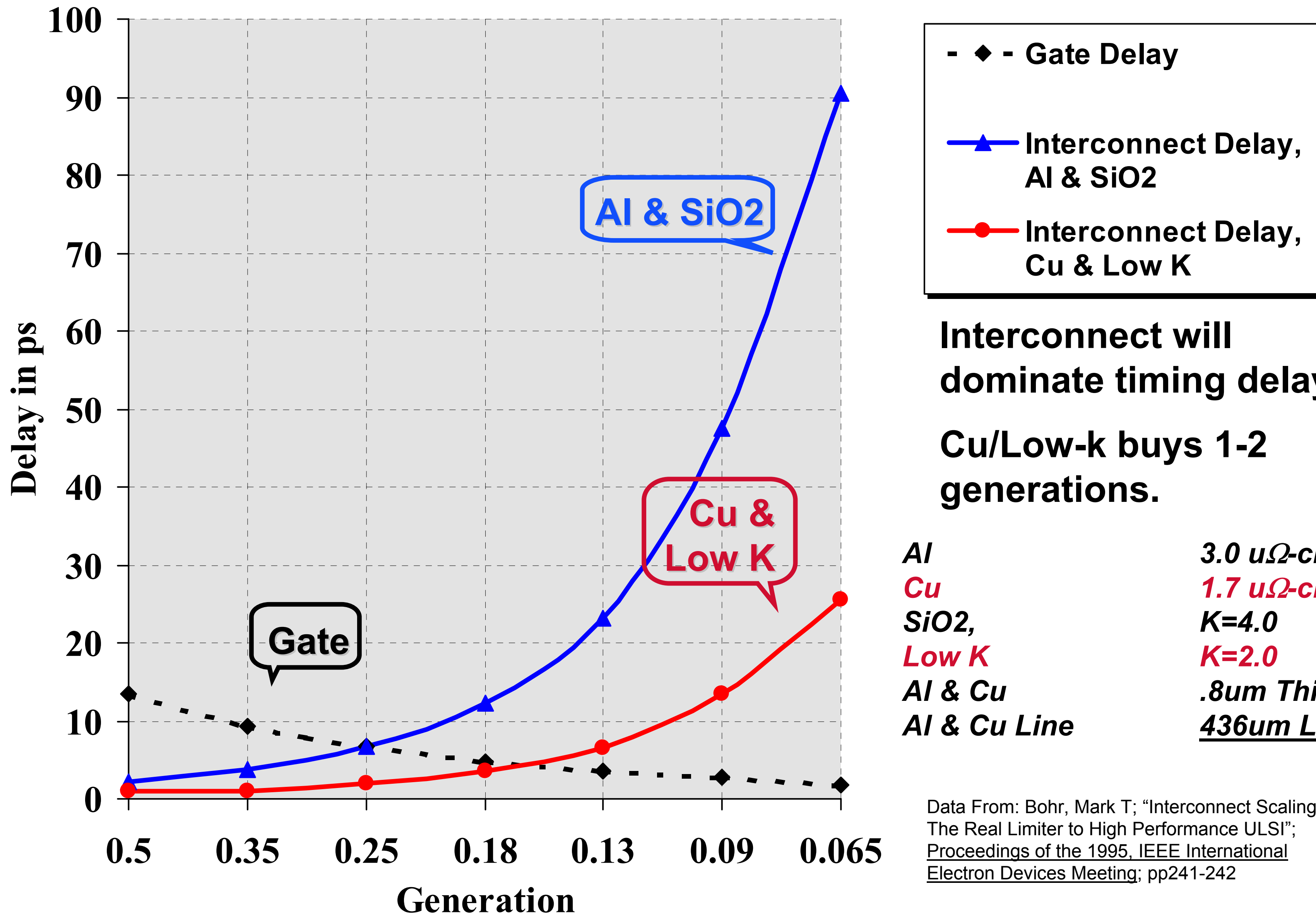
90nm – 9LM





SEM Cross-sections Courtesy of AMD

Why Cu/Low-k?....R*C Product



Interconnect will dominate timing delay.

Cu/Low-k buys 1-2 generations.

Al	*3.0 uΩ-cm*
Cu	*1.7 uΩ-cm*
SiO2,	*K=4.0*
Low K	*K=2.0*
Al & Cu	*.8um Thick*
Al & Cu Line	*436um Long*

Data From: Bohr, Mark T; "Interconnect Scaling - The Real Limiter to High Performance ULSI"; Proceedings of the 1995, IEEE International Electron Devices Meeting; pp241-242

THE PROBLEM IS RC - HOW FAR CAN YOU GO?

A Theoretical Ideal

	Aluminum (alloy) >>>	Copper,		R reduction of
Resistivity	3.2	1.8		1.8 x

	SiO2 >>>>>>>>>	Low-K>>>>>>	Air,	C reduction of
Dielectric Constant	4.2	2.1	1.0	2.0x - Low-K 4.2 x - Air

RC Reduction of

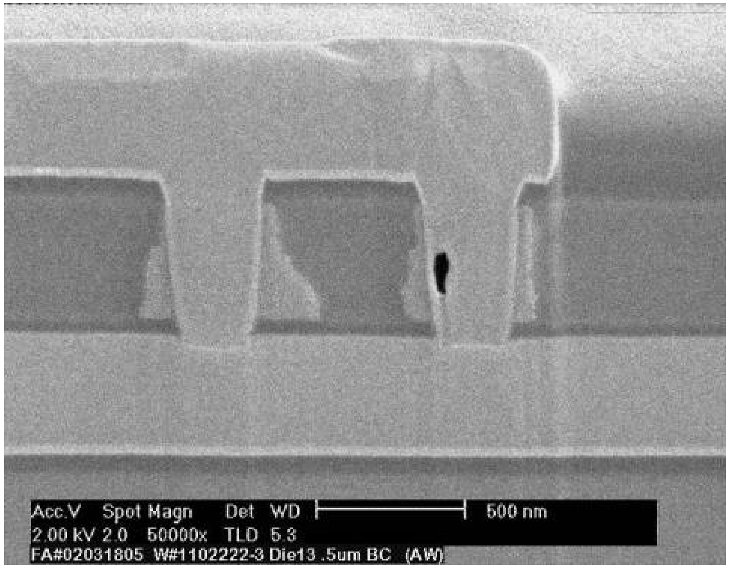
7.5 – Cu/Air

3.5 – Cu/Low-k

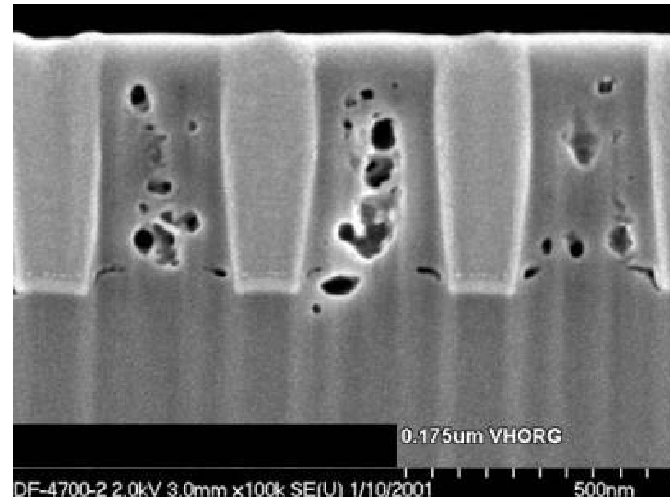
Properties of Porous Ultra Low-k Materials vs. Oxide

Property	Low-k	Oxide
Density (g/cm^3)	1.03	2.2
Dielectric Cons.	~1.9-2.5	4.1
Modulus (GPa)	~3-9	55-70
Hardness (GPa)	~0.3-0.8	3.5
CTE (ppm/K)	~10-17	0.6
Porosity (est.)	~35-65%	NA
Avg. Pore Size	<2.0-10nm	NA
Thermal Conductivity (W/m K)	0.26	1.4

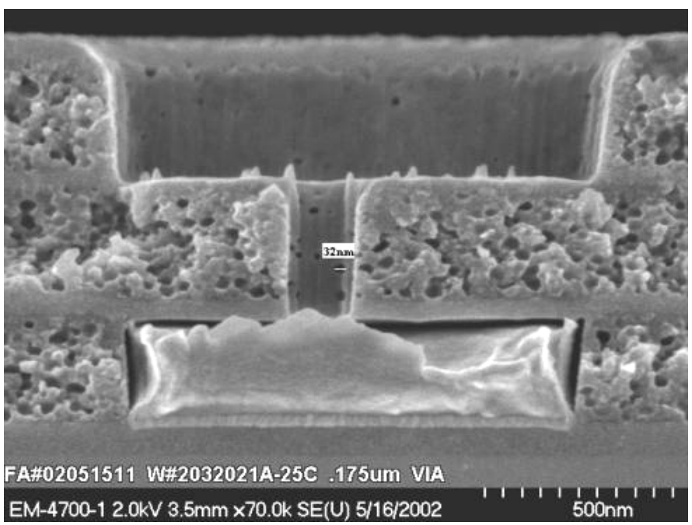
Low-k – Integration Challenges



Low k voiding

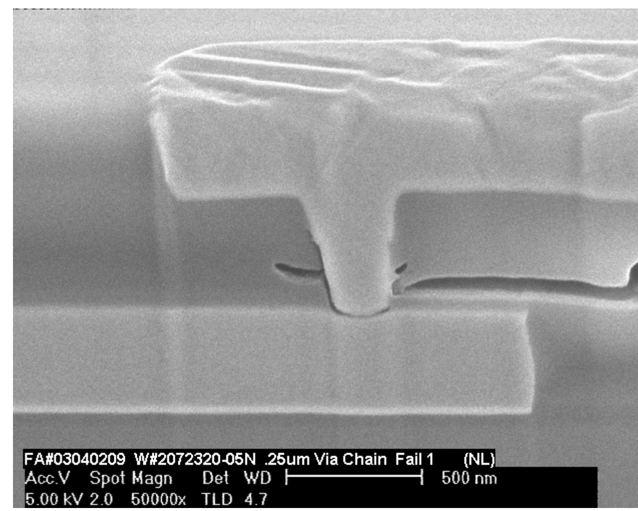


Cu diffusion / barrier integrity

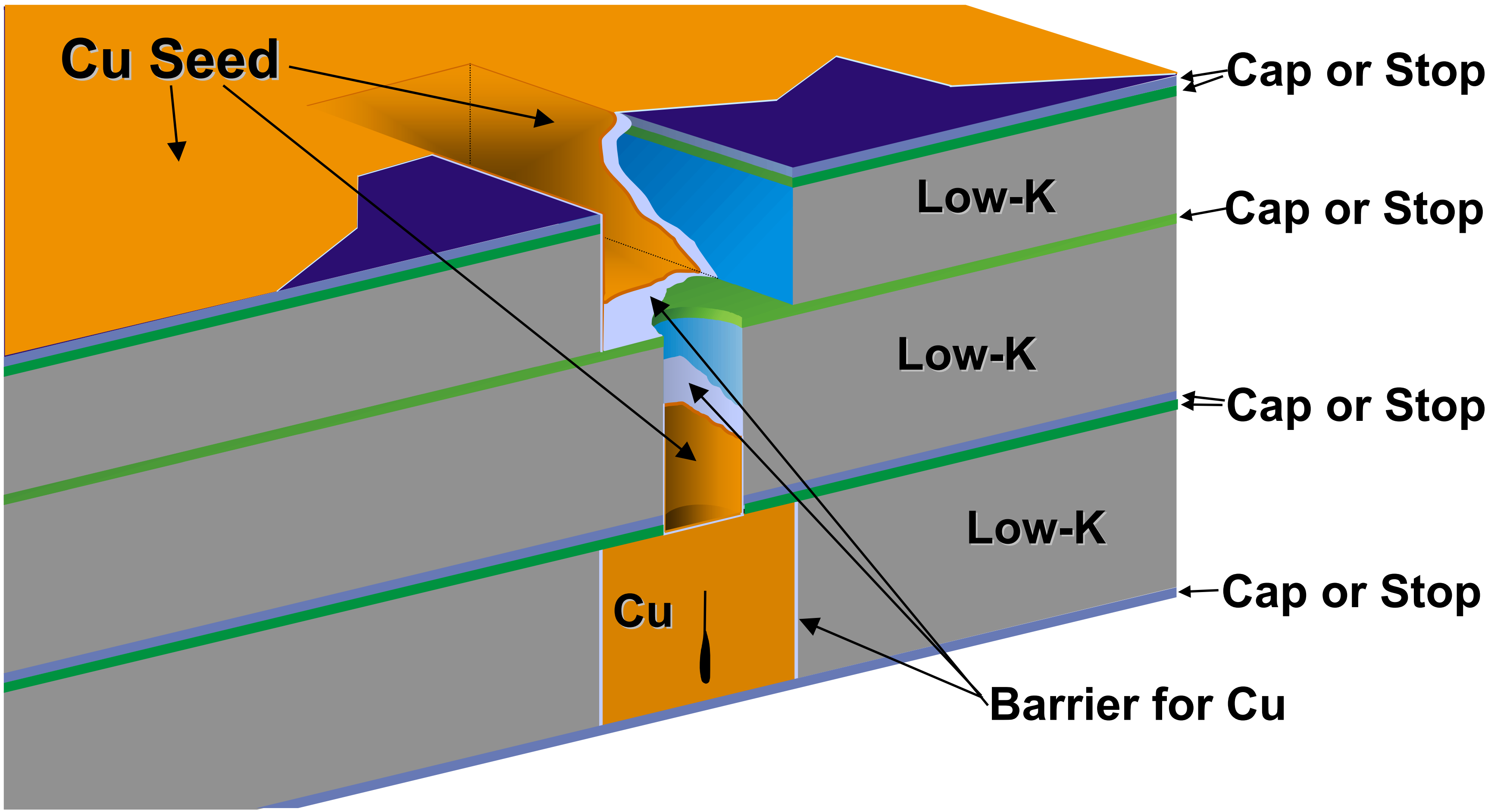


Large pore structure

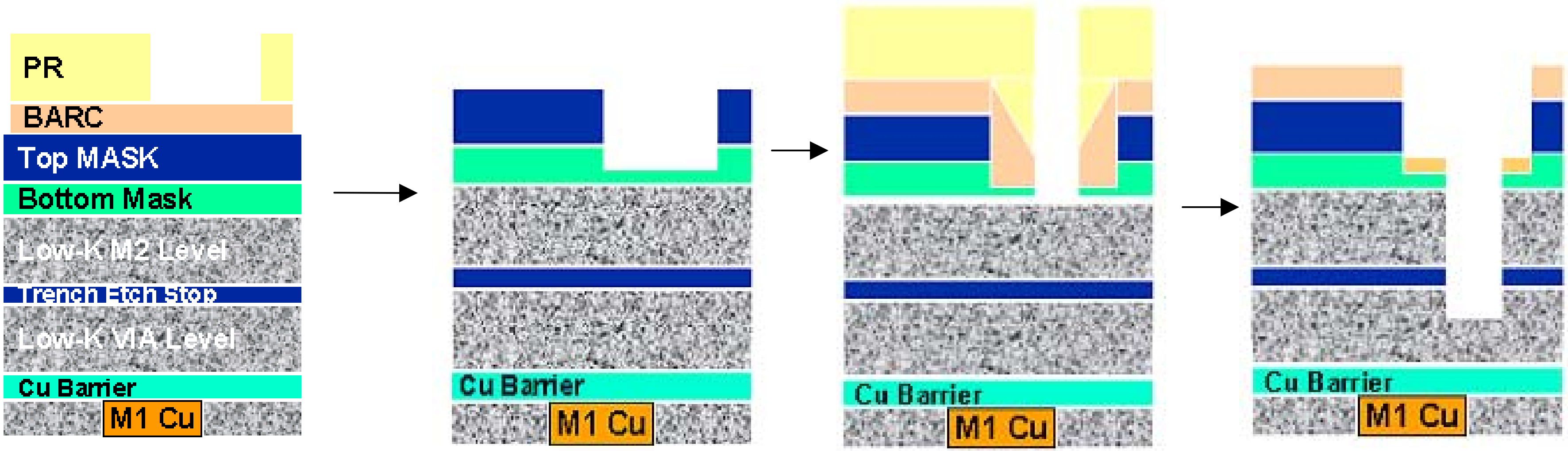
Dielectric cracking



A DUAL DAMASCENE 'UNIT' STRUCTURE



Dual Damascene Dual Top Hard Mask Process



M2 Hard Mask Pattern

1. Low-k – CVD or SOD
2. Etch stop / barrier – CVD
3. Hard Mask – SiO_2 & SiC
4. Conventional Litho

Post HM Open Etch & Ash

1. Define Trench w/ etch process
2. Ash resist
3. No low-k exp to ash process
4. Allows litho rework at Via

VIA Pattern & Initial Bottom Mask Open

1. Litho Via on hard mask
2. Etch through hard mask

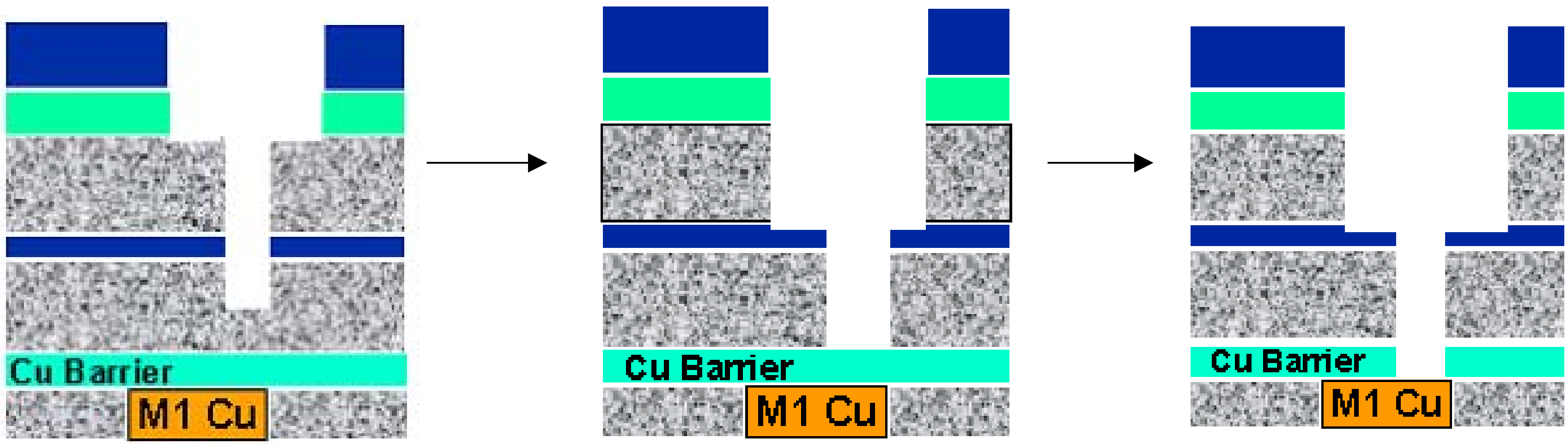
Low –k VIA Etch

1. Etch low-k @ M2
2. Etch Trench Stop
2. Leaves M2 mask
3. Some low-k exposure to Ash

Pot. Low-k Damage

1. Via Structure

Dual Damascene Dual Top Hard Mask Process



Ash & Bottom Hard Mask Open

1. in-situ ash (in etch tool)
2. Open (etch) bottom HM

Pot. Low-k Damage
1. Via Structure

VIA & M2 Simultaneous Etch

1. Drive trench down
2. Complete Via
3. Need to leave etch stop intact

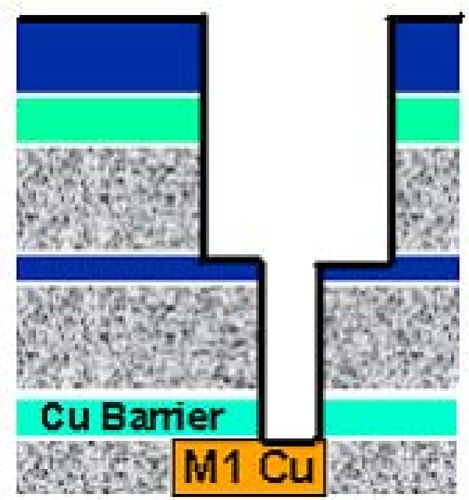
Pot. Low-k Damage
1. Via Structure
2. Trench
3. Etch stop integrity

Cu Barrier Open and Via Cleans

1. Cu open
2. Clean to remove etch & ash residue

Pot. Low-k Damage
1. Moisture uptake
2. Etch residue uptake
3. Cu oxidation
4. All exposed low-k

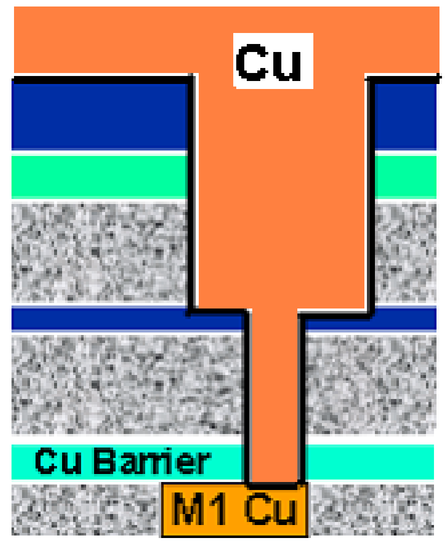
Dual Damascene Dual Top Hard Mask Process



Barrier Seed (pore sealing)

1. Ar sputter etch
2. ALD / CVD material
   Ta, TaN, others
3. Seal damaged pores

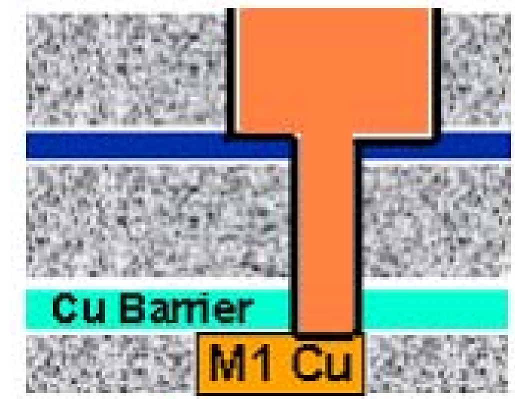
Pot. Low-k Damage
1. Discontinuity
2. Sputter Etch



Cu Plate

1. Fills Trench &
   Via simultaneously

Pot. Issues
1. Fill uniformity
2. Key Holes



CMP

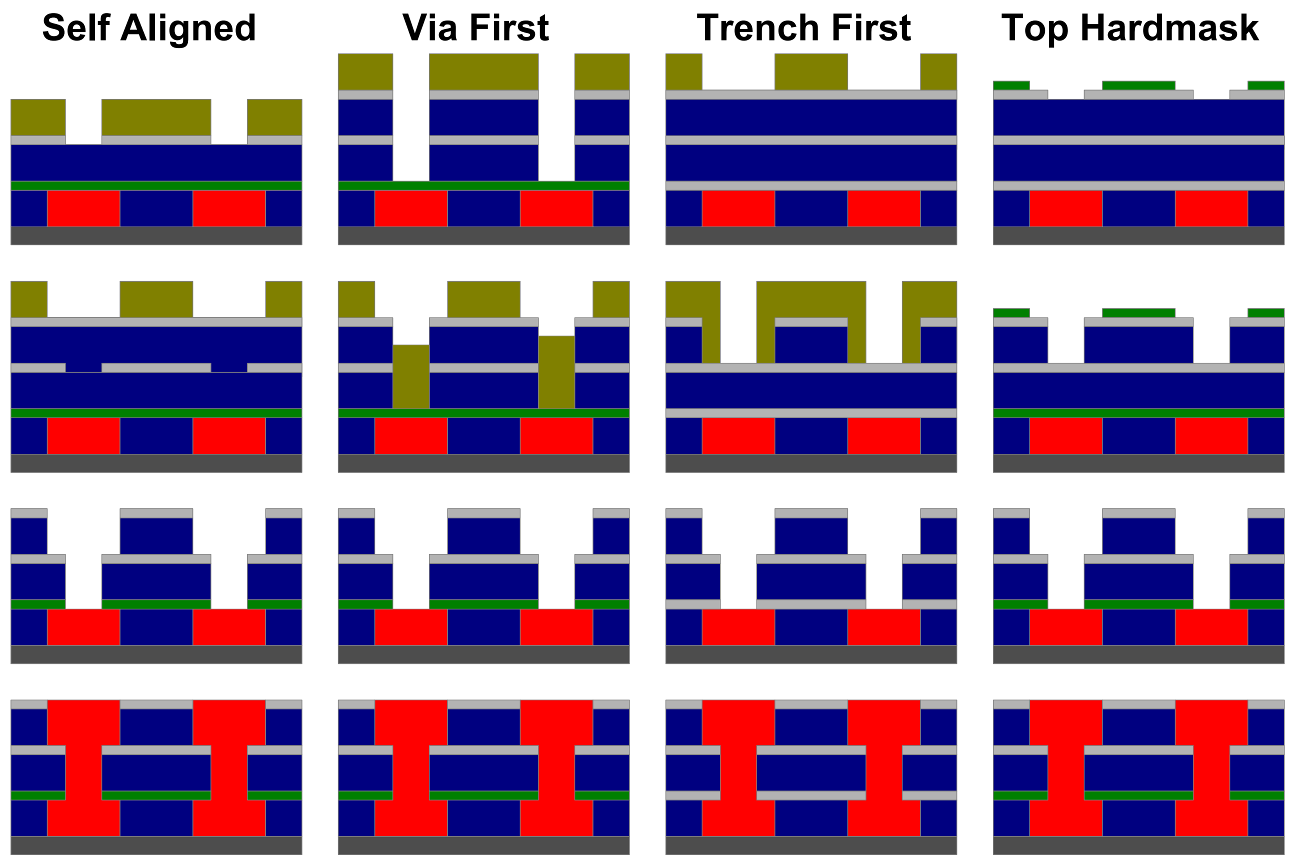
1. Removes Cu & Hard Mask
2. Post CMP cleans

Pot. Issues
1. Uniformity
2. Pressure – damage low-k
3. Cu corrosion

Integration Schemes for Dual Damascene

Each scheme has its own integration issues and challenges.

There are also many variations on each scheme.



Issues

Self Aligned	Via First	Trench First	Top Hardmask
•Alignment •Litho rework	•BARC "fencing" •PR poison •Litho rework	•Litho DOF •BARC fill •PR poison •Litho rework	•High overall k_{eff} •Etch Resist selectivity •Litho Overlay

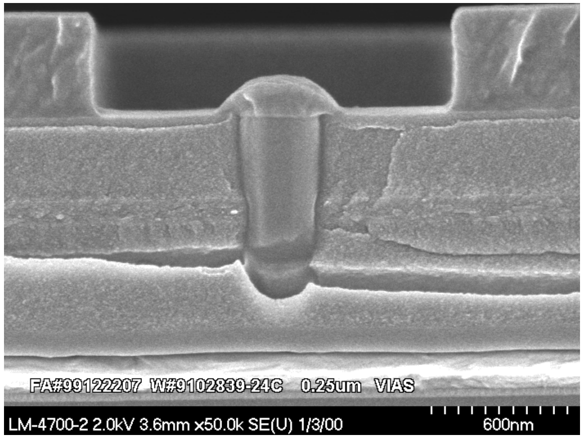
Simple So Far……..Integration Issues

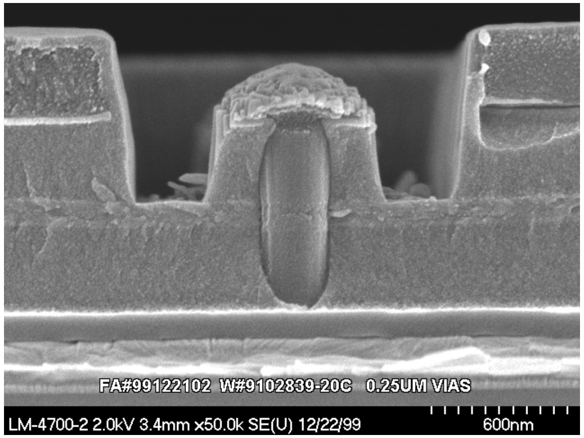
- **Issues**
  - Etch by-products are deposited on exposed low-k films
  - Aqueous processes can drive in contaminates and modify low-k structure
  - Etch, ash, and cleans difficult to control – pores, soft material – CD / uniformity, process selectivity, etc.
  - CMP processes put (shearing) forces on soft and weak low-k structures / materials
  - Discontinuous barriers can allow Cu diffusion / failure
  - Specific integration issues to each low-k

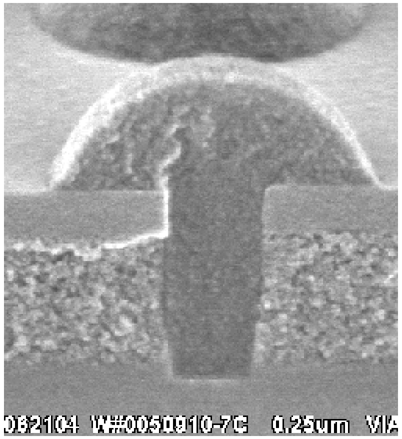
Resist Poisoning

- **Resist poisoning occurs when nitrogen containing chemistries or films can outgas (NH_3) into resist**
  - Use of N_2/H_2 ash processes
  - Exposure of SiCN barrier during Via First Etch Scheme
  - Use of Nitrogen containing films in other areas of stack

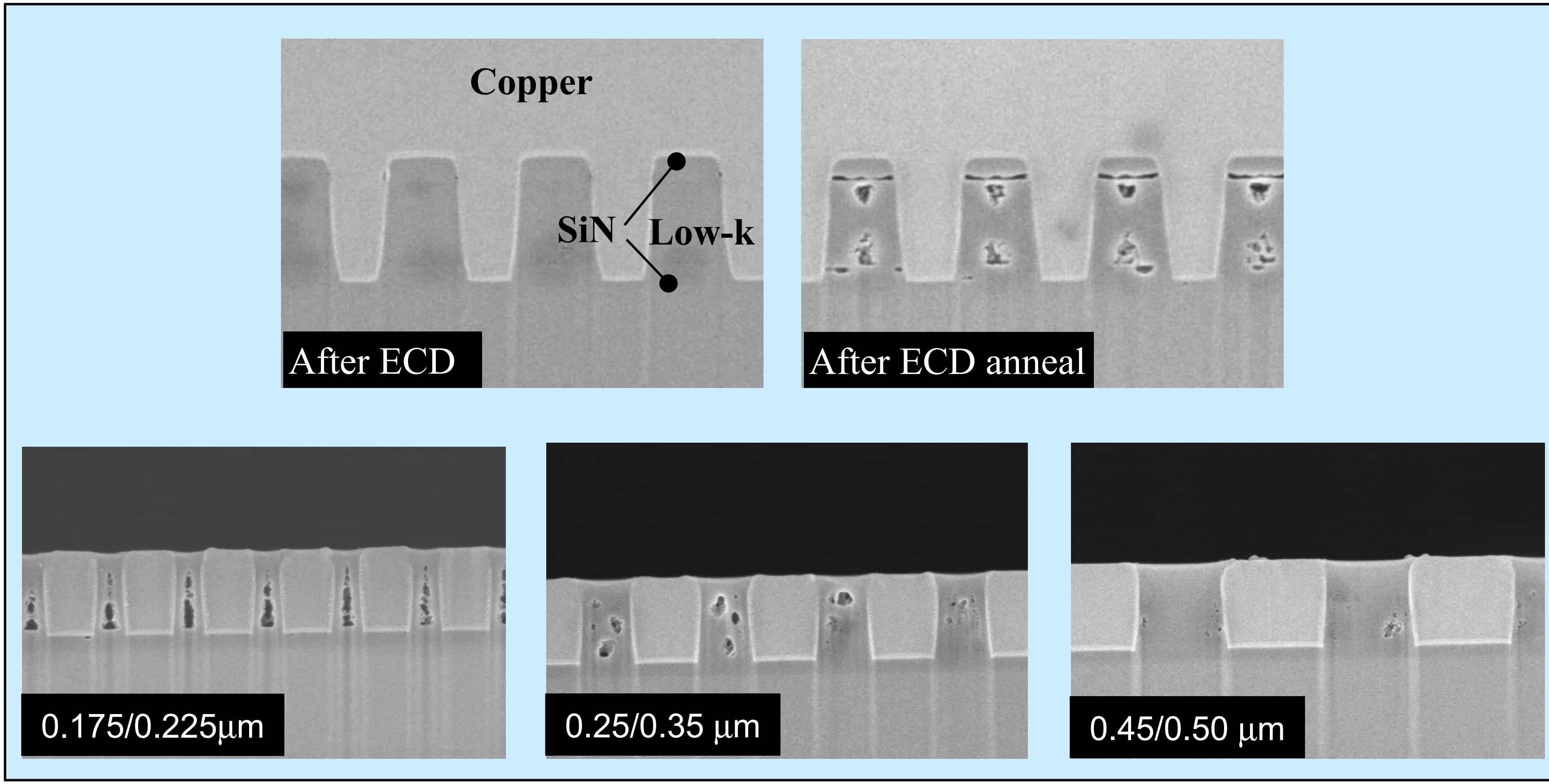
Resist-poisoning *(caused by trapped amines/ NH_3)*





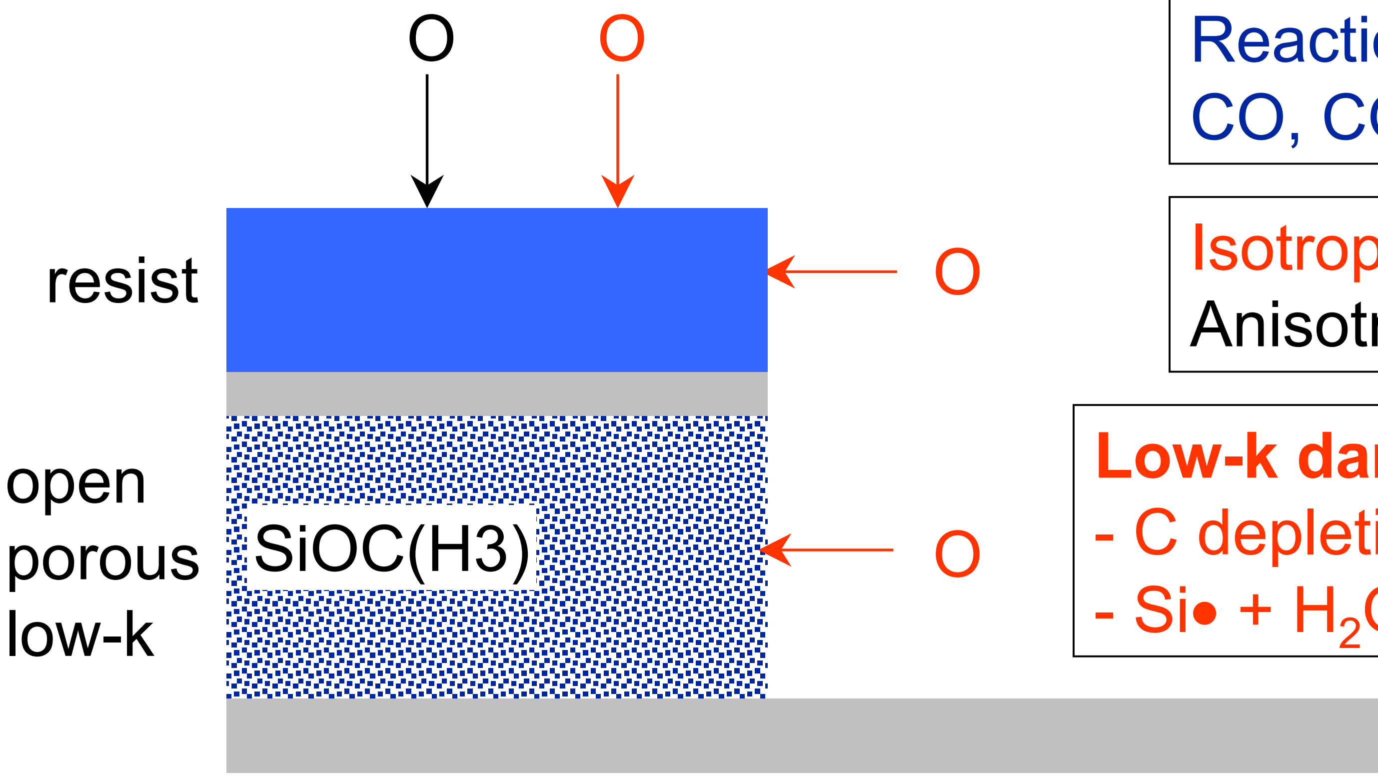


Low-k Voiding



- **Low-k voids occurs during post Cu plating anneal**
- **Wider low-k spacings exhibit less voiding**

Traditional microwave oxygen ashes



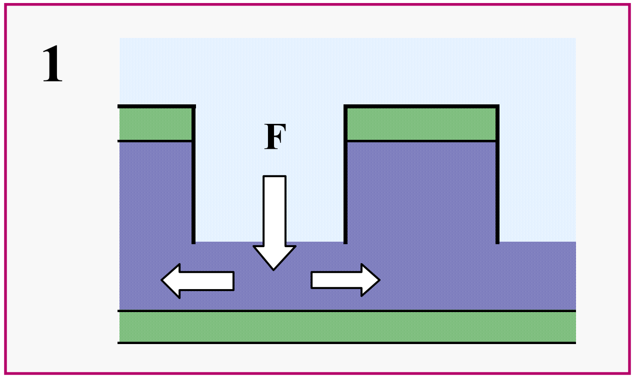
Reaction products:
CO, CO_2, H_2O ↑

Isotropic
Anisotropic

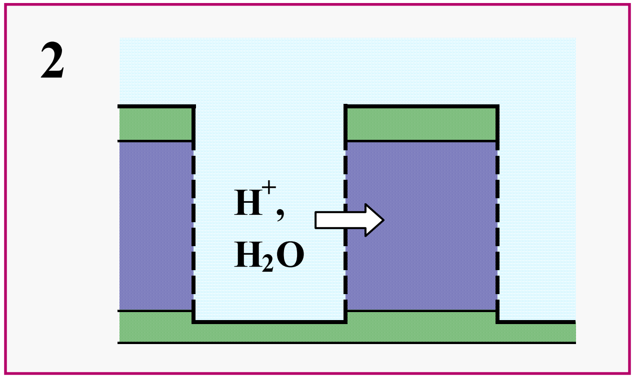
Low-k damage:
- C depletion
- Si• + $H_2O \rightarrow$ SiOH

- **Isotropic ash processes remove also C from porous low-k film**
- **Makes low-k hydrophilic**

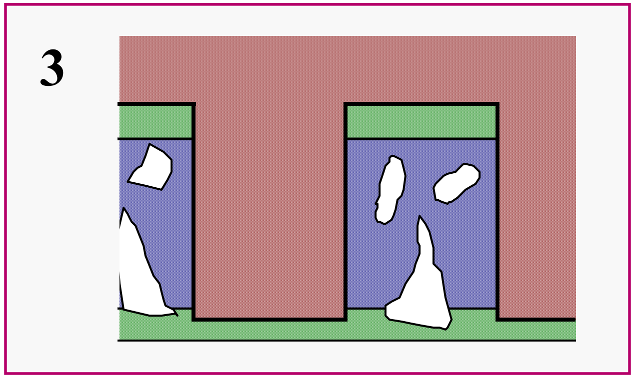
Assumed low-k voiding mechanism



Fluorine captured in pores of low-k
- Primary source is etch process
- Ash releases fluorine from resist/ polymers
- Incomplete removal in post ash wet clean



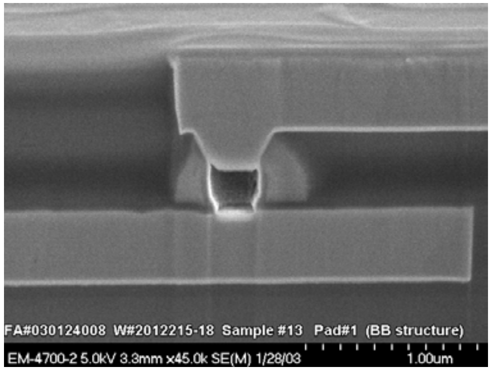
Low-k film becomes hydrophilic
- Ash & etch chemistries can deplete Carbon
- Promotes moisture uptake at sidewalls - cleans
- Discontinuity in barrier/ seed layer – Cu plate
- HF formation



HF reaction with low-k, SiN_x
- Anneal starts HF reaction with low-k
- ‘Sub-micron pressure cooker’
- Mechanically induced stress from copper lines
- SiCN not attacked

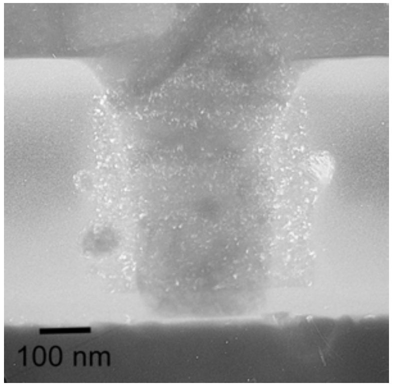
Cu Diffusion / Depletion

- **Cu diffuses out of structures**
  - Barrier discontinuities
  - Moisture / diffusion gradients
  - Electro-thermal stress

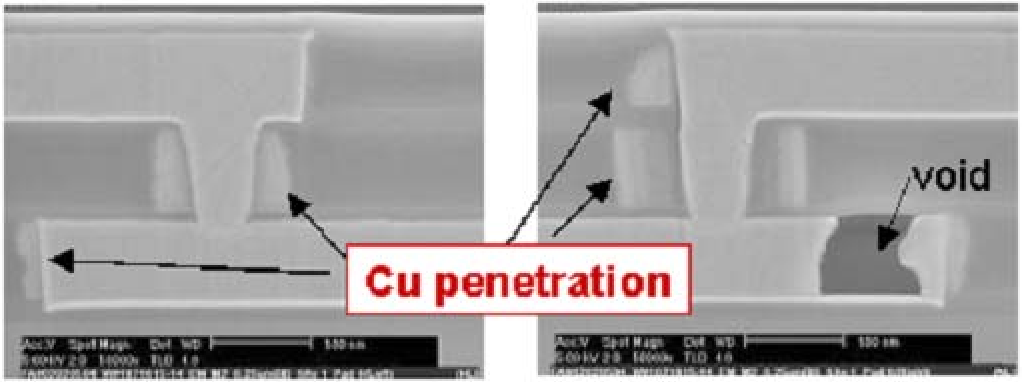


Open Via due to Cu depletion

- **Structure fails from Cu depletion**

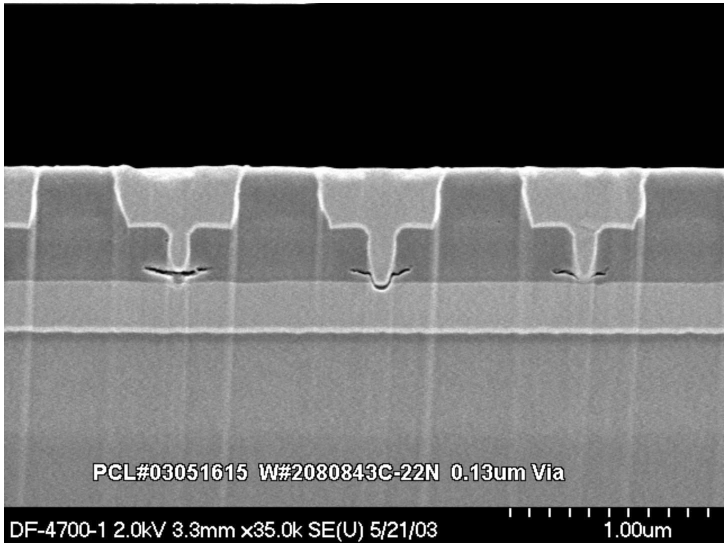


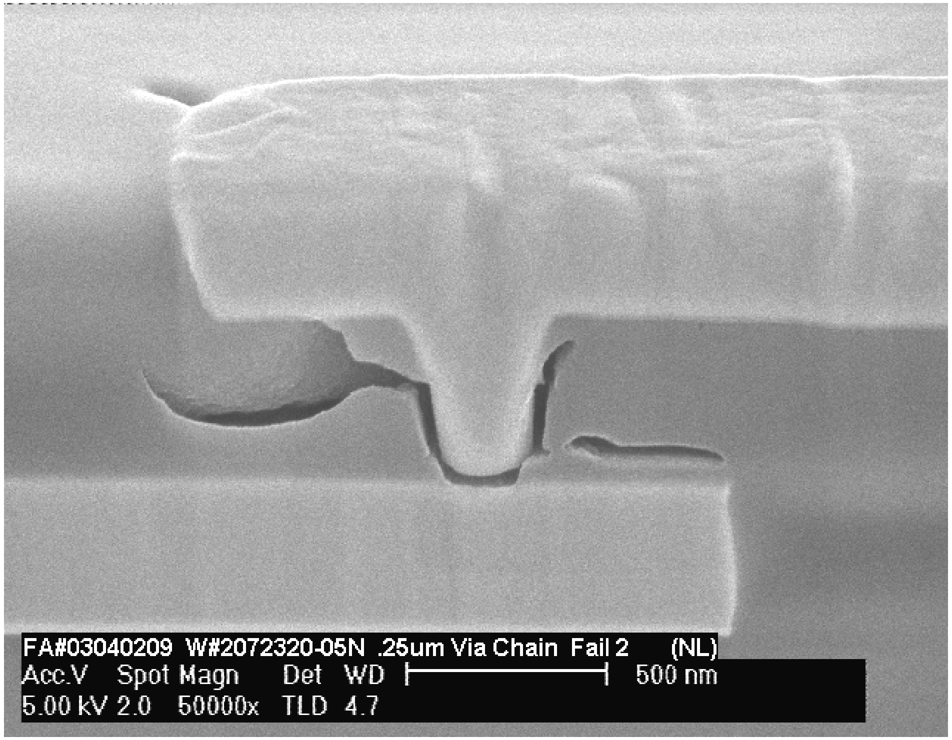
TEM of Cu diffusion into low-k



Dielectric Cracking

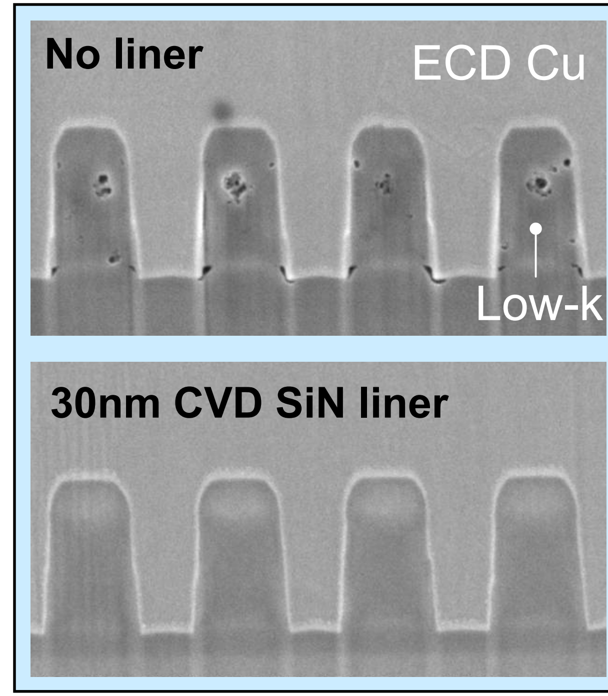
- **CMP – "final straw"**
  - Structural / compound changes to low-k during etch, ash, cleans
  - Stresses from CMP "wiggle" structures



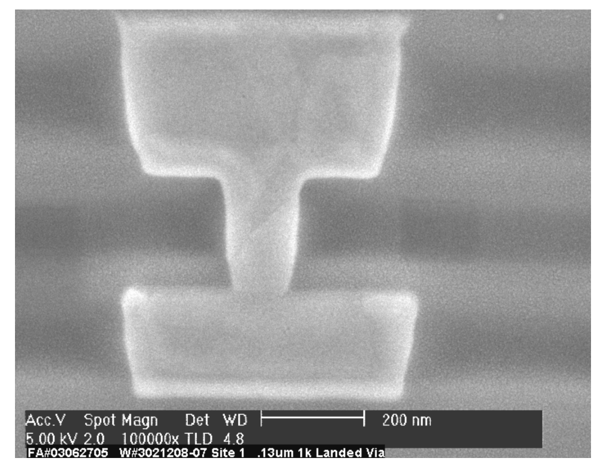


Solutions

- **Low-k voiding**
  - – Implement a “pore sealing” process
    - prevent contaminants & moisture from entering low-k
  - – Implement a cleans process w/ restoration
    - remove contaminants & restore C(H3)
  - – Minimize aqueous treatments
  - – Novel plasma, strip and cleans



- **Dielectric Cracking**
  - – Modulated by low-k damage & CMP force
  - – Restore low-k properties (cleans)



- **Cu Diffusion / Depletion**
  - – Advanced barriers
  - – Novel liners

Conclusions

- **Low-k are difficult materials to integrate**
  - Multiple integration approaches, all have pros & cons
  - Specific issues to different low-k
    - Density & porosity fluctuations by depth
    - Organic materials – behave like photo-resist
  - Require advance stripping, cleaning, metalization & CMP
- **Need to minimize or restore low-k damage**
  - Neutral beam plasmas
  - Ion beams for stripping and pore sealing
  - Restorative cleans processes – scCO_2 w/ HMDS
  - Advanced barriers and metalization processes
  - Pore sealers – sacrificial or permanent