Overview of Dual Damascene Cu/Low-k Interconnect
Presentation Outline

• Interconnect
  – Why ultra low-k?
  – Properties and challenges of porous low-k materials
  – Dual damascene structure

• Dual damascene process flow

• Low-k integration issues & potential solutions

• Conclusion
Interconnect Structure

130nm – 6LM

90nm – 9LM

SEM Cross-sections Courtesy of AMD
Why Cu/Low-k?....R*C Product

Interconnect will dominate timing delay.
Cu/Low-k buys 1-2 generations.

THE PROBLEM IS RC - HOW FAR CAN YOU GO?

A Theoretical Ideal

<table>
<thead>
<tr>
<th>Material</th>
<th>R Reduction of</th>
<th>C Reduction of</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum (alloy) &gt;&gt;&gt;&gt; Copper, Resistivity</td>
<td>3.2 1.8 1.8 x</td>
<td>1.8 x Low-K</td>
</tr>
<tr>
<td>SiO2 &gt;&gt;&gt;&gt;&gt;&gt;&gt;&gt;Low-K&gt;&gt;&gt;&gt;&gt; Air, Dielectric Constant</td>
<td>4.2 2.1 1.0 2.0x - Low-K</td>
<td>4.2 x - Air</td>
</tr>
</tbody>
</table>

RC Reduction of:
- 7.5 – Cu/Air
- 3.5 – Cu/Low-k
# Properties of Porous Ultra Low-k Materials vs. Oxide

<table>
<thead>
<tr>
<th>Property</th>
<th>Low-k</th>
<th>Oxide</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density (g/cm³)</td>
<td>1.03</td>
<td>2.2</td>
</tr>
<tr>
<td>Dielectric Cons.</td>
<td>~1.9-2.5</td>
<td>4.1</td>
</tr>
<tr>
<td>Modulus (GPa)</td>
<td>~3-9</td>
<td>55-70</td>
</tr>
<tr>
<td>Hardness (GPa)</td>
<td>~0.3-0.8</td>
<td>3.5</td>
</tr>
<tr>
<td>CTE (ppm/K)</td>
<td>~10-17</td>
<td>0.6</td>
</tr>
<tr>
<td>Porosity (est.)</td>
<td>~35-65%</td>
<td>NA</td>
</tr>
<tr>
<td>Avg. Pore Size</td>
<td>&lt;2.0-10nm</td>
<td>NA</td>
</tr>
<tr>
<td>Thermal Conductivity (W/m K)</td>
<td>0.26</td>
<td>1.4</td>
</tr>
</tbody>
</table>
Low-k – Integration Challenges

- Low k voiding
- Cu diffusion / barrier integrity
- Large pore structure
- Dielectric cracking
A DUAL DAMASCENE ‘UNIT’ STRUCTURE

Cu Seed

Cap or Stop

Low-K

Cap or Stop

Cap or Stop

Cap or Stop

Barrier for Cu
Dual Damascene Dual Top Hard Mask Process

M2 Hard Mask Pattern
1. Low-k – CVD or SOD
2. Etch stop / barrier – CVD
3. Hard Mask – SiO₂ & SiC
4. Conventional Litho

Post HM Open Etch & Ash
1. Define Trench with etch process
2. Ash resist
3. No low-k exposure to ash process
4. Allows litho rework at Via

VIA Pattern & Initial Bottom Mask Open
1. Litho Via on hard mask
2. Etch through hard mask

Low –k VIA Etch
1. Etch low-k @ M2
2. Etch Trench Stop
3. Leaves M2 mask
4. Some low-k exposure to Ash

Pot. Low-k Damage
1. Via Structure
Dual Damascene Dual Top Hard Mask Process

Ash & Bottom Hard Mask Open
1. In-situ ash (in etch tool)
2. Open (etch) bottom HM
Pot. Low-k Damage
1. Via Structure

VIA & M2 Simultaneous Etch
1. Drive trench down
2. Complete Via
3. Need to leave etch stop intact
Pot. Low-k Damage
1. Via Structure
2. Trench
3. Etch stop integrity

Cu Barrier Open and Via Cleans
1. Cu open
2. Clean to remove etch & ash residue
Pot. Low-k Damage
1. Moisture uptake
2. Etch residue uptake
3. Cu oxidation
4. All exposed low-k
Dual Damascene Dual Top Hard Mask Process

**Barrier Seed**  
(pore sealing)

1. Ar sputter etch  
2. ALD / CVD material  
   Ta, TaN, others  
3. Seal damaged pores

Pot. Low-k Damage  
1. Discontinuity  
2. Sputter Etch

**Cu Plate**

1. Fills Trench & Via simultaneously

Pot. Issues  
1. Fill uniformity  
2. Key Holes

**CMP**

1. Removes Cu & Hard Mask  
2. Post CMP cleans

Pot. Issues  
1. Uniformity  
2. Pressure – damage low-k  
3. Cu corrosion
Integration Schemes for Dual Damascene

Each scheme has its own integration issues and challenges.

There are also many variations on each scheme.

Issues

- Alignment
- Litho rework
- BARC “fencing”
- PR poison
- Litho rework
- Litho DOF
- BARC fill
- PR poison
- Litho rework
- High overall $k_{\text{eff}}$
- Etch Resist selectivity
- Litho Overlay
Simple So Far……Integration Issues

• Issues
  – Etch by-products are deposited on exposed low-k films
  – Aqueous processes can drive in contaminates and modify low-k structure
  – Etch, ash, and cleans difficult to control – pores, soft material – CD / uniformity, process selectivity, etc.
  – CMP processes put (shearing) forces on soft and weak low-k structures / materials
  – Discontinuous barriers can allow Cu diffusion / failure
  – Specific integration issues to each low-k
Resist Poisoning

- Resist poisoning occurs when nitrogen containing chemistries or films can outgas (NH₃) into resist
  - Use of N₂/H₂ ash processes
  - Exposure of SiCN barrier during Via First Etch Scheme
  - Use of Nitrogen containing films in other areas of stack

Resist-poisoning *(caused by trapped amines/ NH₃)*
Low-k Voiding

- Low-k voids occurs during post Cu plating anneal
- Wider low-k spacings exhibit less voiding
Traditional microwave oxygen ashes

- Isotropic ash processes remove also C from porous low-k film
- Makes low-k hydrophilic

Reaction products: CO, CO₂, H₂O ↑

Isotropic
Anisotropic

Low-k damage:
- C depletion
- Si• + H₂O → SiOH
**Assumed low-k voiding mechanism**

1. **Fluorine captured in pores of low-k**
   - Primary source is etch process
   - Ash releases fluorine from resist/polymers
   - Incomplete removal in post ash wet clean

2. **Low-k film becomes hydrophilic**
   - Ash & etch chemistries can deplete Carbon
   - Promotes moisture uptake at sidewalls - cleans
   - Discontinuity in barrier/seed layer – Cu plate
   - HF formation

3. **HF reaction with low-k, SiNx**
   - Anneal starts HF reaction with low-k
   - ‘Sub-micron pressure cooker’
   - Mechanically induced stress from copper lines
   - SiCN not attacked
Cu Diffusion / Depletion

- Cu diffuses out of structures
  - Barrier discontinuities
  - Moisture / diffusion gradients
  - Electro-thermal stress

- Structure fails from Cu depletion

TEM of Cu diffusion into low-k

Open Via due to Cu depletion
Dielectric Cracking

- CMP – “final straw”
  - Structural / compound changes to low-k during etch, ash, cleans
  - Stresses from CMP “wiggle” structures
Solutions

• **Low-k voiding**
  – Implement a “pore sealing” process
    • prevent contaminants & moisture from entering low-k
  – Implement a cleans process w/ restoration
    • remove contaminants & restore C(H3)
  – Minimize aqueous treatments
  – Novel plasma, strip and cleans

• **Dielectric Cracking**
  – Modulated by low-k damage & CMP force
  – Restore low-k properties (cleans)

• **Cu Diffusion / Depletion**
  – Advanced barriers
  – Novel liners
Conclusions

• **Low-k are difficult materials to integrate**
  – Multiple integration approaches, all have pros & cons
  – Specific issues to different low-k
    • Density & porosity fluctuations by depth
    • Organic materials – behave like photo-resist
  – Require advance stripping, cleaning, metalization & CMP

• **Need to minimize or restore low-k damage**
  – Neutral beam plasmas
  – Ion beams for stripping and pore sealing
  – Restorative cleans processes – scCO$_2$ w/ HMDS
  – Advanced barriers and metalization processes
  – Pore sealers – sacrificial or permanent