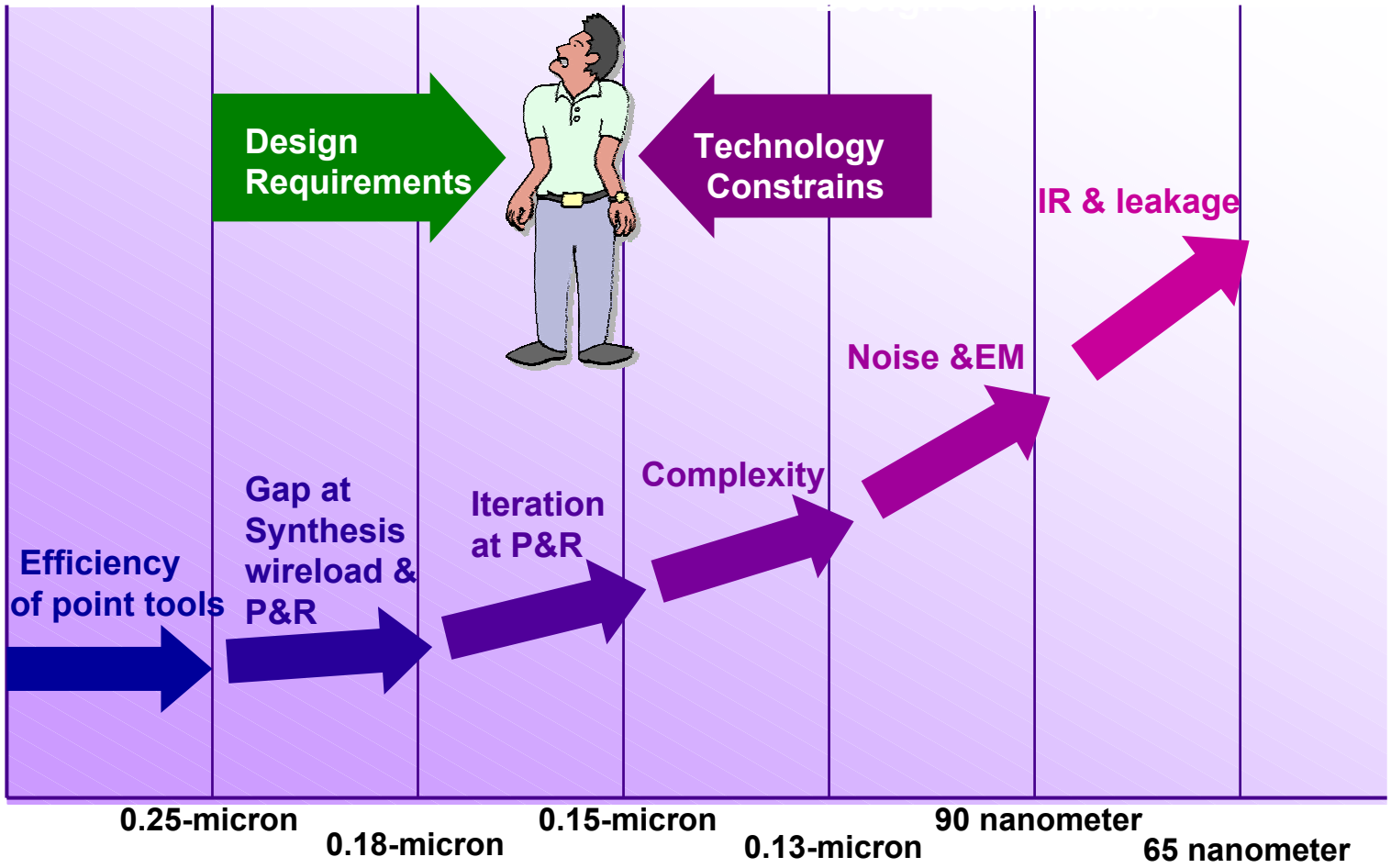
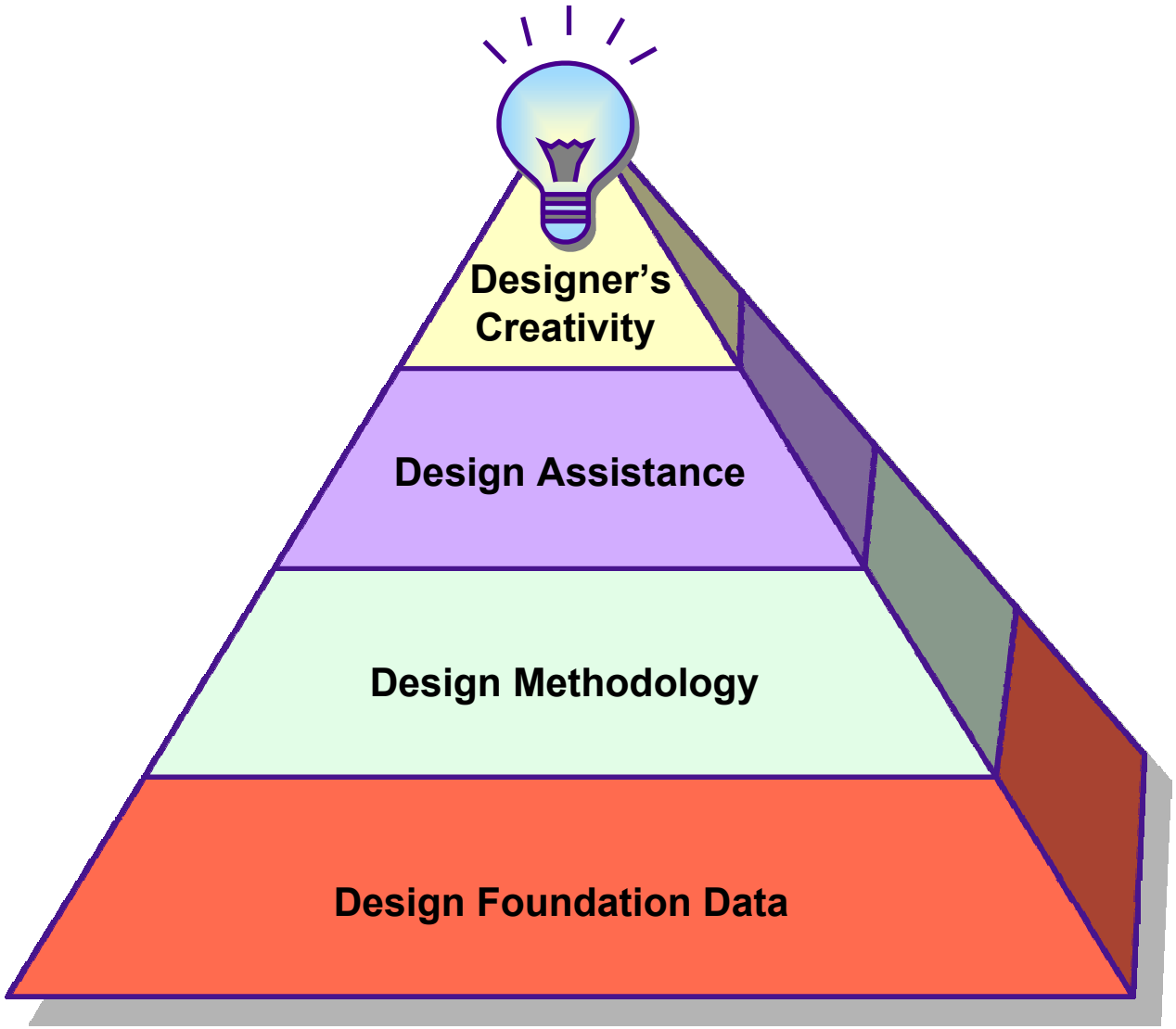
TSMC Design Services:

Bringing Your Products to Market Faster

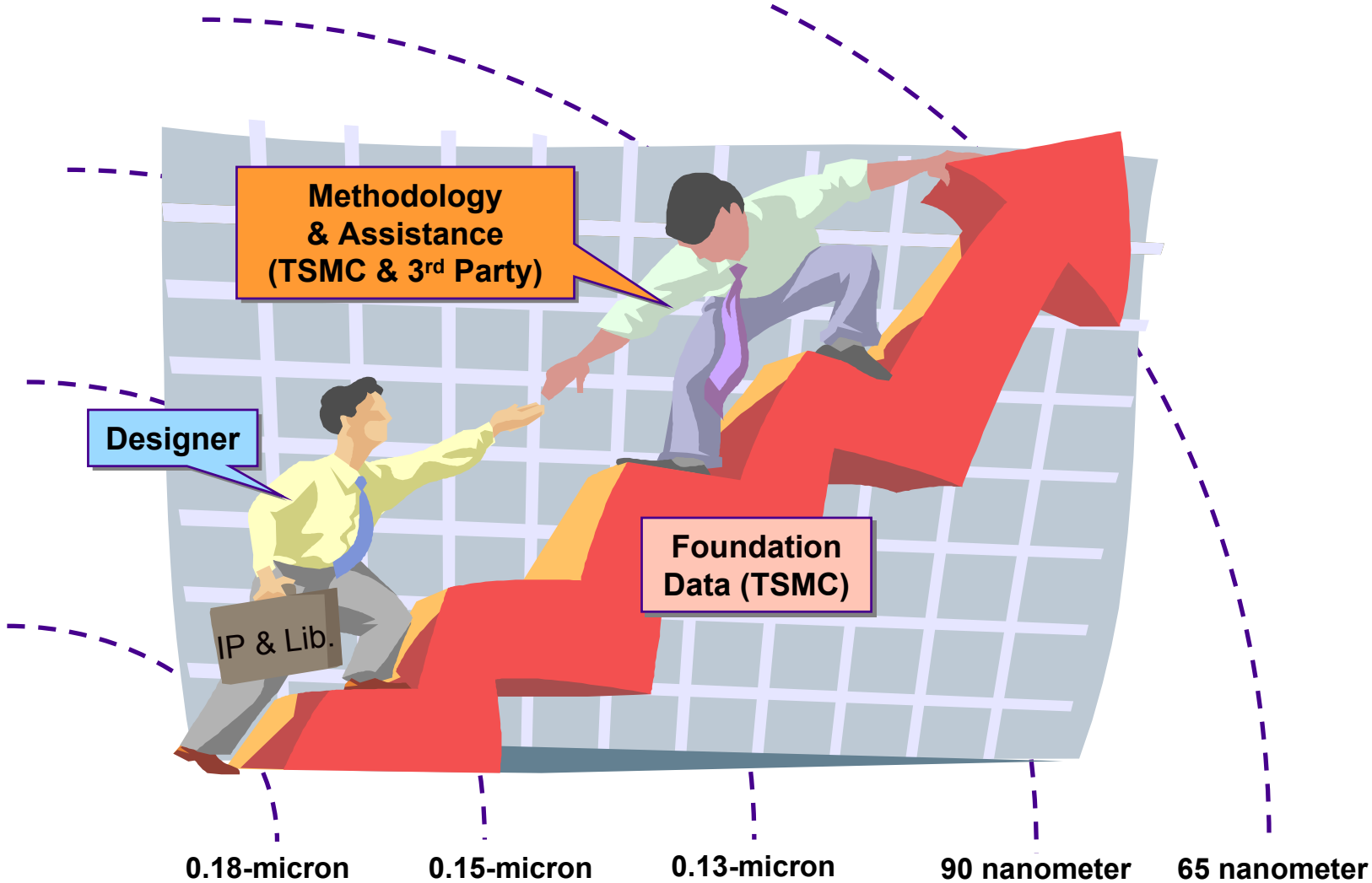
Intense Design Challenges



What We Provide Besides Wafers



Enabling Time to Volume



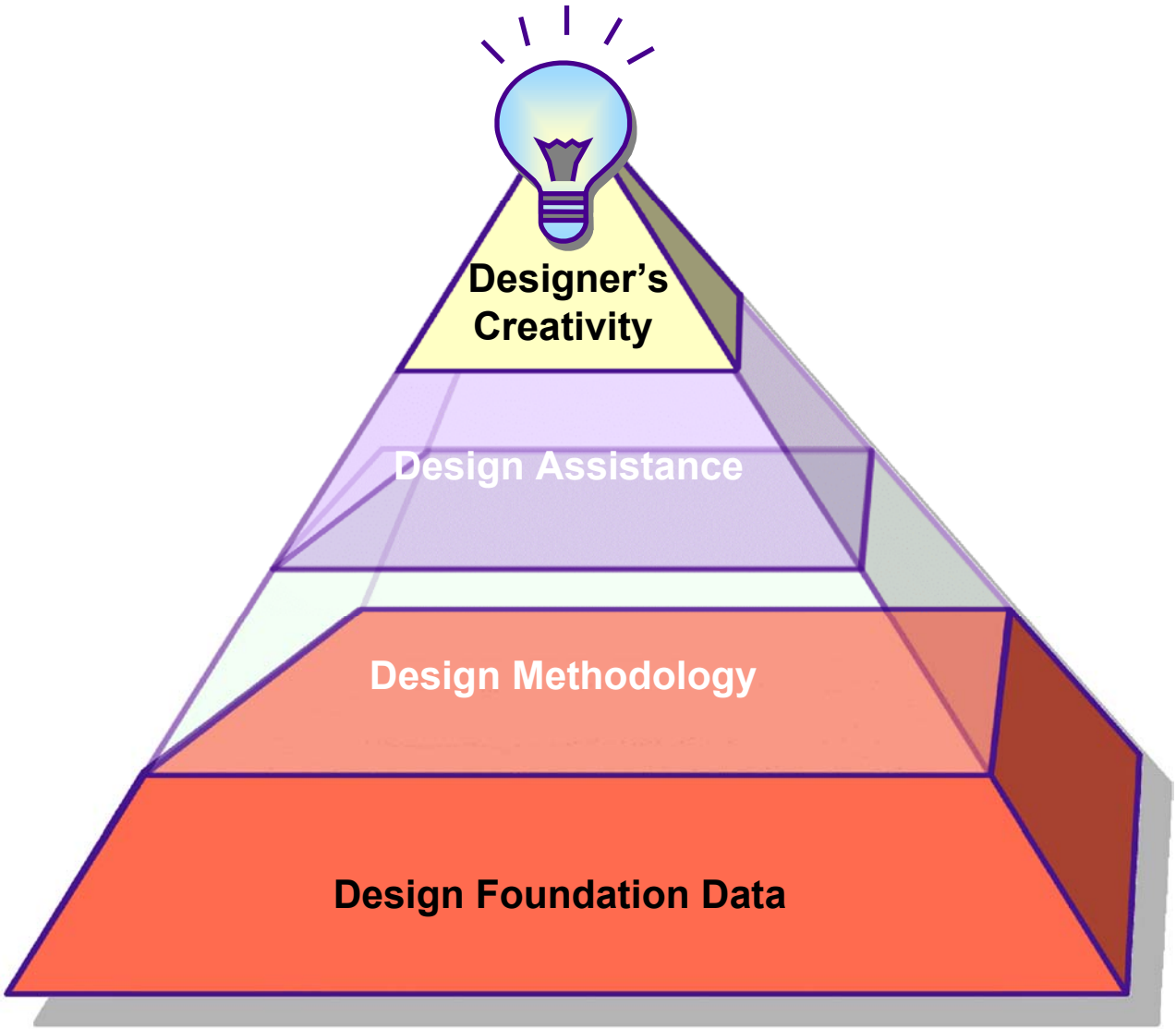
Extensive Portfolio of Alliances

- **Foundation:** EDA Alliance
  - Design Rule related: DRC, LVS
  - Spice Model related: Spice, RCX
- **Methodology:** EDA Alliance
  - Digital Reference Flow
    - Four generations of quality delivery
  - RF/MS Design Kit
    - Foundry industry's first and broadest node coverage
- **Design Assistance:**
  - TSMC Implementation Service
  - 3rd-Party Implementation Service
  - Silicon Debug and Repair Service

tsmc

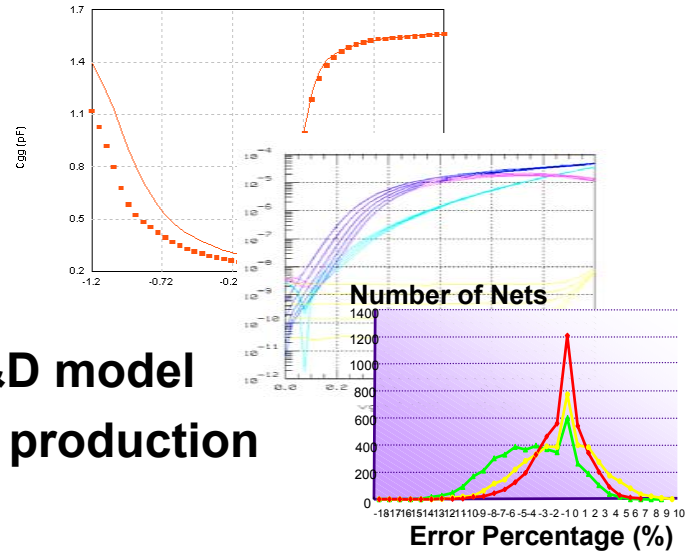
DCA Alliance

Validation Alliance

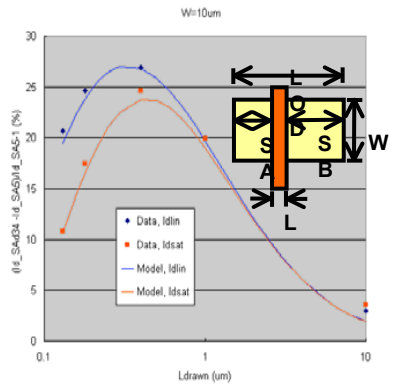


Foundation Data Quality

SPICE Model



- **Device Modeling**
  - **Version strategy**
    - **V0.0x, V0.x – guess model, R&D model**
    - **V1.x, V2.x – silicon model and production**
  - **Accuracy**
    - **Silicon correlation**
    - **Corner models (-40° ~ 125°)**
  - **Improved MOSFET Modeling**
    - **Vt Modeling**
    - **Gate current modeling**
    - **STI stress effect modeling**
    - **Gate capacitance modeling**
    - **Diode leakage current modeling**



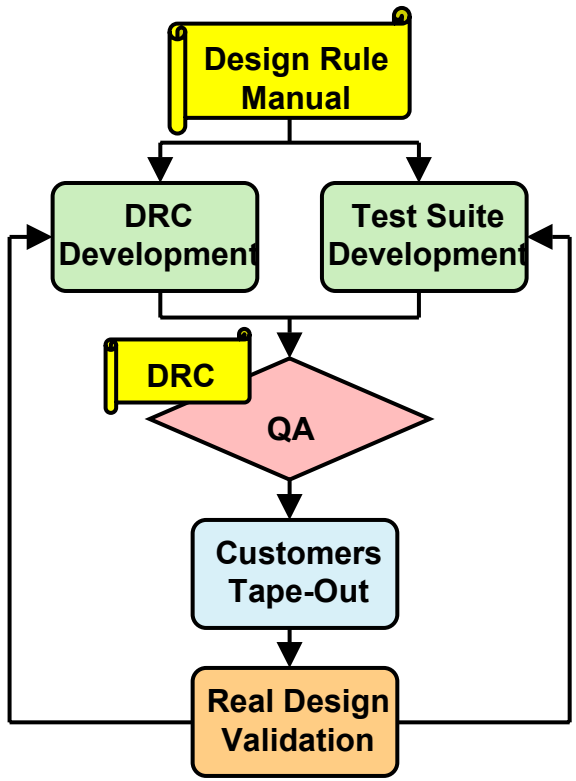
Foundation Data Quality

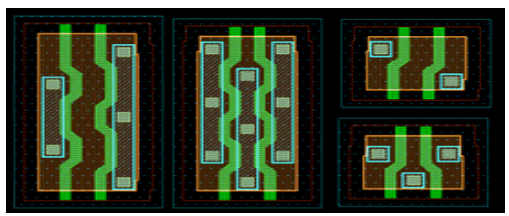
- DRC, LVS
  - Early Availability

    In-house development synchronizes release with DRM
  - High Quality

    Double-blind QA ensures industry-leading quality
  - Extensive Portfolio

    Broad support of widely used tools

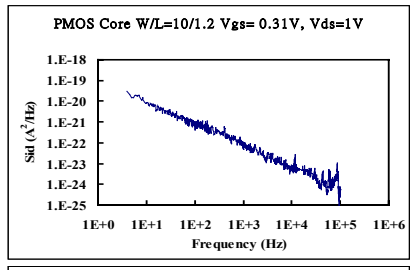


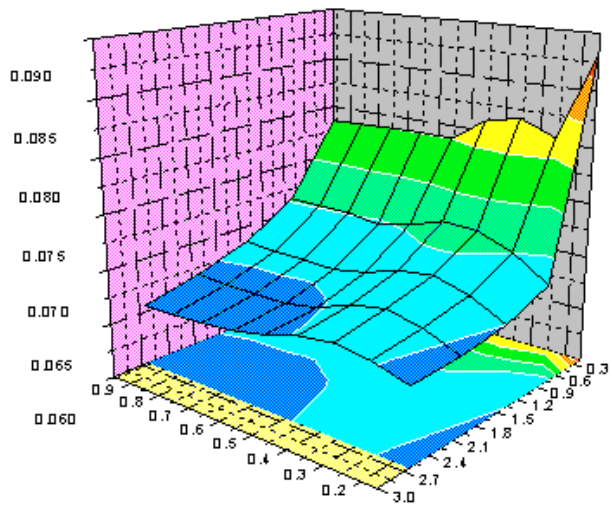


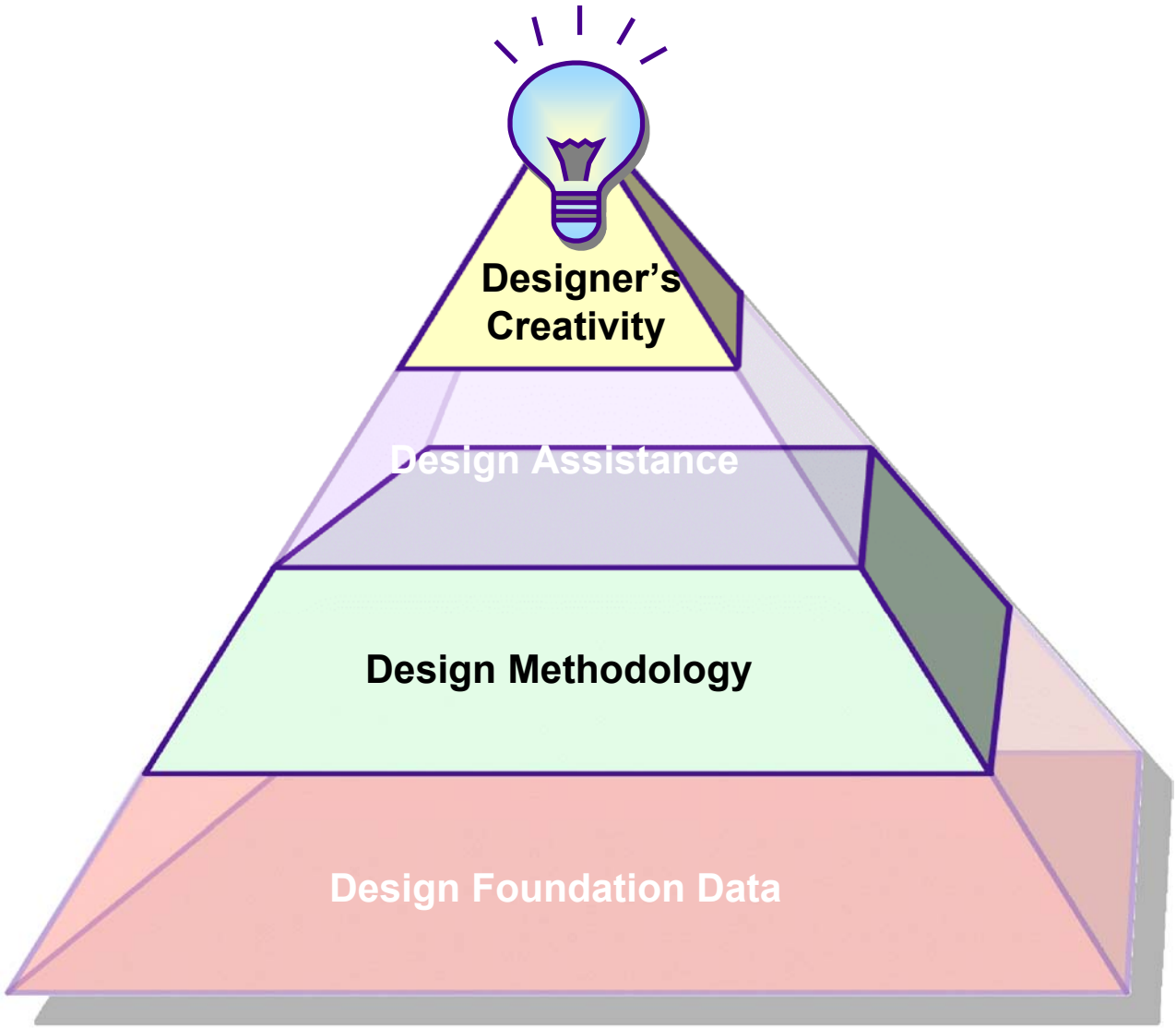
Foundation Data Quality

Extraction Model

- Interconnect Model
  - Realistic Corner Model
    - Reflects combination of multi-layer statistical corners
  - Performs silicon correlation with commercial tools
  - RC Accuracy enhancement
    - Model with metal-thickness
    - 90 nanometer enabled

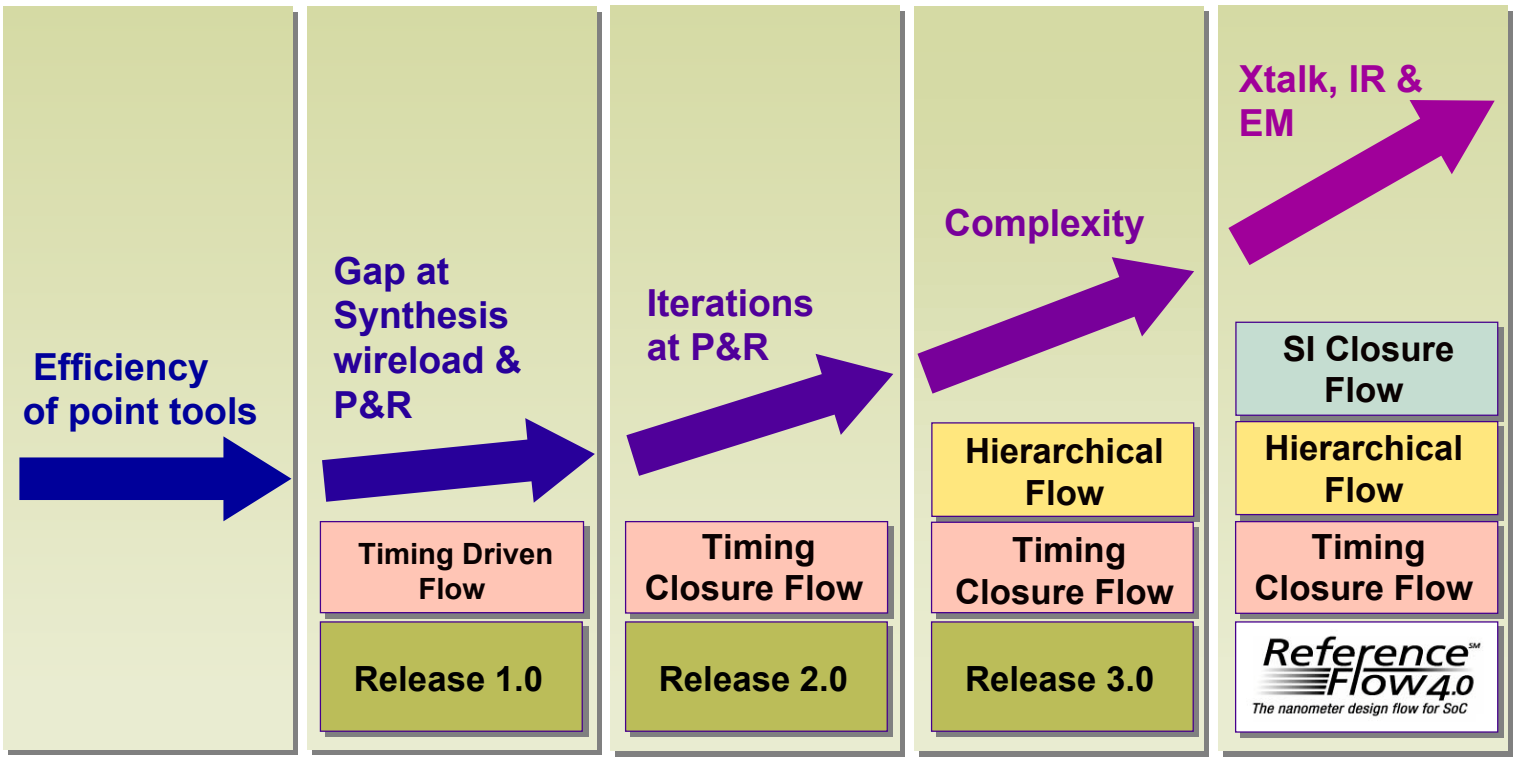






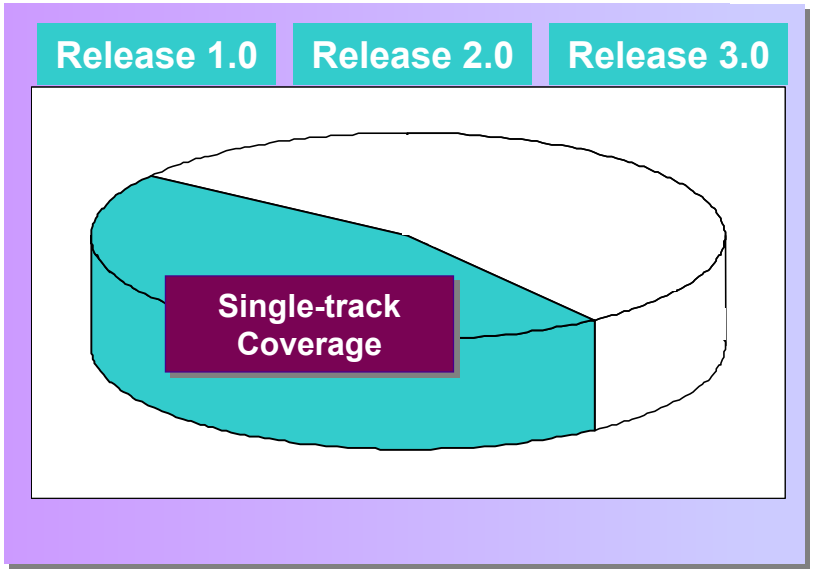
Industry's Most Comprehensive Flow

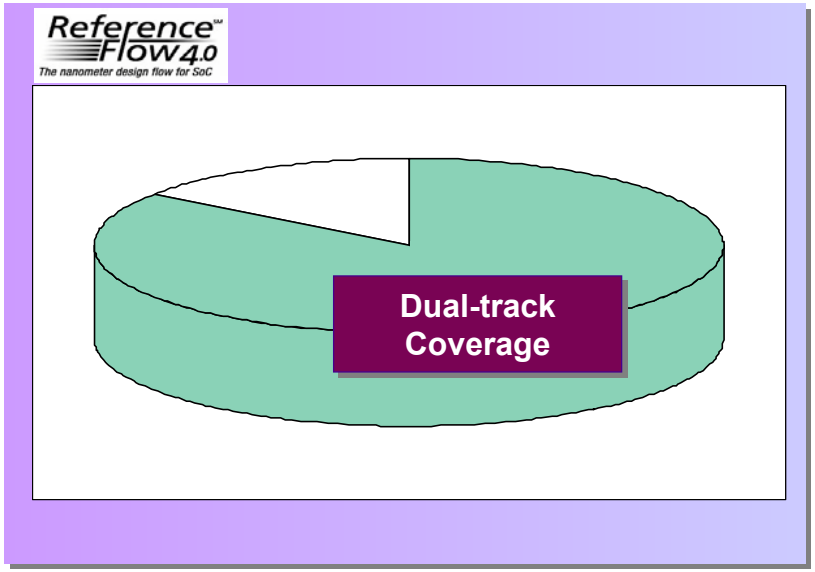
- Four consecutive quality deliveries
- Each release addresses new design challenges
- All releases are backward compatible



Dual-Track Reference Flow

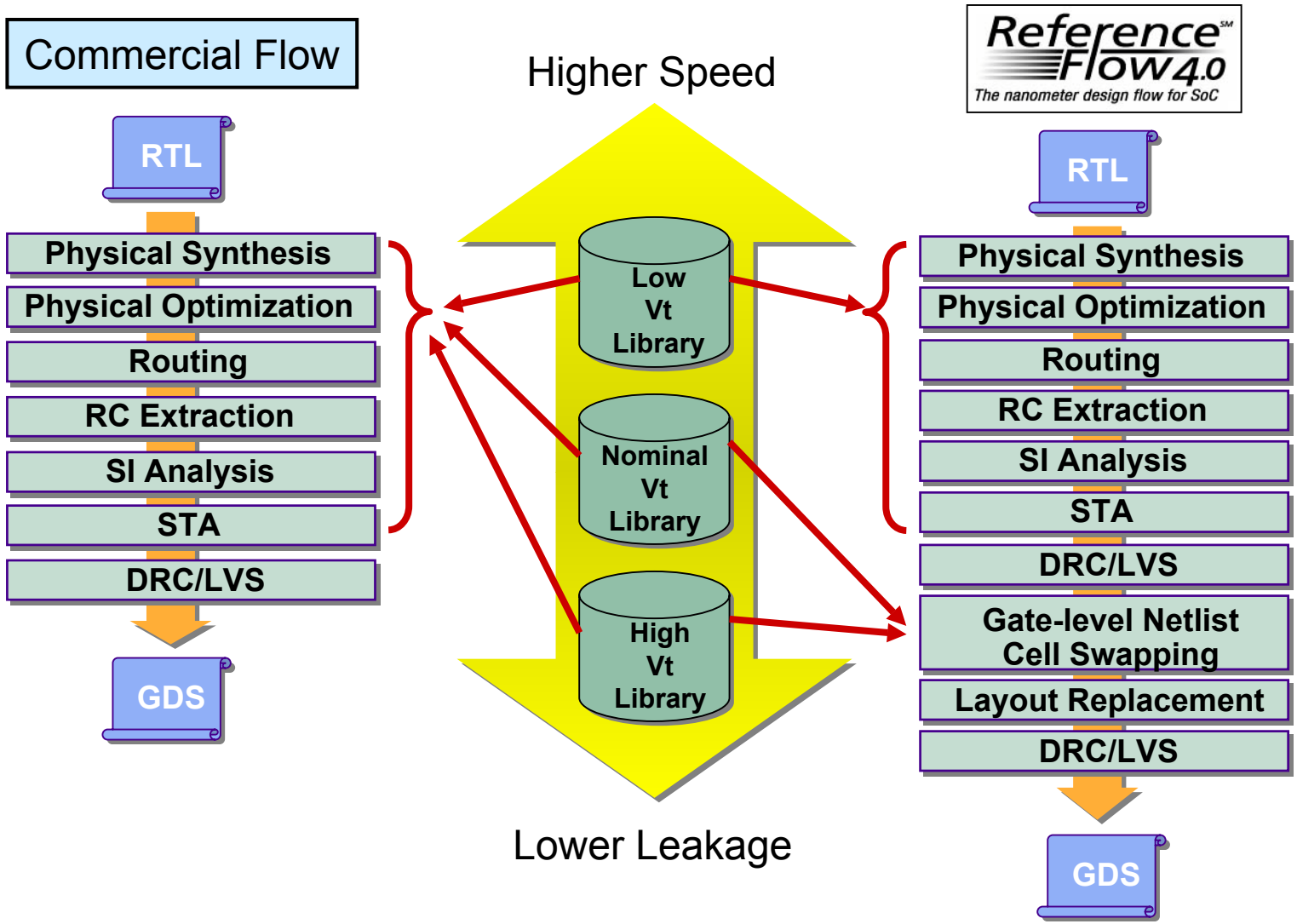
- Expands customer support through multiple major vendors coverage
- Responds to customers' feedback





Note: TSMC Customer Base Coverage (physical implementation)

Multi-Vt Solution for Power Optimization

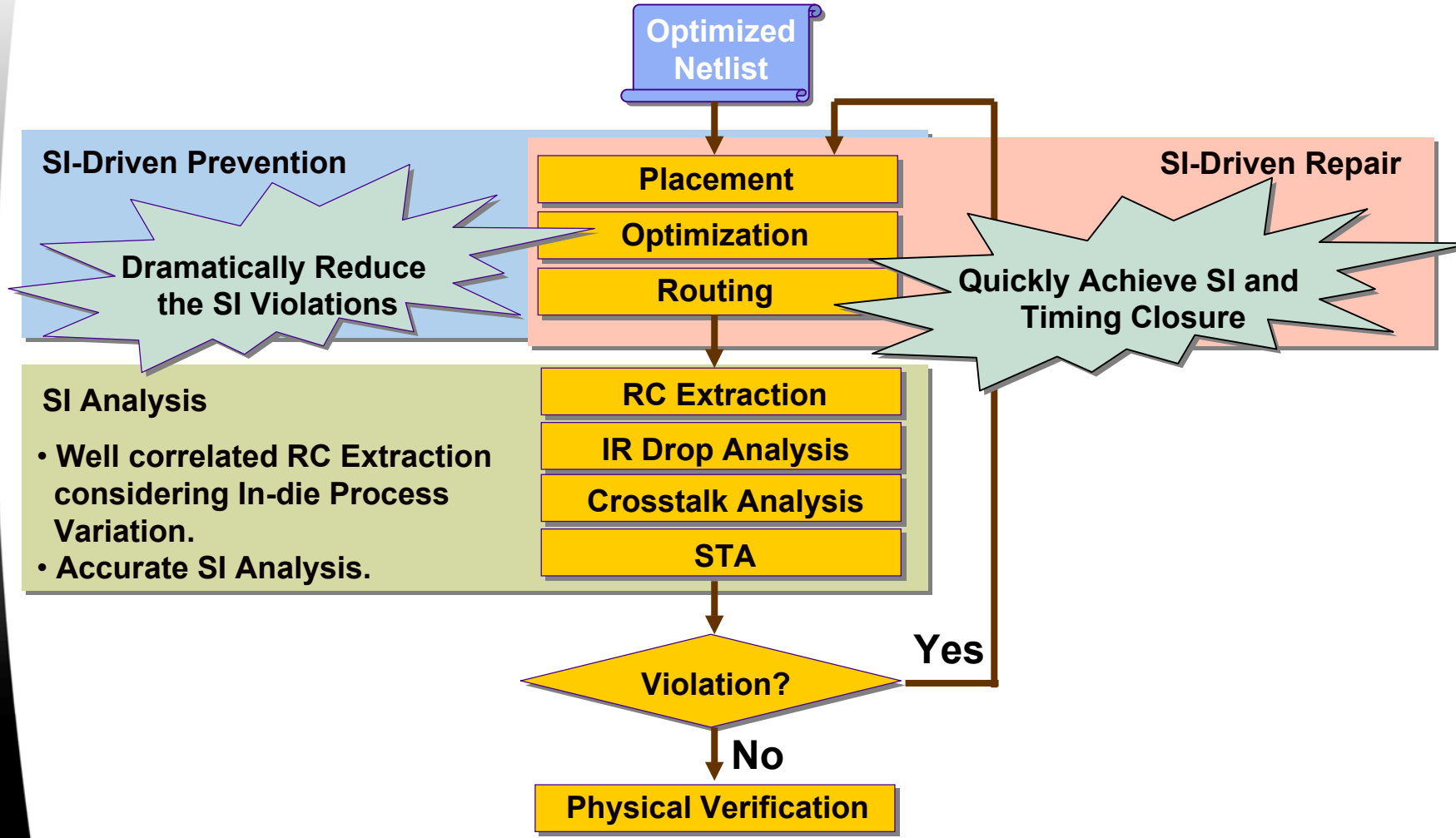


Power/Speed Optimization Example

- Design Case: ARM RISC Processor
- Technology: TSMC 90 nanometer

Case	Power (mA)		Frequency (MHz)	Cell Distribution		
	Leakage	Dynamic		HVT	HVT	HVT
LVT	21.6	123.8	360			100%
NVT	3.6	92.9	280		100%	
HVT	1.3	90.7	200	100%		
N/L VT	10.5	106.2	360		72%	28%
H/N/L VT	9.7	105.5	360	43%	27%	28%
H/N VT	2.2	91.5	280	73%	27%	

SI and Timing Closure (Prevention, Analysis and Repair)



Demonstration of SI and Timing Closure

- TSMC 0.13-micron technology
- Two million-gate design

	Number of glitch violations	Number of timing violations
1st Iteration	1437	622
2nd Iteration	116	112
3rd Iteration	18	40
Final Clean-up	0	0

- Achieve both SI and timing closure with Reference Flow 4.0

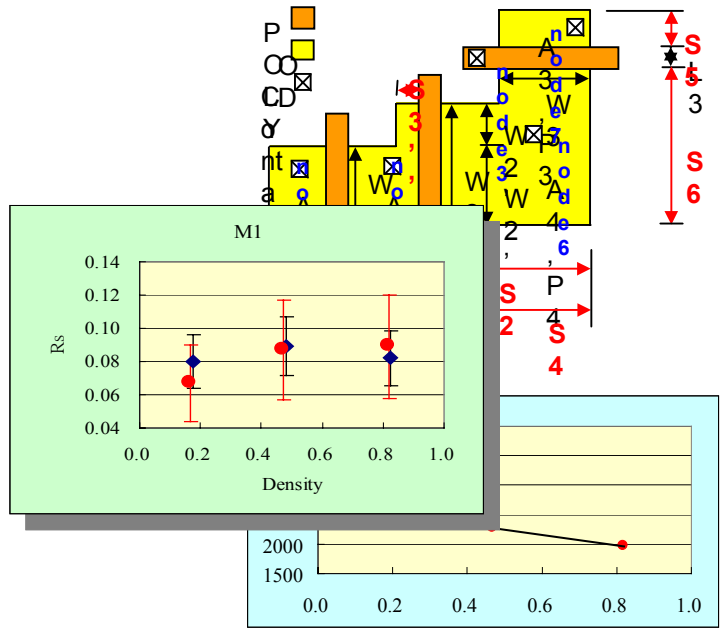
DFM (Design for More?)

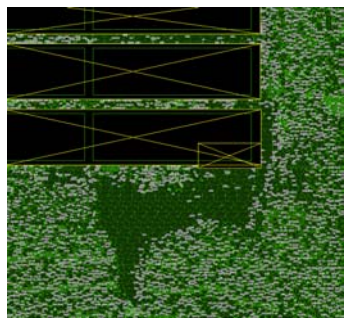
- How can a chip fail? How to avoid failures?
  - During design implementation (DFA – Design for Accuracy)
    - Design Spec
      - Functional error (Logic – function verification)
      - Electrical error (Timing, power – timing closure, power analysis)
    - Silicon technology spec
      - Physical error (rule -- DRC check)
      - Circuit error (silicon model, SPICE simulation)
  - During manufacturing (DFM – Design for Manufacturability)
    - Mask/OPC induced
    - Process steps induced
    - Material induced
  - During usage (DFR – Design for Reliability)
    - Time induced (electron-migration, wire-heating)
    - Situational signal induced (cross-talk delay and glitch)
    - Environment induced (temperature, shock)

Design for Accuracy

DFA (increase accuracy; bring out best performance)

- Length of Defusion (LOD)
  - STI stress effect
  - Function of length
  - BSIM3 & BSIM4 support
  - ADS, Eldo, Hspice, Spectre
- Metal thickness/width modeling
  - RC accuracy
  - Corner model
- IR Drop
  - Capacitance calculation
  - De-coupling cell insertion
- Cross-talk
  - Delay, noise or glitches
  - SI design closure
    - Prevention
    - Analysis
    - Repair

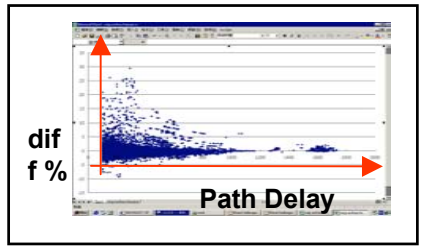




DFM (Design for Manufacturability)

- **Mask induced**
  - Lithographical effect
    - Layer density rule
- **Process steps induced**
  - CMP effect
    - Metal thickness variation modeling
    - Metal density rule
  - Charge zap effect
    - Antenna rule
- **Material induced**
  - STI effect LOD
    - LOD device modeling
  - Dielectric material
    - Maximize redundant VIA
  - Stack VIA effect
    - Stack height limit

Analysis of Dummy Metal Impact on Delay



Width						
Spacing	0.20	0.40	0.60	1	2	3
0.21	2.653					
0.24	2.698					
0.42	2.339					
0.63	2.304					

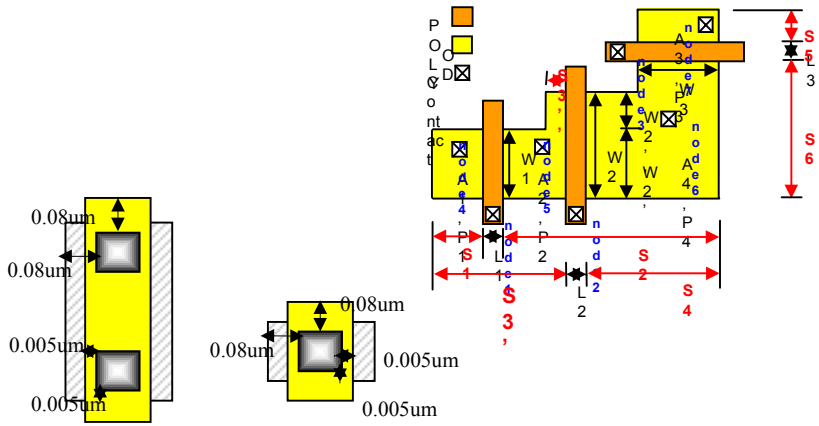
S\W	0.20	0.40	0.60	1	2	3
0.21	0.389	0.389	0.389	0.389	0.389	0.389
0.24						
0.42						
0.63						
0.84						

S\W	0.20	0.40	0.60	1	2	3
0.21	0.2275	0.4275	0.6275	1.0275	2.0275	3.0275
0.24	0.2275	0.4275	0.6275	1.0275	2.0275	3.0275
0.42	0.2275	0.4275	0.6275	1.0275	2.0275	3.0275
0.63	0.2275	0.4275	0.6275	1.0275	2.0275	3.0275
0.84	0.2275	0.4275	0.6275	1.0275	2.0275	3.0275

Resistivity

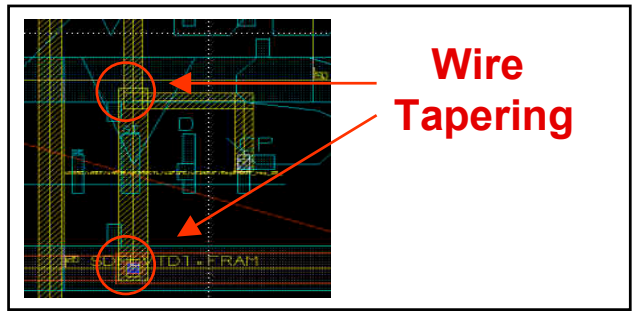
Thickness

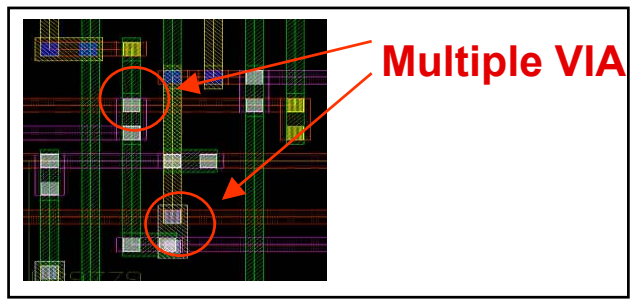
width



DFR (Design for Reliability)

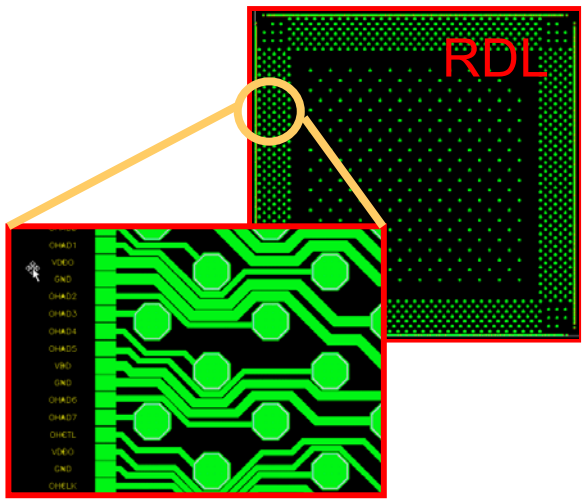
- DFR (avoid failure in use; increase MTBF)
- Electro-migration
  - Power EM
    - Power mesh
    - Wire tapering
  - Signal EM
    - Multiple via insertion
- Cross-talk
  - Delay, noise or glitches
  - SI design closure
    - Prevention
    - Analysis
    - Repair
- Hot electron
  - Safe IR control design practice
- Self-heating wire
  - Safe power/clock mesh design practice

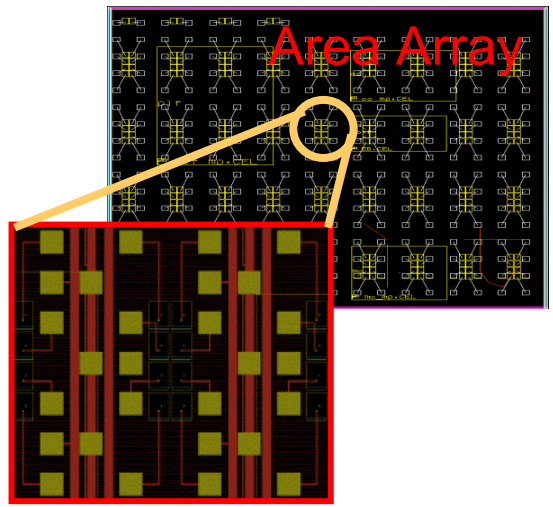




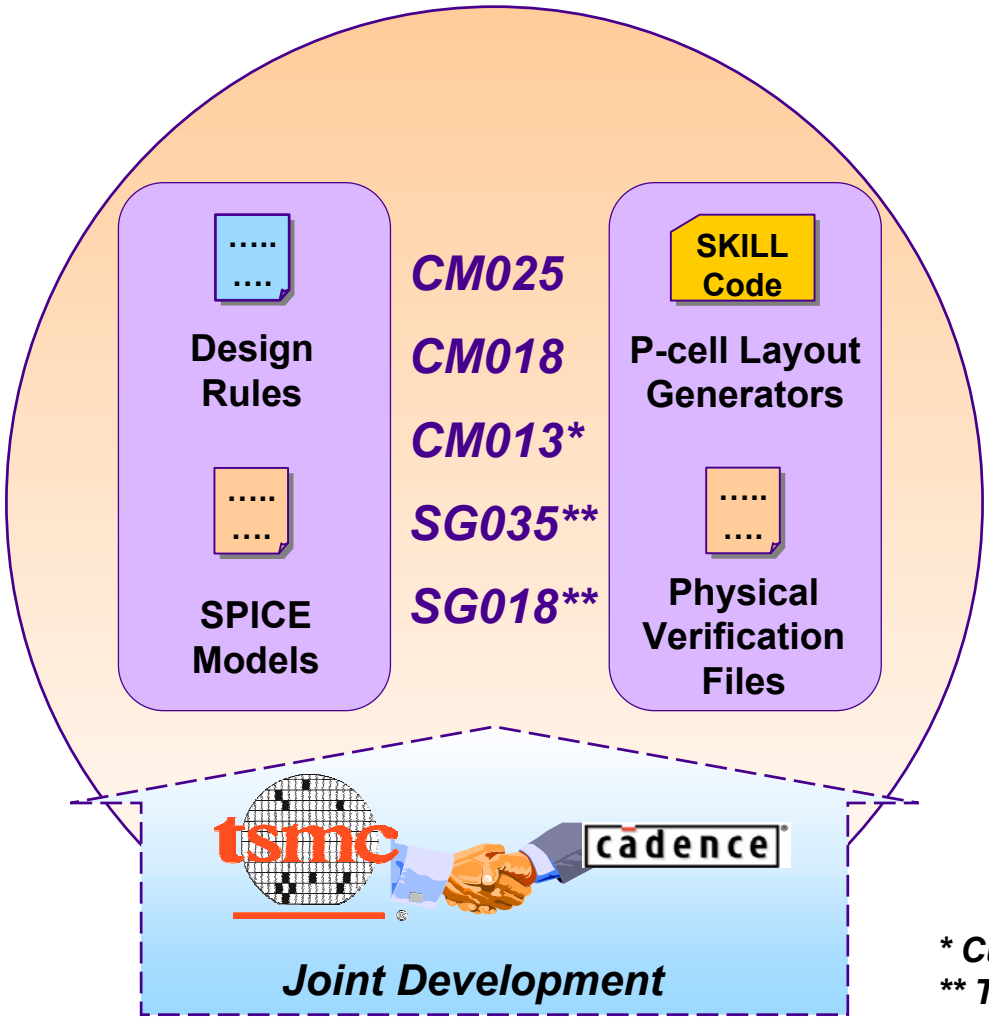
Flip-Chip Capability

- RDL Flow (available)
  - Silicon proven flow on several customer chips.
- Area Array Flow (under development)
  - Cluster approach using TSMC developed flip chip I/Os
  - Silicon validated on internal test chip
  - Fine tuned for new I/O cells (better structure)





PDK for High Quality MS/RF Designs



Mixed Signal/RF Designers

Download & Support

(TSMC-Online)

**** Currently posted with CL013***
***** Temporary posted at Cadence web site***

For Mentor ADK contact Mentor

TSMC PDK Device List

Elements

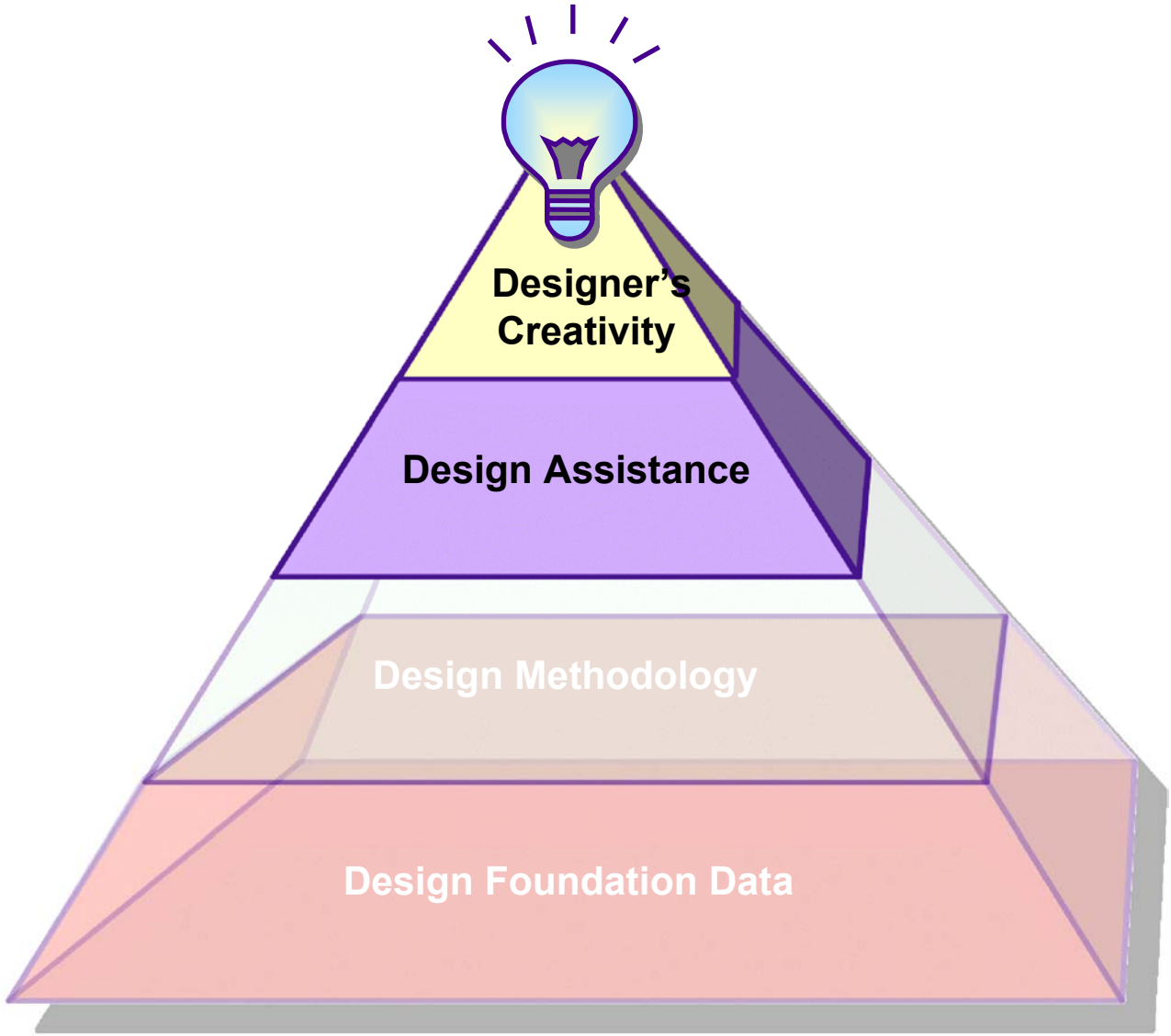
Active	Passive	Supporting
MOS	Resistor	EDS
	Inductance	RF Pad
	Capacitor	
	Varactor	

Features

4-T model	3-T model	Noise model	Statistical model
MOS	Resistor	Thermal	Corner
	Capacitor	Flicker	Matching
	Inductance		

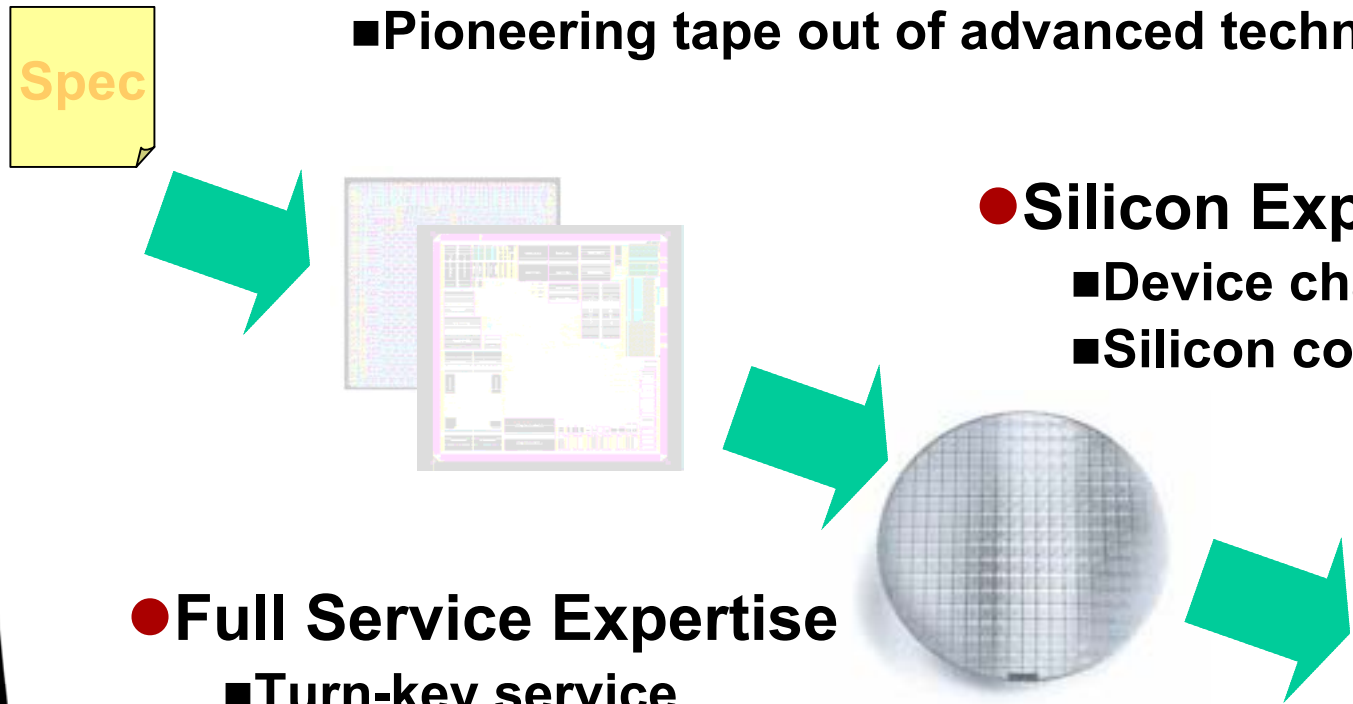
Methodology

Monte-Carlo



TSMC In-house Implementation Service

- **Design & EDA Expertise**
  - Birth place of TSMC reference flows
  - In-house library, I/O & IP development
  - Pioneering tape out of advanced technologies



- **Silicon Expertise**
  - Device characterization
  - Silicon correlation

- **Full Service Expertise**
  - Turn-key service
  - Key customer driven
  - Product engineering

Industry's Largest Design Center Alliance

28 Worldwide Partners

Over 400 Tapeouts in 2002

The Applications You Want

- Computer
- Consumer
- Communication

The Services You Require

- Platform-based Design
- Memory Characterization
- Full Custom Layout
- RTL-to-GDSII
- DFT Service
- Mixed Signal Design
- Netlist-to-GDSII
- RF Design
- SRAM Design

The Business Models You Prefer

- NRE-based Outsourcing Service
- Turnkey/ASIC Service
- T&M-based Consulting Service

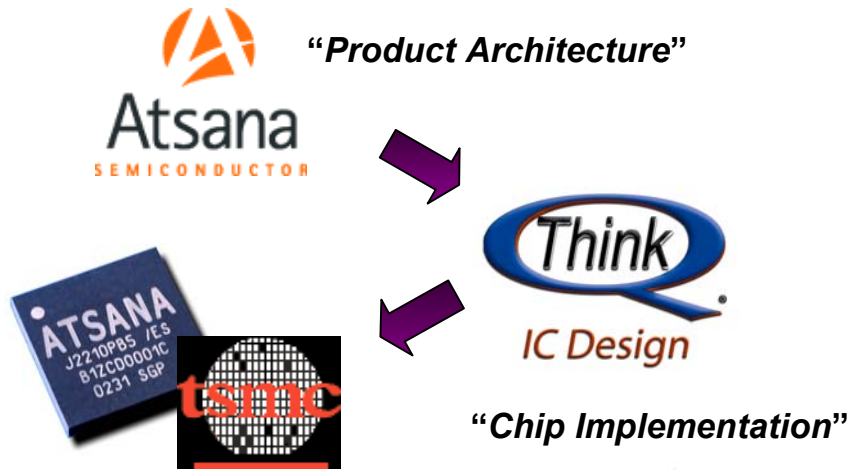
DCA Success Story - Consumer

QThink Customer Design Success

Atsana J2210 Media Processor

Ideally suited to video and image encoding and decoding applications that are reliant on a low power, low cost integrated processing solution. Applications include:

- **Wireless Video Phones**
- **Camera Accessory Modules**
- **Wireless PDAs**
- **Wireless PC/ Network Cameras**

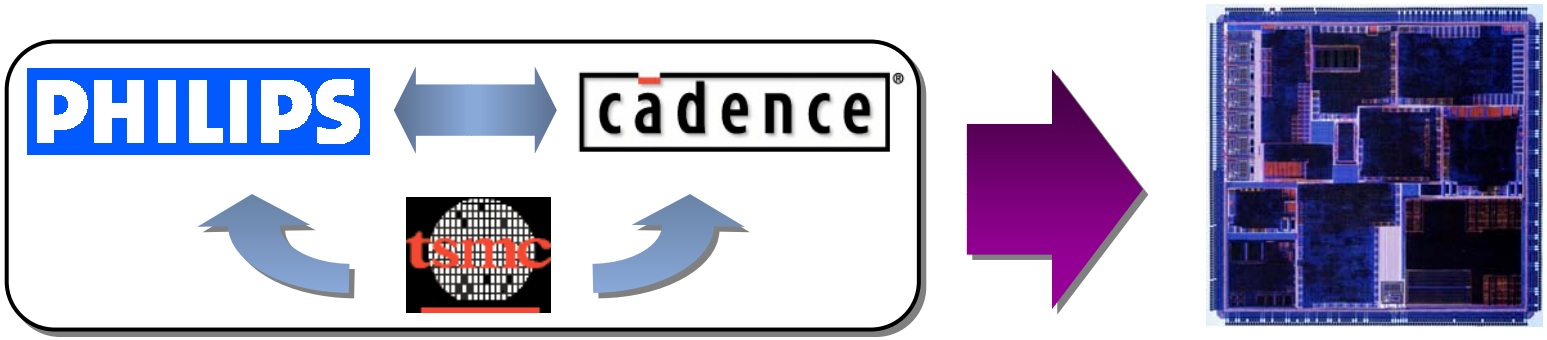


"We chose QThink because our project team found that they offered a solid solution with a flexible interface that would allow customization of some areas of the design. They were one of the few that had true 0.13u tape-out experience along with strong skills in the generation and integration of custom macros, and that gave us good confidence that the project would be successful."

Richard Bériault
Director of Engineering
Atsana Semiconductor

- ***FIRST-PASS SILICON SUCCESS!***
- **TECHNOLOGY: 0.13 µm CMOS process, 100 MHz operating frequency**
- **APPLICATION: Array Processor for parallel operations, ARM922T™ for host and high-level instructions**
- **PACKAGE: 180 pin CABGA**
- **POWER: 1.2V Core and 2.5/3.3 V I/Os, Multiple Power Modes**

DCA Facilitates Customer Success



Chip Photomicrograph of Philips Semiconductors' EDAC 2002 award winner Nexperia-based Home Entertainment Engine pnx8526

"Philips Semiconductors selected Cadence Design Foundry to join Philips existing design capability in a design partnership to implement the pnx8526 product.

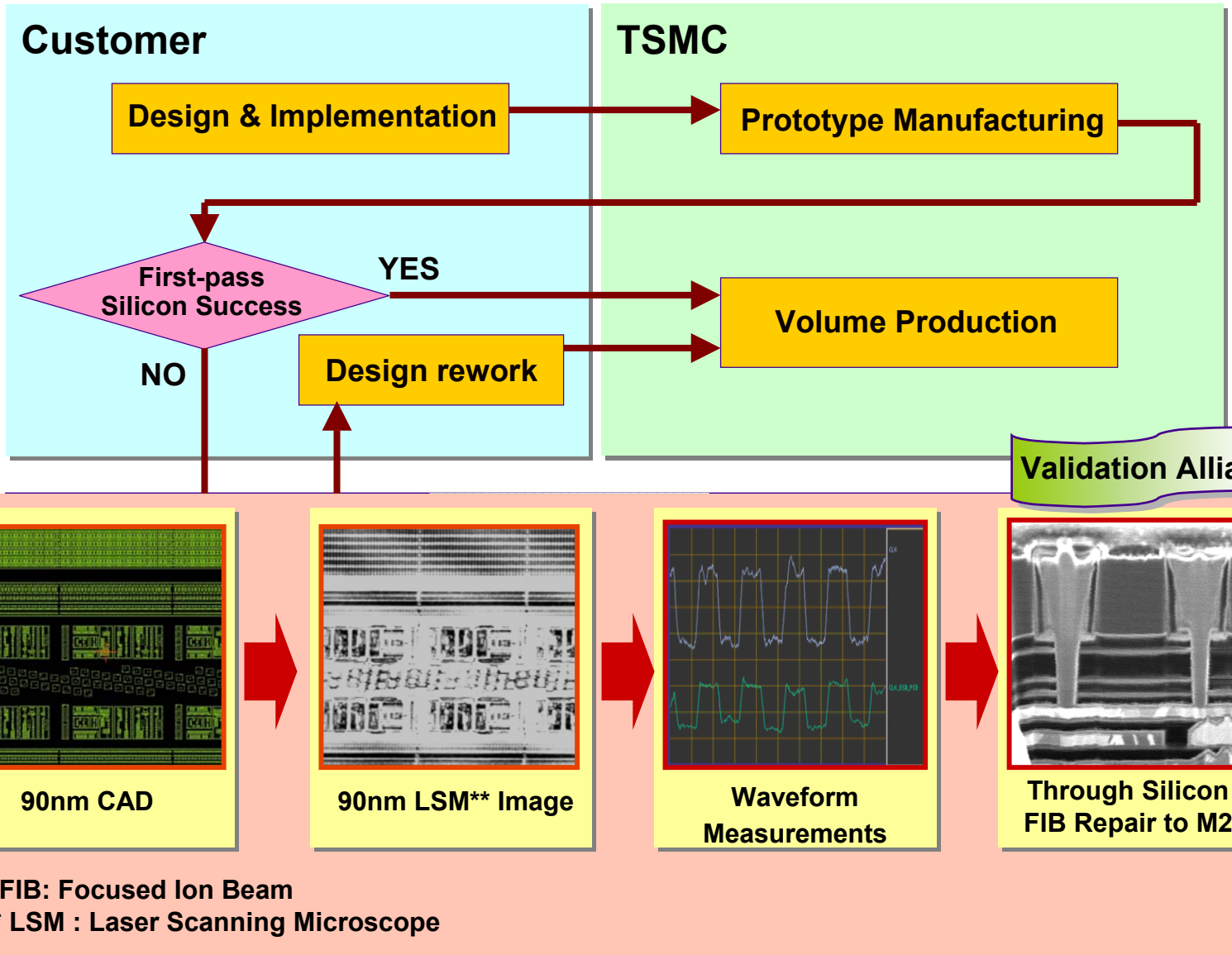
The combined efforts of both teams resulted in an essentially first silicon success product that met the end customer's aggressive production IC availability requirements"

Wout Bijker
Vice-President, Business Line Broadband Home Servers
Philips Semiconductors

- 5 Million Gates
- 778Kbits of Sram (232 instances)
- 0.13 um TSMC (1P8M + RDL)
- 158MHz core clock speed, 56 domains
- 150MHz Processor, 200MHz DSP
- Complex Analog functions.
- 8.6mm x 8.2mm
- 367 I/Os and Power
- Wirebond, BGA
- Power consumption 2.6W

First Silicon Success®

IC Validation Alliance – Bridging The Gap Between Prototype & Volume



IC Validation - Business Model & Program Snap Shot

- The business model you need from 
  - Guaranteed localization of failure; no service charge if failure is not localized
  - Project based pricing; remove the time and materials risk
- 28 IC validation projects completed in the program's first 14 months

Technology	0.13 μm	0.18 μm	0.25 μm	0.35 μm
# of Projects	13	13	1	1

- 8 more projects underway
- Covering computer, consumer and communication applications

Summary

Time-to-Design Start

- High quality, highly consistent foundation data
  - DRC, LVS, RCX, SPICE

Time-to-Tapeout

- Robust and state-of-the-art methodology support
  - Four generations of Reference Flow
  - Expanded PDK for RF/MS design needs
- Most comprehensive 3rd-party and in-house design services portfolio

Time-to-Volume

- Flexible service business models
- Safety net provided through Validation Service

TSMC Design Services:
Bringing Your Products to Market Faster

Reference

A Complete Design Service Package

Reference Flows

Reference Flow 4.0
The nanometer design flow for SoC

Cadence, Synopsys
Mentor, Syntest

DRC

Cadence	Assura Diva Dracula
Mentor	Calibre
Synopsys	Hercules

Spice

Agilent	ADS
Cadence	Spectre
Mentor	Eldo
Synopsys	H-Spice

Mixed-Sig /RF Design Kits

Cadence	PDK
Mentor*	ADK

LVS

Cadence	Assura Diva Dracula
Mentor	Calibre
Synopsys	Hercules

Application Notes

Usage Guideline etc.

RCX

Cadence	Assura Fire&Ice(QX) HyperExtract Nautilus
Mentor	xCalibre
Sequence	Columbus
Synopsys	Arcadia Raphael NES Star RC(XT)

Substrate

Cadence	Substrate-Storm**

** In progress* *** Upon request*

EDA Alliance

World Leading Design Foundation and Design Methodology

Methodology

Reference Flow

Dual implementation tracks Enabling direct manufacturability into TSMC's advanced technologies

Analog Design Kit

Off-the-shelf productivity from industry-leading analog tools

Foundation

DRC

Double-blind Quality Assurance

LVS

Matches device (spice), layers (design rule) and application notes

SPICE

Industry leading models

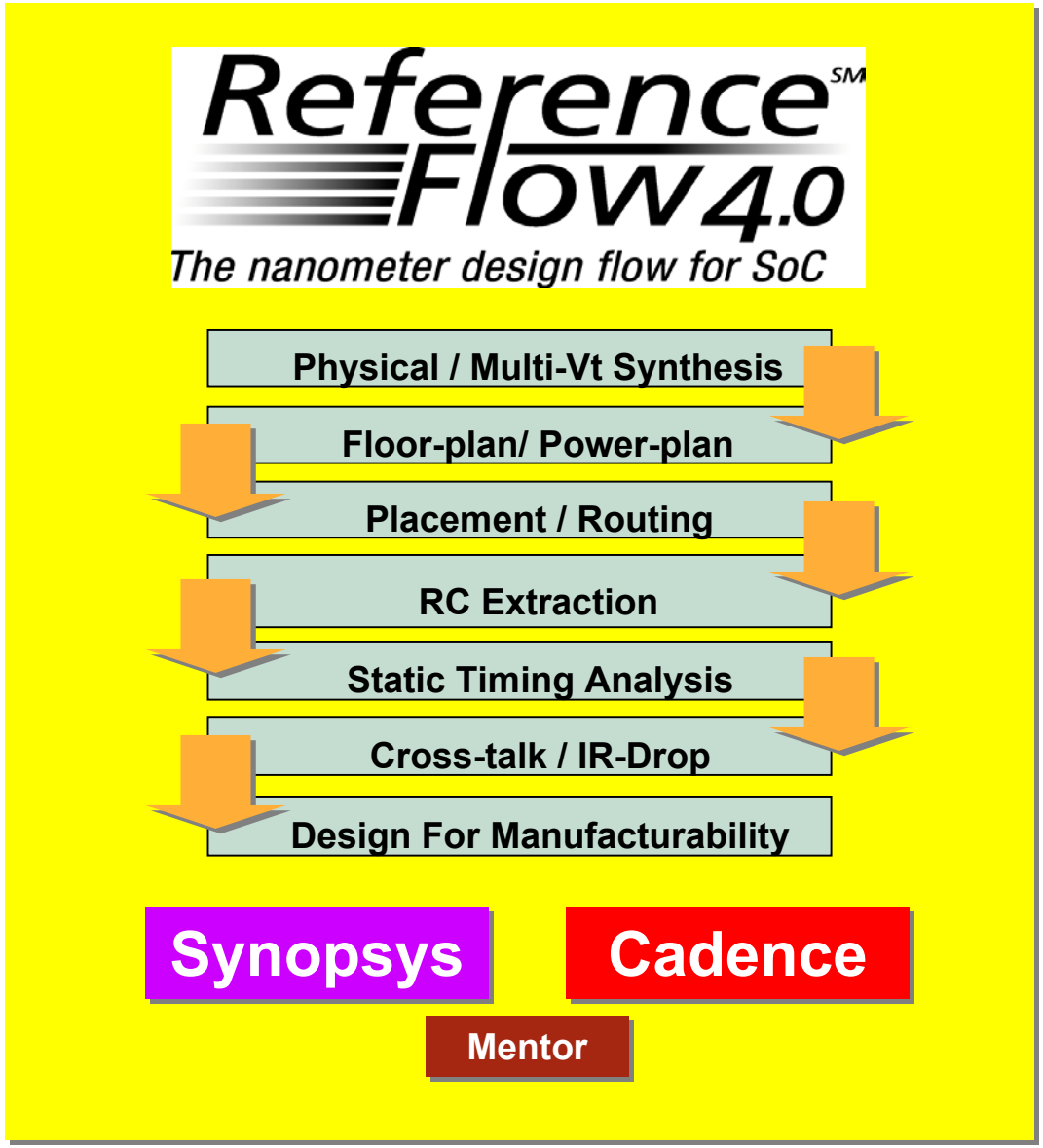
RCX

Always calibrated to silicon

Substrate

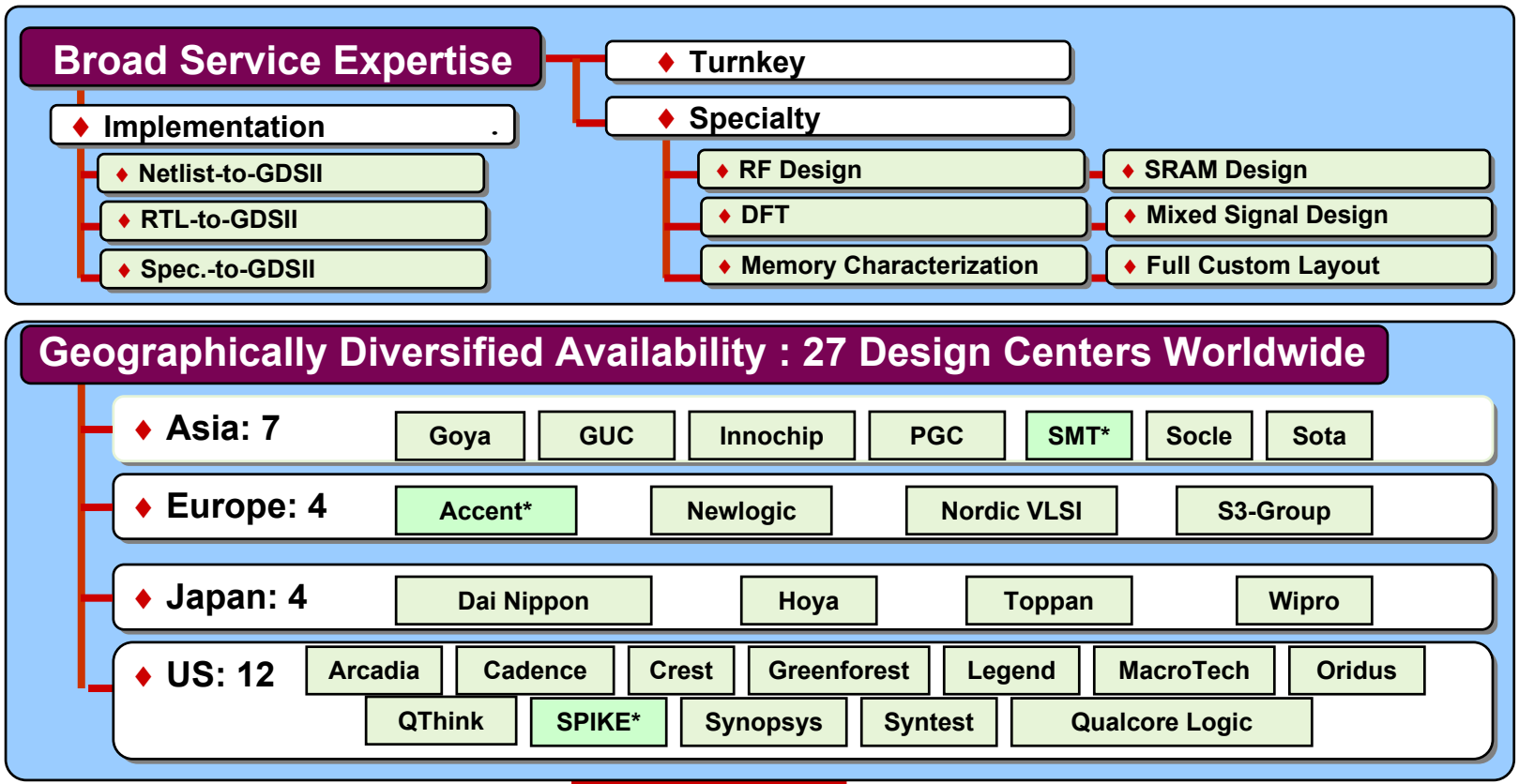
Advanced noise analysis for RF design

cadence SYNOPSYS Mentor Graphics SEQUENCE Agilent Technologies



Current Design Center Alliance

The Most Extensive Design Center Portfolio in Foundry Industry



Bring Multiple Choices to Customers !

** New additions*