TSMC Design Services:
Bringing Your Products to Market Faster
Intense Design Challenges

- Design Requirements
- Technology Constrains
- Efficiency of point tools
- Gap at Synthesis wireload & P&R
- Iteration at P&R
- Complexity
- Noise & EM
- IR & leakage

Technology Constrains:
- 0.25-micron
- 0.18-micron
- 0.15-micron
- 0.13-micron
- 90 nanometer
- 65 nanometer
What We Provide Besides Wafers

- Design Foundation Data
- Design Methodology
- Design Assistance
- Designer's Creativity
Enabling Time to Volume

- Methodology & Assistance (TSMC & 3rd Party)
- Designer
- Foundation Data (TSMC)

- 0.18-micron
- 0.15-micron
- 0.13-micron
- 90 nanometer
- 65 nanometer
Extensive Portfolio of Alliances

- **Foundation:** EDA Alliance
  - Design Rule related: DRC, LVS
  - Spice Model related: Spice, RCX

- **Methodology:** EDA Alliance
  - Digital Reference Flow
    - Four generations of quality delivery
  - RF/MS Design Kit
    - Foundry industry’s first and broadest node coverage

- **Design Assistance:**
  - TSMC Implementation Service
  - 3rd-Party Implementation Service
  - Silicon Debug and Repair Service
Foundation Data Quality

- **Device Modeling**
  - Version strategy
    - V0.0x, V0.x – guess model, R&D model
    - V1.x, V2.x – silicon model and production
  - Accuracy
    - Silicon correlation
    - Corner models (-40° ~ 125°)
  - Improved MOSFET Modeling
    - Vt Modeling
    - Gate current modeling
    - STI stress effect modeling
    - Gate capacitance modeling
    - Diode leakage current modeling

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SPICE Model

**Error Percentage (%)**

**Number of Nets**

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Foundation Data Quality

- **DRC, LVS**
  - Early Availability
    - In-house development synchronizes release with DRM
  - High Quality
    - Double-blind QA ensures industry-leading quality
  - Extensive Portfolio
    - Broad support of widely used tools
Foundation Data Quality

Interconnect Model
- Realistic Corner Model
  - Reflects combination of multi-layer statistical corners
- Performs silicon correlation with commercial tools
- RC Accuracy enhancement
  - Model with metal-thickness
  - 90 nanometer enabled

PMOS Core W/L=10/1.2 Vgs=0.41V, Vds=1V

Sid (A^2/Hz)

PMOS Core W/L=10/1.2 Vgs=0.5V, Vds=1V

Sid (A^2/Hz)

PMOS Core W/L=10/1.2 Vgs=0.31V, Vds=1V

Sid (A^2/Hz)
Designer’s Creativity

Design Assistance

Design Methodology

Design Foundation Data
Industry’s Most Comprehensive Flow

- Four consecutive quality deliveries
- Each release addresses new design challenges
- All releases are backward compatible

Efficiency of point tools

Gap at Synthesis wireload & P&R

Timing Driven Flow

Iteration at P&R

Timing Closure Flow

Complexity

Xtalk, IR & EM

SI Closure Flow

Hierarchical Flow

Timing Closure Flow

Reference Flow 4.0

The nanometer design flow for 30C

Release 3.0
Dual-Track Reference Flow

- Expands customer support through multiple major vendors coverage
- Responds to customers’ feedback

Note: TSMC Customer Base Coverage (physical implementation)
Multi-Vt Solution for Power Optimization

Commercial Flow
- RTL
- Physical Synthesis
- Physical Optimization
- Routing
- RC Extraction
- SI Analysis
- STA
- DRC/LVS

Higher Speed
- RTL
- Physical Synthesis
- Physical Optimization
- Routing
- RC Extraction
- SI Analysis
- STA
- DRC/LVS
- Low Vt Library
- Nominal Vt Library
- High Vt Library

Lower Leakage
- RTL
- Physical Synthesis
- Physical Optimization
- Routing
- RC Extraction
- SI Analysis
- STA
- DRC/LVS
- Gate-level Netlist
- Cell Swapping
- Layout Replacement
- DRC/LVS
- GDS

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## Power/Speed Optimization Example

- **Design Case:** ARM RISC Processor
- **Technology:** TSMC 90 nanometer

<table>
<thead>
<tr>
<th>Case</th>
<th>Power (mA)</th>
<th>Frequency (MHz)</th>
<th>Cell Distribution</th>
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<tbody>
<tr>
<td></td>
<td>Leakage</td>
<td>Dynamic</td>
<td></td>
</tr>
<tr>
<td>LVT</td>
<td>21.6</td>
<td>123.8</td>
<td>360</td>
</tr>
<tr>
<td>NVT</td>
<td>3.6</td>
<td>92.9</td>
<td>280</td>
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<tr>
<td>HVT</td>
<td>1.3</td>
<td>90.7</td>
<td>200</td>
</tr>
<tr>
<td>N/L VT</td>
<td>10.5</td>
<td>106.2</td>
<td>360</td>
</tr>
<tr>
<td>H/N/L VT</td>
<td>9.7</td>
<td>105.5</td>
<td>360</td>
</tr>
<tr>
<td>H/N VT</td>
<td>2.2</td>
<td>91.5</td>
<td>280</td>
</tr>
</tbody>
</table>
SI and Timing Closure
(Prevention, Analysis and Repair)

SI Analysis
- Well correlated RC Extraction considering In-die Process Variation.
- Accurate SI Analysis.

SI-Driven Prevention
Dramatically Reduce the SI Violations

SI-Driven Repair
Quickly Achieve SI and Timing Closure

Placement
Optimization
Routing
RC Extraction
IR Drop Analysis
Crosstalk Analysis
STA

Violation?
Yes

Physical Verification

Optimized Netlist

Dramatically Reduce the SI Violations
Demonstration of SI and Timing Closure

- TSMC 0.13-micron technology
- Two million-gate design

<table>
<thead>
<tr>
<th></th>
<th>Number of glitch violations</th>
<th>Number of timing violations</th>
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<tbody>
<tr>
<td>1st Iteration</td>
<td>1437</td>
<td>622</td>
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<tr>
<td>2nd Iteration</td>
<td>116</td>
<td>112</td>
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<tr>
<td>3rd Iteration</td>
<td>18</td>
<td>40</td>
</tr>
<tr>
<td>Final Clean-up</td>
<td>0</td>
<td>0</td>
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</table>

- Achieve both SI and timing closure with Reference Flow 4.0
DFM (Design for More?)

- How can a chip fail? How to avoid failures?
  - During design implementation (DFA – Design for Accuracy)
    - Design Spec
      - Functional error (Logic – function verification)
      - Electrical error (Timing, power – timing closure, power analysis)
    - Silicon technology spec
      - Physical error (rule -- DRC check)
      - Circuit error (silicon model, SPICE simulation)
  - During manufacturing (DFM – Design for Manufacturability)
    - Mask/OPC induced
    - Process steps induced
    - Material induced
  - During usage (DFR – Design for Reliability)
    - Time induced (electron-migration, wire-heating)
    - Situational signal induced (cross-talk delay and glitch)
    - Environment induced (temperature, shock)
Design for Accuracy

DFA (increase accuracy; bring out best performance)

- Length of Defusion (LOD)
  - STI stress effect
  - Function of length
  - BSIM3 & BSIM4 support
  - ADS, Eldo, Hspice, Spectre

- Metal thickness/width modeling
  - RC accuracy
  - Corner model

- IR Drop
  - Capacitance calculation
  - De-coupling cell insertion

- Cross-talk
  - Delay, noise or glitches
  - SI design closure
    - Prevention
    - Analysis
    - Repair
DFM (Design for Manufacturability)

- **Mask induced**
  - Lithography effects
    - Layer density rule

- **Process steps induced**
  - CMP effect
    - Metal thickness variation modeling
    - Metal density rule
  - Charge zap effect
    - Antenna rule

- **Material induced**
  - STI effect LOD
    - LOD device modeling
  - Dielectric material
    - Maximize redundant VIA
  - Stack VIA effect
    - Stack height limit

---

**Analysis of Dummy Metal Impact on Delay**

Path Delay

<table>
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<tr>
<th>Width</th>
<th>0.20</th>
<th>0.40</th>
<th>0.60</th>
<th>1</th>
<th>2</th>
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<td>0.24</td>
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<td>0.19</td>
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<td>0.28</td>
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<td>0.42</td>
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<td>0.70</td>
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<td>0.46</td>
<td>0.46</td>
<td>0.46</td>
<td>0.46</td>
<td>0.46</td>
</tr>
</tbody>
</table>

Resistivity

| Thickness | Width
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<tbody>
<tr>
<td>0.005um</td>
<td>0.08um</td>
</tr>
<tr>
<td>0.010um</td>
<td>0.08um</td>
</tr>
<tr>
<td>0.015um</td>
<td>0.08um</td>
</tr>
<tr>
<td>0.020um</td>
<td>0.08um</td>
</tr>
</tbody>
</table>

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DFR (Design for Reliability)

- DFR (avoid failure in use; increase MTBF)

- Electro-migration
  - Power EM
    - Power mesh
    - Wire tapering
  - Signal EM
    - Multiple via insertion

- Cross-talk
  - Delay, noise or glitches
  - SI design closure
    - Prevention
    - Analysis
    - Repair

- Hot electron
  - Safe IR control design practice

- Self-heating wire
  - Safe power/clock mesh design practice

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Flip-Chip Capability

- RDL Flow (available)
  - Silicon proven flow on several customer chips.

- Area Array Flow (under development)
  - Cluster approach using TSMC developed flip chip I/Os
  - Silicon validated on internal test chip
  - Fine tuned for new I/O cells (better structure)
PDK for High Quality MS/RF Designs

CM025
CM018
CM013*
SG035**
SG018**

Mixed Signal/RF Designers

Download & Support
(TSMC-Online)

* Currently posted with CL013
** Temporary posted at Cadence web site

Joint Development

For Mentor ADK contact Mentor

Design Rules
SPICE Models

P-cell Layout Generators
Physical Verification Files

SKILL Code
TSMC PDK Device List

Elements
- Active
  - MOS
- Passive
  - Resistor
  - Inductance
  - Capacitor
  - Varactor
- Supporting
  - EDS
  - RF Pad

Features
- 4-T model
  - MOS
- 3-T model
  - Resistor
  - Capacitor
  - Inductance
- Noise model
  - Thermal
  - Flicker
- Statistical model
  - Corner
  - Matching

Methodology
- Monte-Carlo
TSMC In-house Implementation Service

- **Design & EDA Expertise**
  - Birth place of TSMC reference flows
  - In-house library, I/O & IP development
  - Pioneering tape out of advanced technologies

- **Silicon Expertise**
  - Device characterization
  - Silicon correlation

- **Full Service Expertise**
  - Turn-key service
  - Key customer driven
  - Product engineering
Industry’s Largest Design Center Alliance

28 Worldwide Partners
Over 400 Tapeouts in 2002

The Applications You Want
- Computer
- Consumer
- Communication

The Services You Require
- Platform-based Design
- RTL-to-GDSII
- Netlist-to-GDSII
- Memory Characterization
- DFT Service
- RF Design
- Full Custom Layout
- Mixed Signal Design
- SRAM Design

The Business Models You Prefer
- NRE-based Outsourcing Service
- Turnkey/ASIC Service
- T&M-based Consulting Service

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DCA Success Story - Consumer
Ideally suited to video and image encoding and decoding applications that are reliant on a low power, low cost integrated processing solution. Applications include:

- Wireless Video Phones
- Camera Accessory Modules
- Wireless PDAs
- Wireless PC/ Network Cameras

"We chose QThink because our project team found that they offered a solid solution with a flexible interface that would allow customization of some areas of the design. They were one of the few that had true 0.13µm tape-out experience along with strong skills in the generation and integration of custom macros, and that gave us good confidence that the project would be successful."

Richard Bériault
Director of Engineering
Atsana Semiconductor

- FIRST-PASS SILICON SUCCESS!
- TECHNOLOGY: 0.13 µm CMOS process, 100 MHz operating frequency
- APPLICATION: Array Processor for parallel operations, ARM922T™ for host and high-level instructions
- PACKAGE: 180 pin CABGA
- POWER: 1.2V Core and 2.5/3.3 V I/Os, Multiple Power Modes
“Philips Semiconductors selected Cadence Design Foundry to join Philips existing design capability in a design partnership to implement the pnx8526 product.

The combined efforts of both teams resulted in an essentially first silicon success product that met the end customer’s aggressive production IC availability requirements”

Wout Bijker
Vice-President, Business Line Broadband Home Servers
Philips Semiconductors

- 5 Million Gates
- 778Kbits of Sram (232 instances)
- 0.13 um TSMC (1P8M + RDL)
- 158MHz core clock speed, 56 domains
- 150MHz Processor, 200MHz DSP
- Complex Analog functions.
- 8.6mm x 8.2mm
- 367 I/Os and Power
- Wirebond, BGA
- Power consumption 2.6W

First Silicon Success®
IC Validation Alliance – Bridging The Gap Between Prototype & Volume

Customer

Design & Implementation

TSMC

Prototype Manufacturing

First-pass Silicon Success

YES

NO

Design rework

Volume Production

Validation Alliance

90nm CAD

90nm LSM** Image

Waveform Measurements

Through Silicon FIB Repair to M2

* FIB: Focused Ion Beam
** LSM : Laser Scanning Microscope
IC Validation - Business Model & Program Snap Shot

- The business model you need from npTest
  - Guaranteed localization of failure; no service charge if failure is not localized
  - Project based pricing; remove the time and materials risk

- 28 IC validation projects completed in the program’s first 14 months

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.13 µm</th>
<th>0.18 µm</th>
<th>0.25 µm</th>
<th>0.35 µm</th>
</tr>
</thead>
<tbody>
<tr>
<td># of Projects</td>
<td>13</td>
<td>13</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

- 8 more projects underway
- Covering computer, consumer and communication applications
Summary

**Time-to-Design Start**
- High quality, highly consistent foundation data
- DRC, LVS, RCX, SPICE

**Time-to-Tapeout**
- Robust and state-of-the-art methodology support
- Four generations of Reference Flow
- Expanded PDK for RF/MS design needs
- Most comprehensive 3rd-party and in-house design services portfolio

**Time-to-Volume**
- Flexible service business models
- Safety net provided through Validation Service
TSMC Design Services: Bringing Your Products to Market Faster
Reference
A Complete Design Service Package

**Reference Flows**
- Cadence, Synopsys
- Mentor, Syntest

**Mixed-Sig /RF Design Kits**
- Cadence PDK
- Mentor ADK
- In progress
- Upon request

**RCX**
- Cadence Assura
- Fire&Cice(QX)
- HyperExtract
- Nautilus
- Mentor xCalibre
- Sequence Columbus
- Synopsys Arcadia
- Raphael NES
- Star RC(XT)

**DRC**
- Cadence Assura
- Diva
- Dracula
- Mentor Calibre
- Synopsys Hercules

**LVS**
- Cadence Assura
- Diva
- Dracula
- Mentor Calibre
- Synopsys Hercules

**Spice**
- Agilent ADS
- Cadence Spectre
- Mentor Eldo
- Synopsys H-Spice

**Application Notes**
- Usage Guideline etc.

**Substrate**
- Cadence Substrate-Storm

*In progress**  **Upon request**

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## EDA Alliance

*World Leading Design Foundation and Design Methodology*

### Methodology

<table>
<thead>
<tr>
<th>Reference Flow</th>
<th>Analog Design Kit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual implementation tracks Enabling direct manufacturability into TSMC’s advanced technologies</td>
<td>Off-the-shelf productivity from industry-leading analog tools</td>
</tr>
</tbody>
</table>

### Foundation

<table>
<thead>
<tr>
<th>DRC</th>
<th>LVS</th>
<th>SPICE</th>
<th>RCX</th>
<th>Substrate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Double-blind Quality Assurance</td>
<td>Matches device (spice), layers (design rule) and application notes</td>
<td>Industry leading models</td>
<td>Always calibrated to silicon</td>
<td>Advanced noise analysis for RF design</td>
</tr>
</tbody>
</table>

### Supporting Tools

- Cadence
- Synopsys
- Mentor Graphics
- SEQUENCE
- Agilent Technologies
Physical / Multi-Vt Synthesis
Floor-plan/ Power-plan
Placement / Routing
RC Extraction
Static Timing Analysis
Cross-talk / IR-Drop
Design For Manufacturability

Synopsys    Cadence

Mentor
**Current Design Center Alliance**

The Most Extensive Design Center Portfolio in Foundry Industry

### Geographically Diversified Availability: 27 Design Centers Worldwide

- **Asia:** 7
  - Goya
  - GUC
  - Innochip
  - PGC
  - SMT*
  - Socle
  - Sota
- **Europe:** 4
  - Accent*
  - Newlogic
  - Nordic VLSI
  - S3-Group
- **Japan:** 4
  - Dai Nippon
  - Hoya
  - Toppan
  - Wipro
- **US:** 12
  - Arcadia
  - Cadence
  - Crest
  - Greenforest
  - Legend
  - MacroTech
  - Oridus
  - QThink
  - SPIKE*
  - Synopsys
  - Syntest
  - Qualcore Logic

### Broad Service Expertise

- **Implementation**
  - Netlist-to-GDSII
  - RTL-to-GDSII
  - Spec-to-GDSII
- **Turnkey**
- **Specialty**
  - RF Design
  - DFT
  - Memory Characterization
  - SRAM Design
  - Mixed Signal Design
  - Full Custom Layout

*New additions*

**Bring Multiple Choices to Customers!**