SOI Technology: Overview and Device Physics

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Outline

- ◊ Introduction (Where SOI Technology stands today)
- ◊ SOI Materials (SOS, SIMOX, Wafer Bonding, Unibond®)
- ◊ The "Classical" SOI MOSFET (Partially/Fully Depleted)
- ◊ Other SOI MOSFETs (Hybrid, Double Gate, Ground Plane, multiple gates)
- ◊ SOI Circuits (Hi-T°, Low-Power, RAMs)

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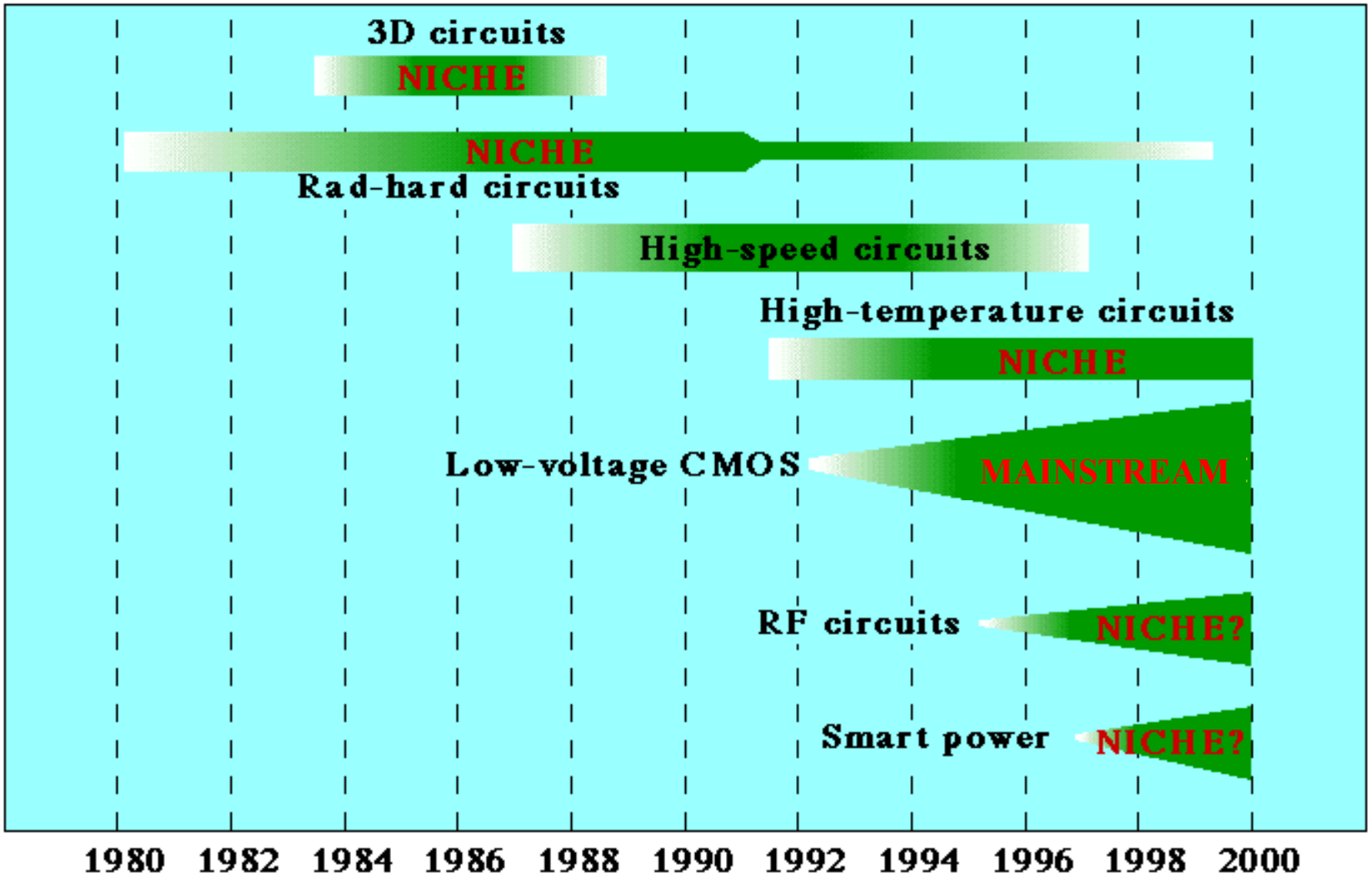
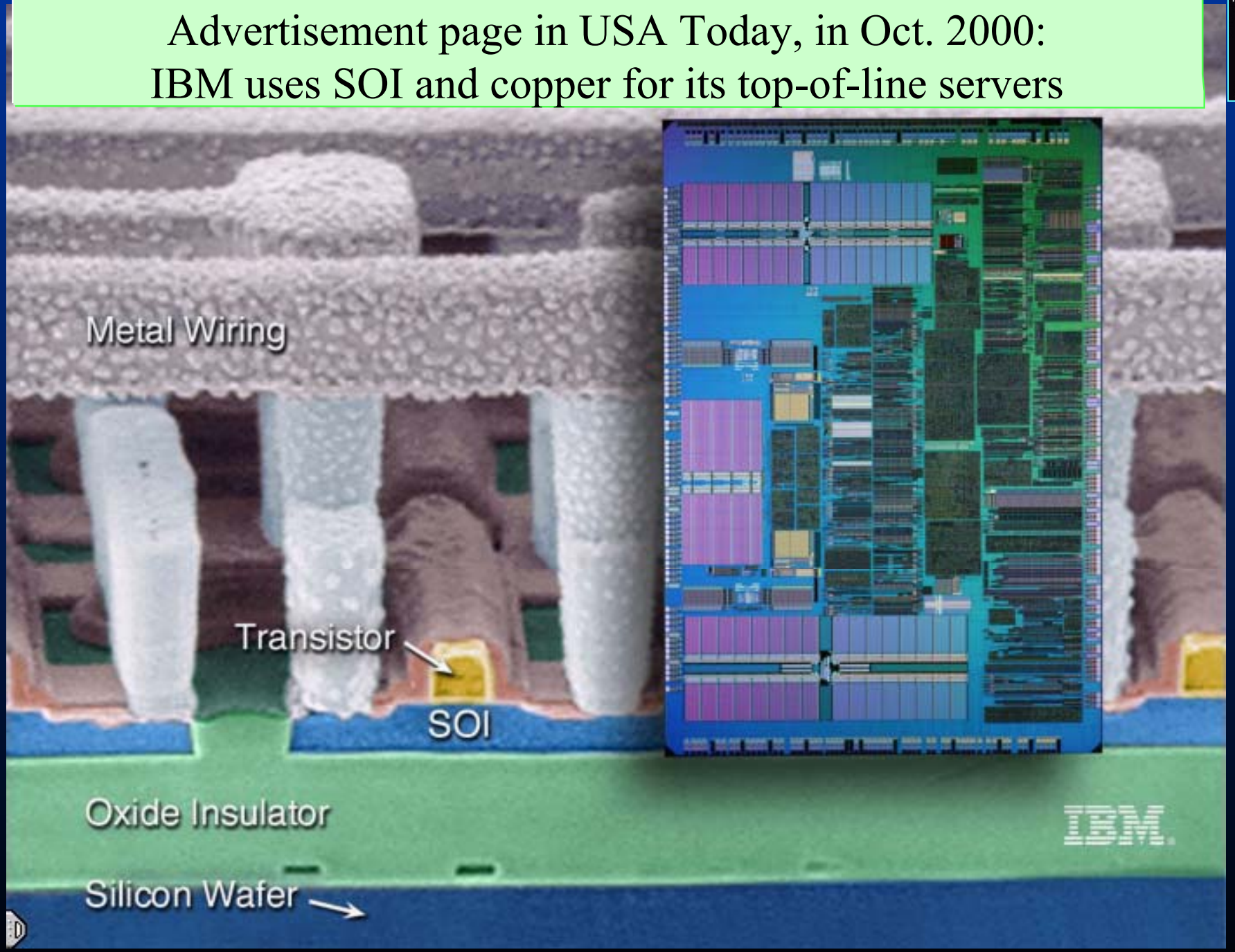

3D circuits
NICHE
NICHE
Rad-hard circuits
High-speed circuits
High-temperature circuits
NICHE
Low-voltage CMOS
MAINSTREAM
RF circuits
NICHE?
Smart power
NICHE?
1980
1982
1984
1986
1988
1990
1992
1994
1996
1998
2000

US Semiconductor Manufacturers Using SOI

IBM	PD	Microprocessor
Motorola	PD/FD	Microprocessor
AMD	PD/FD	Microprocessor
TI	PD	Various
HP	PD	Microprocessor
Peregrine	FD (SOS)	RF, logic, EEPROM analog, Rad-hard
Synova	PD	Rad-Hard
Honeywell	PD	Hi-T°; Rad-hard
Lincoln Lab	FD	Low-power, Rad-hard

SOI news web site: http://www.soisolutions.com

Advertisement page in USA Today, in Oct. 2000: IBM uses SOI and copper for its top-of-line servers

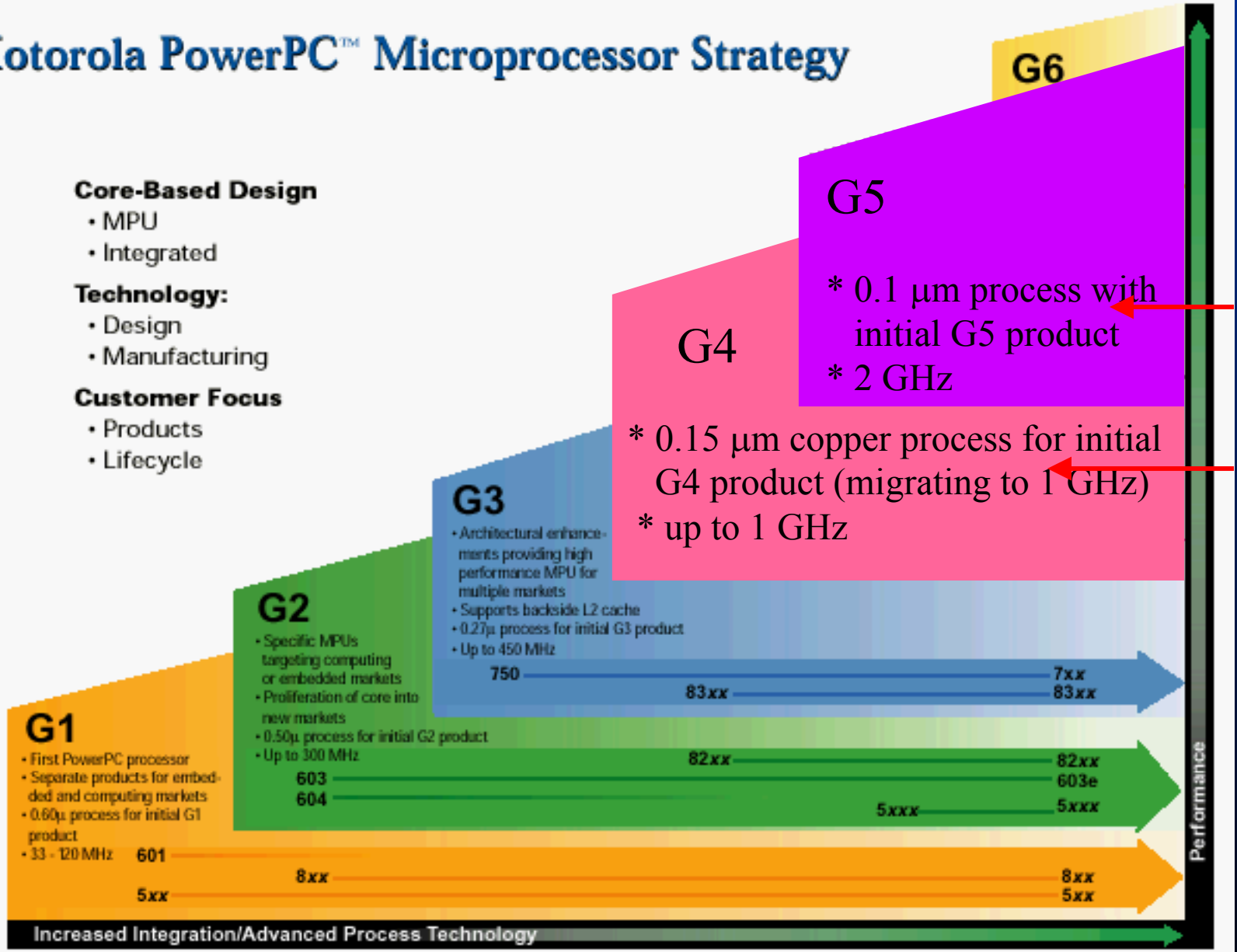


Motorola PowerPC™ Microprocessor Strategy

Core-Based Design
- MPU
- Integrated

Technology:
- Design
- Manufacturing

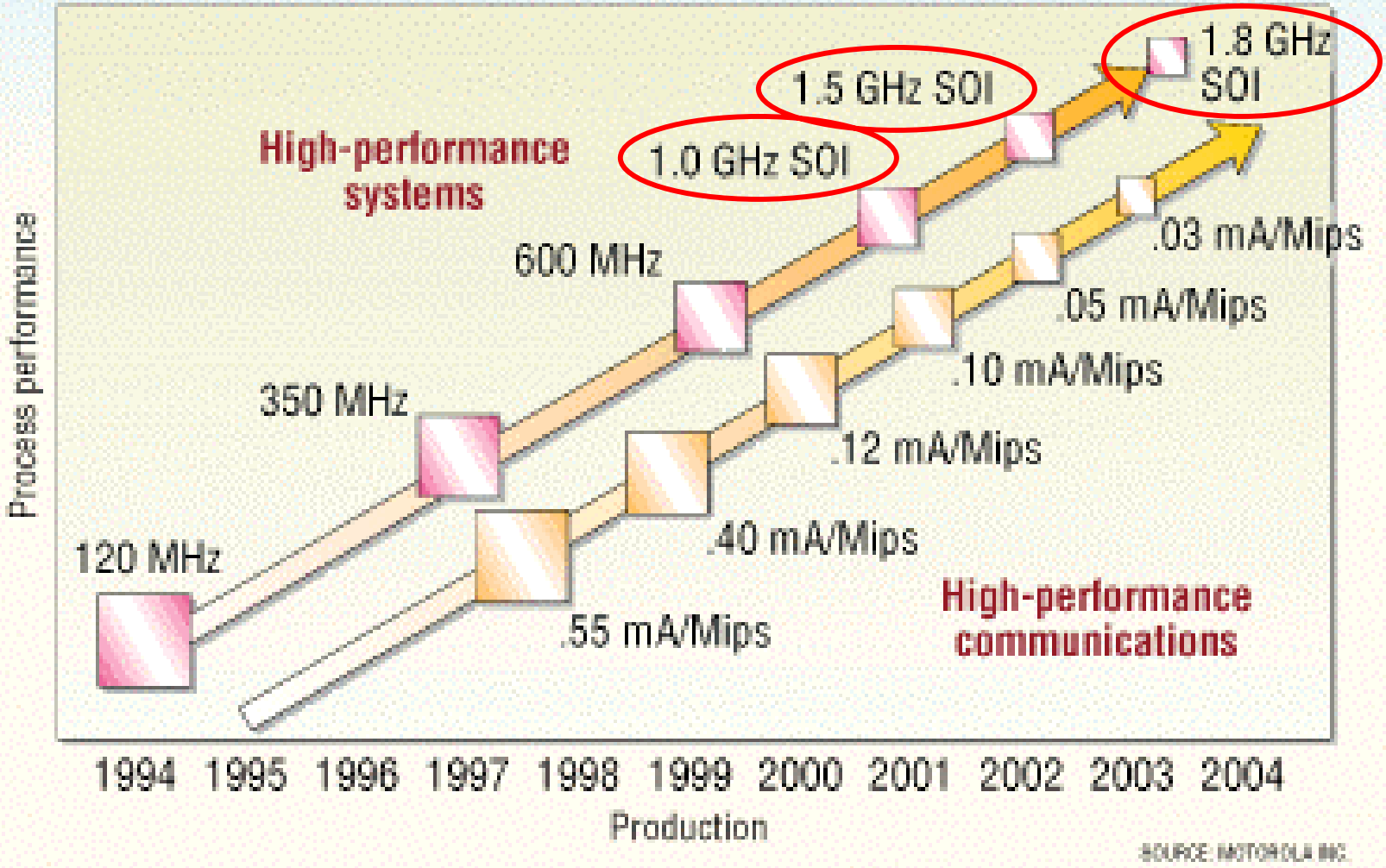
Customer Focus
- Products
- Lifecycle

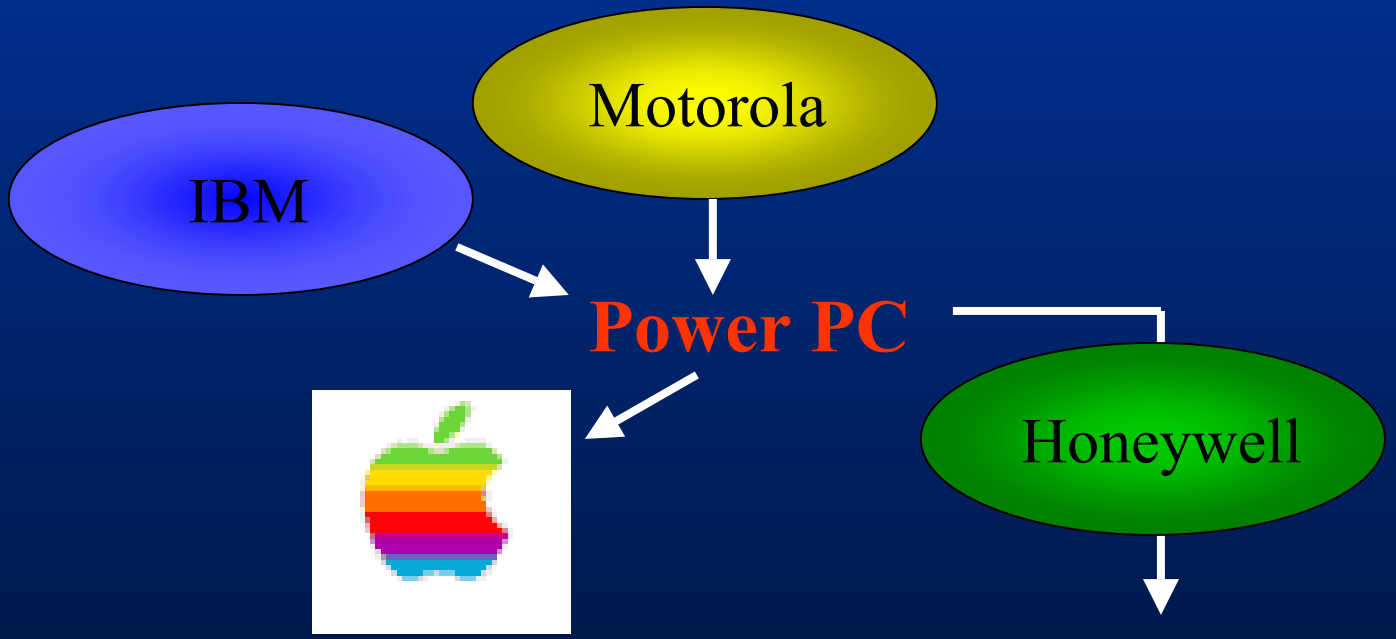


6xx, 7xx, 7xxx — high performance microprocessor targeting computing and high-end embedded
8xx, 8xxx — integrated processor targeting the Communications and Consumer markets
5xx, 5xxx — integrated processor targeting the Transportation market

MOTO SHIFTS TO SOI FOR HIGH PERFORMANCE

CMOS technology platform stresses power consumption





CLEARWATER, FLA. FEBRUARY 4, 1999 - Honeywell Space Systems and Motorola Semiconductor Products Sector today announced a joint licensing agreement for PowerPC* technology for use in Honeywell space processors. The result will be a next generation space microprocessor which will be radiation hardened to withstand the destructive effects of space, will operate with Power PC software and use less power.

Internally, Honeywell is referring to this next generation microprocessor as the Space Processor Chip (SpacePC). It combines the capabilities of the advanced Motorola PowerPC 603e microprocessor with Honeywell's radiation and performance enhancing Silicon On Insulator (SOI) technology.

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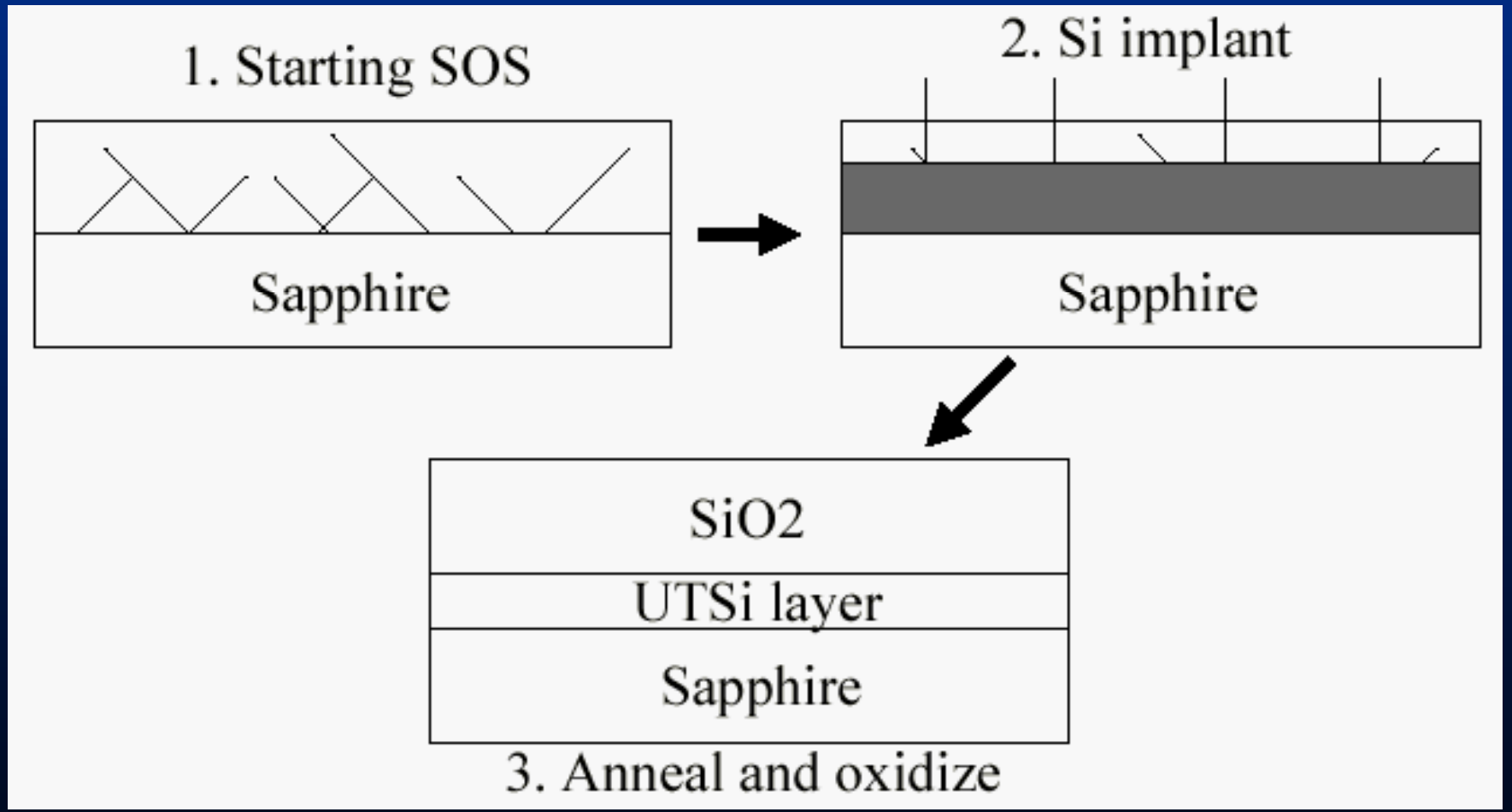
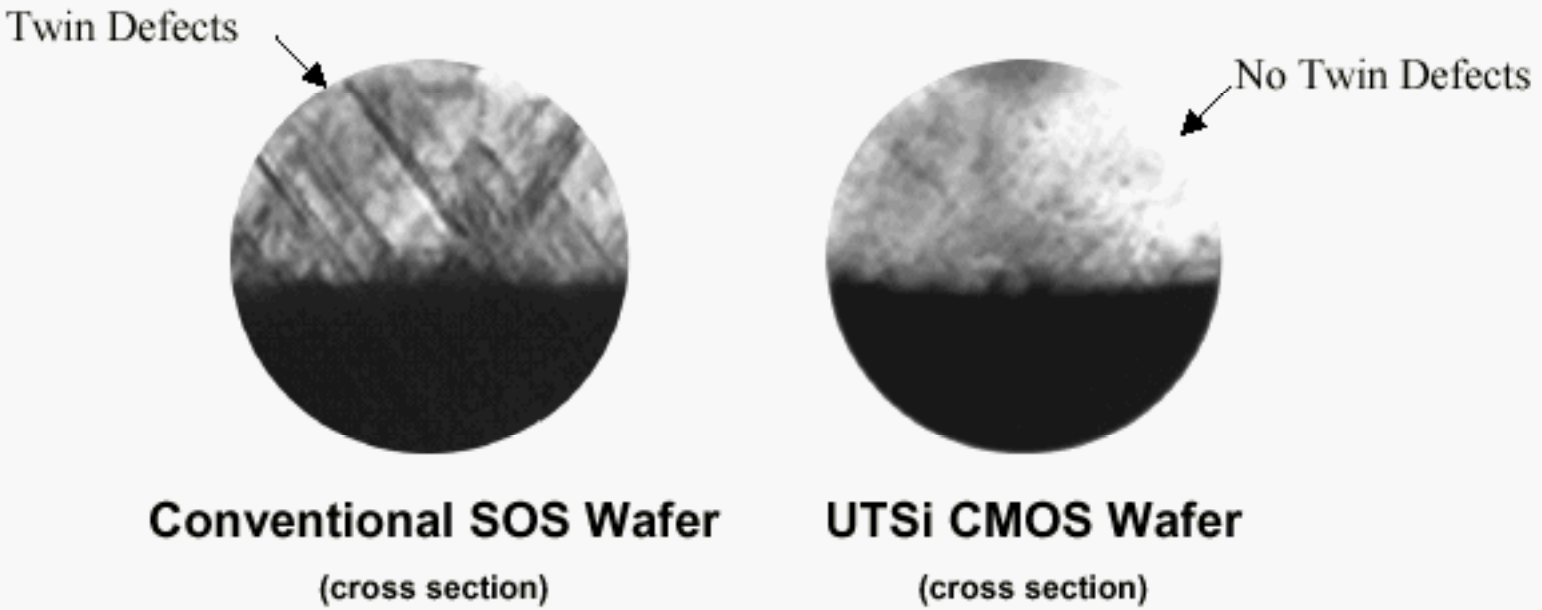
Silicon on Sapphire

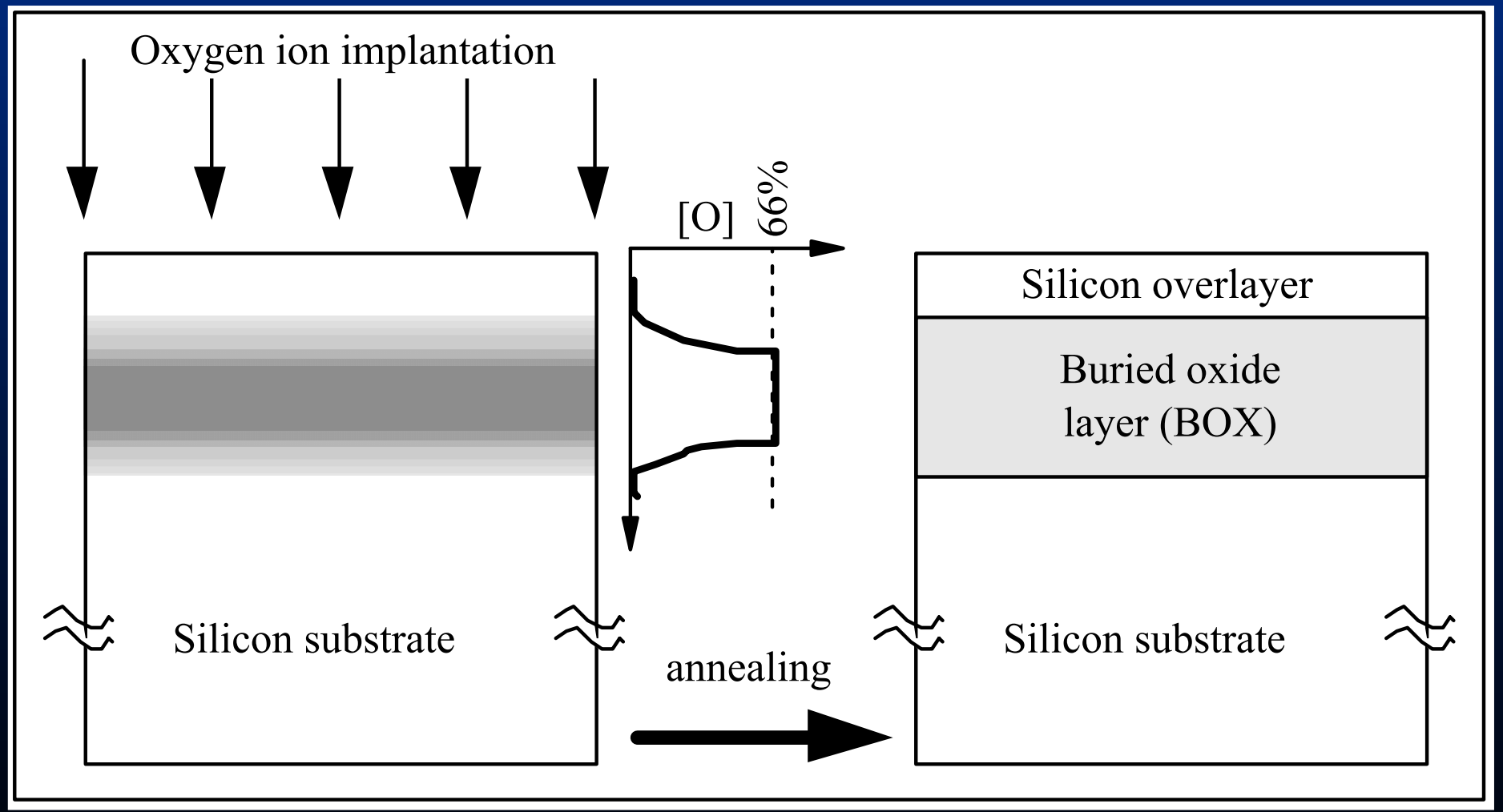


Silicon on Sapphire

Elimination of defects in silicon-on-sapphire process.

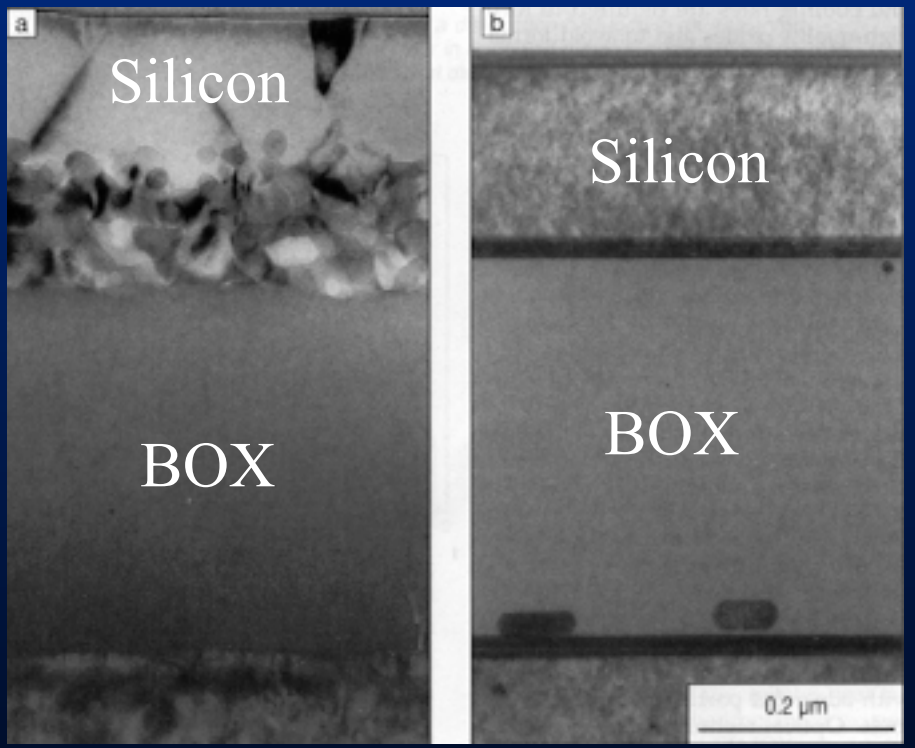


SIMOX


Oxygen ion implantation
[O]
66%
Silicon substrate
annealing
Silicon overlayer
Buried oxide
layer (BOX)
Silicon substrate

SIMOX

SIMOX, circa 1985

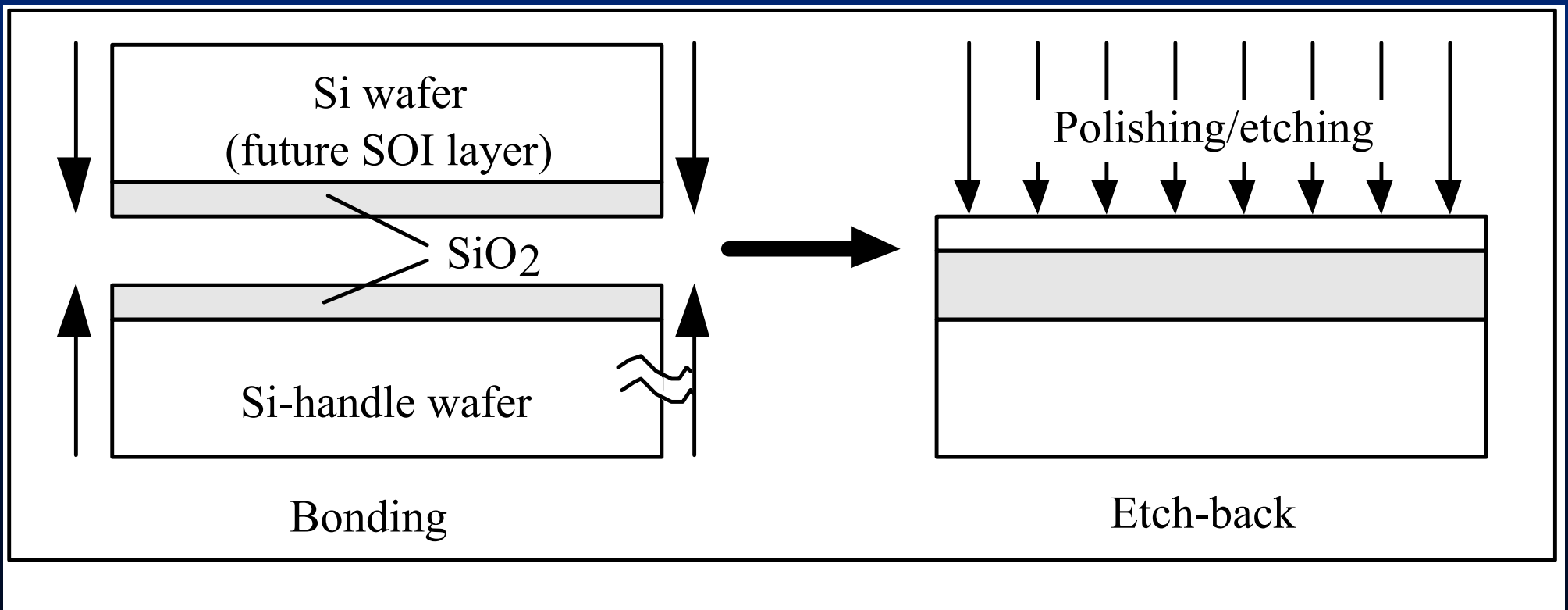


SIMOX, 1998

1,000,000,000 dislocations/cm²

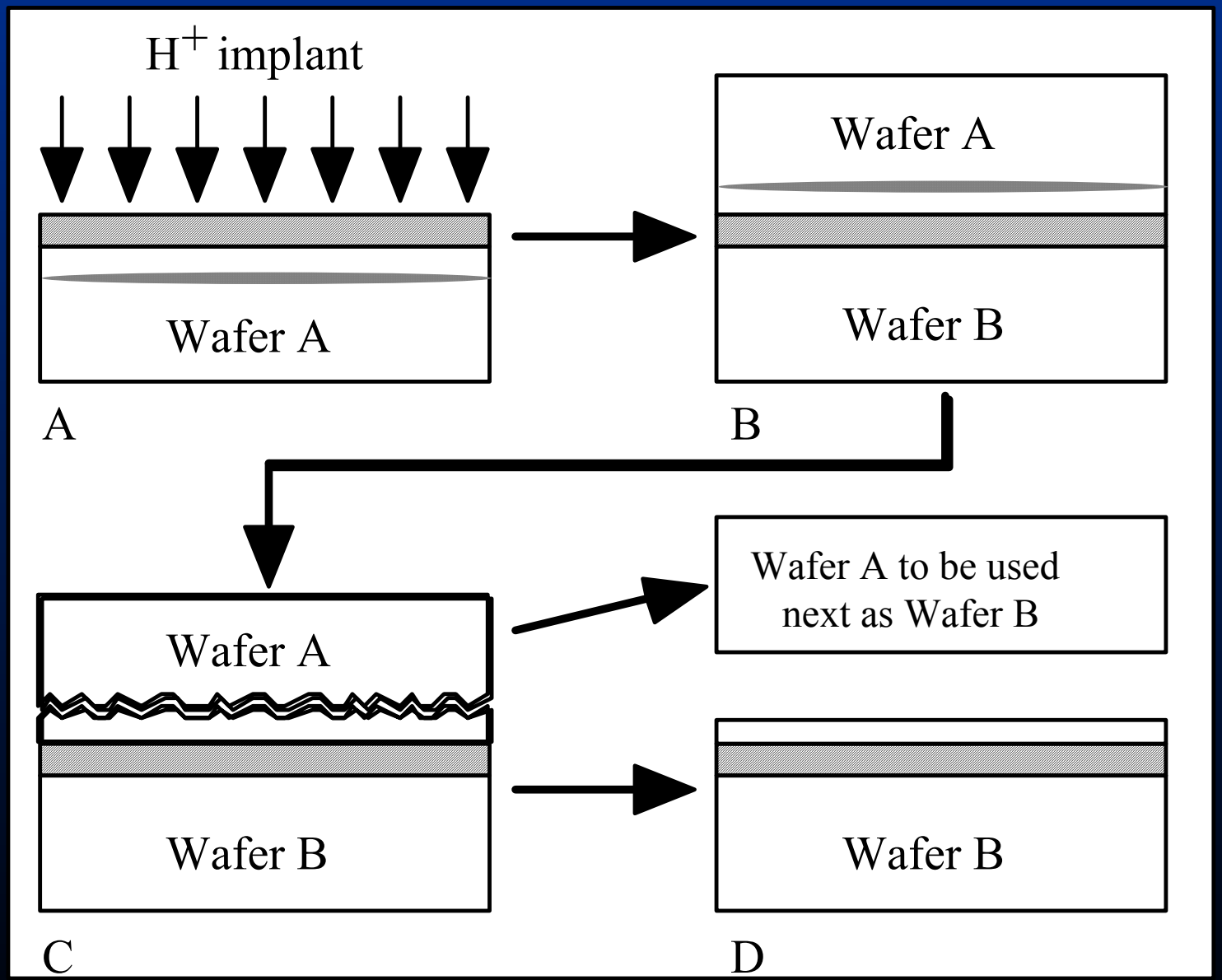
3,000 dislocations/cm²

Wafer Bonding and Etch Back



Wafer Bonding

Smart-Cut® / Unibond®



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(Partially/Fully Depleted)

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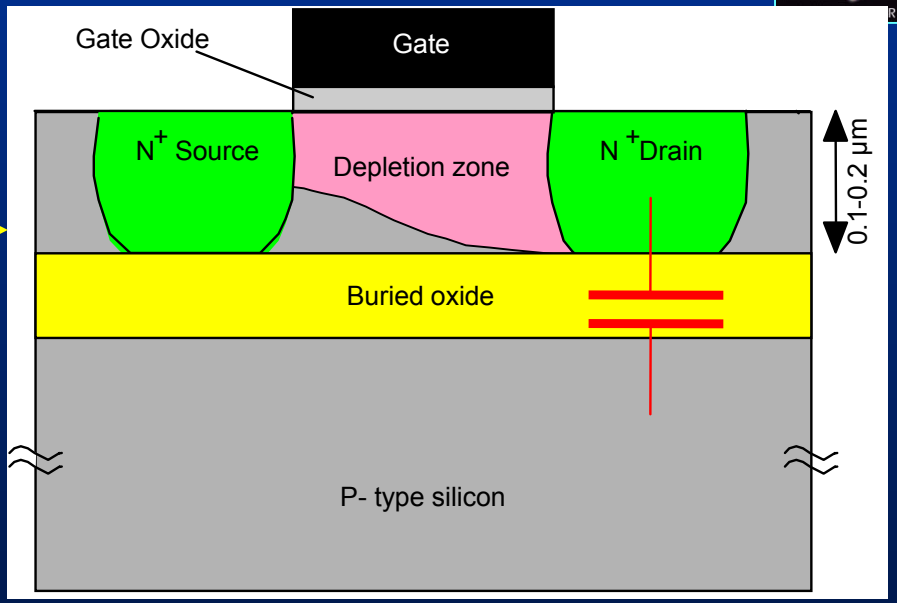
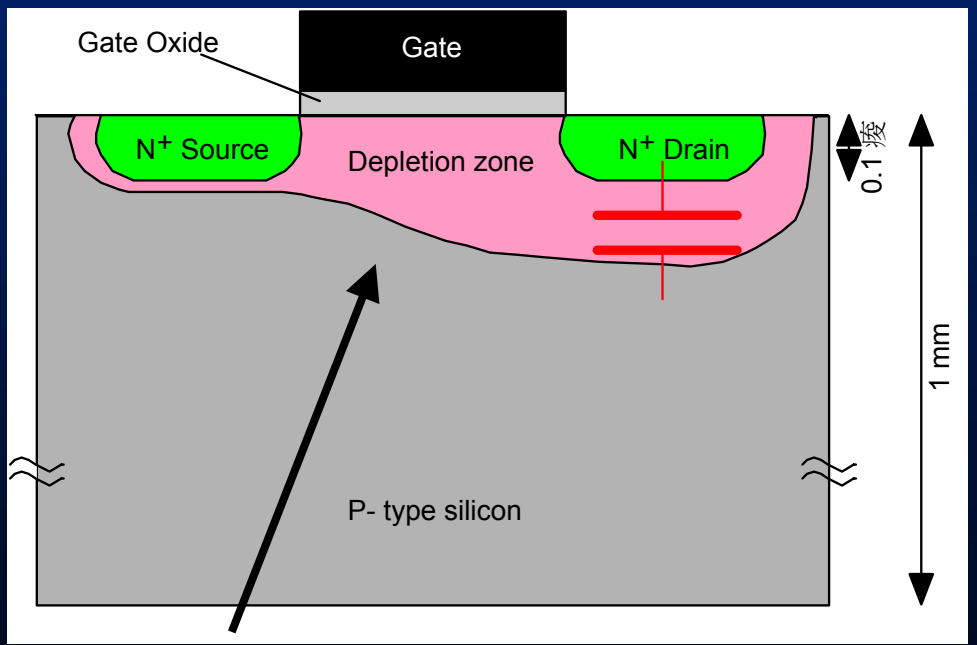
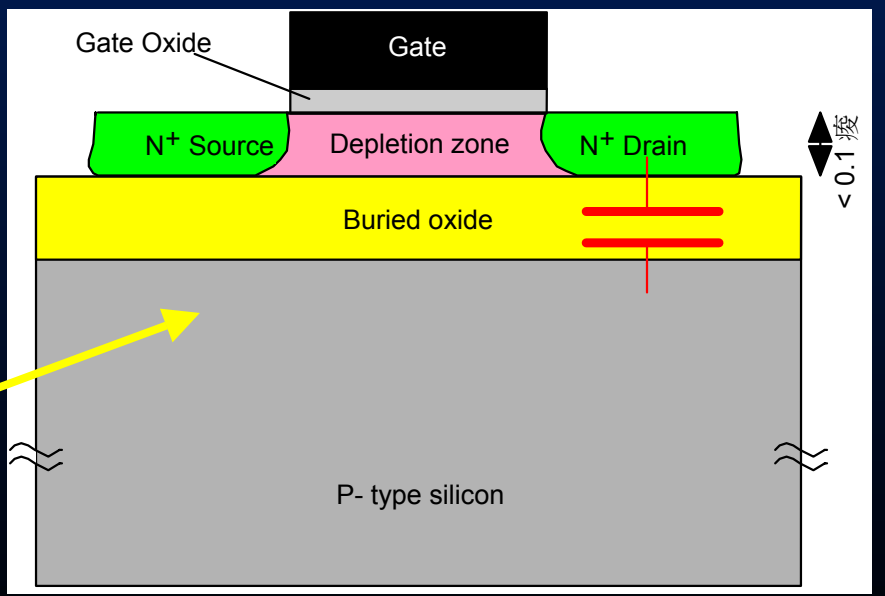
MOSFETs



Partially Depleted SOI

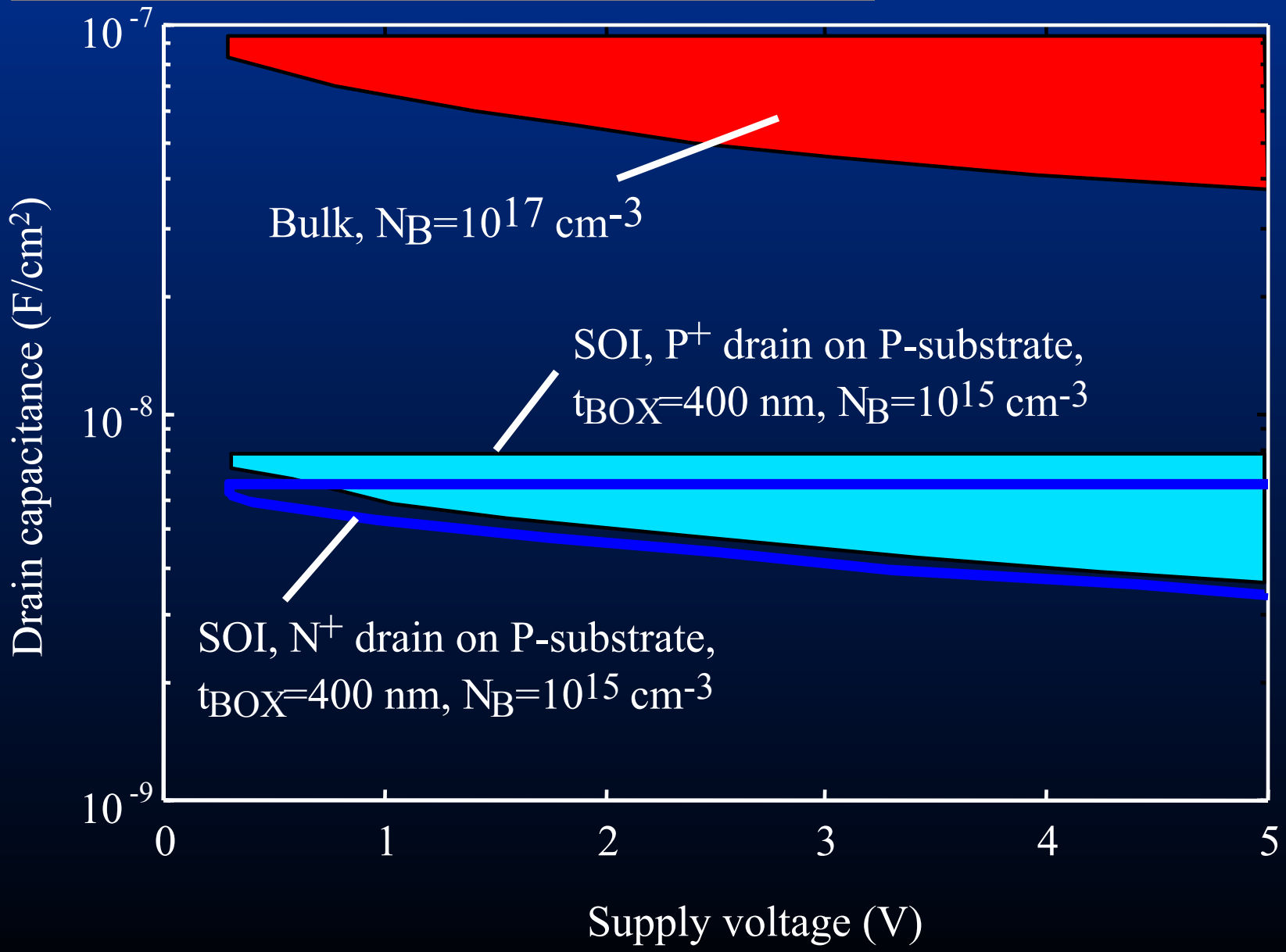


Bulk

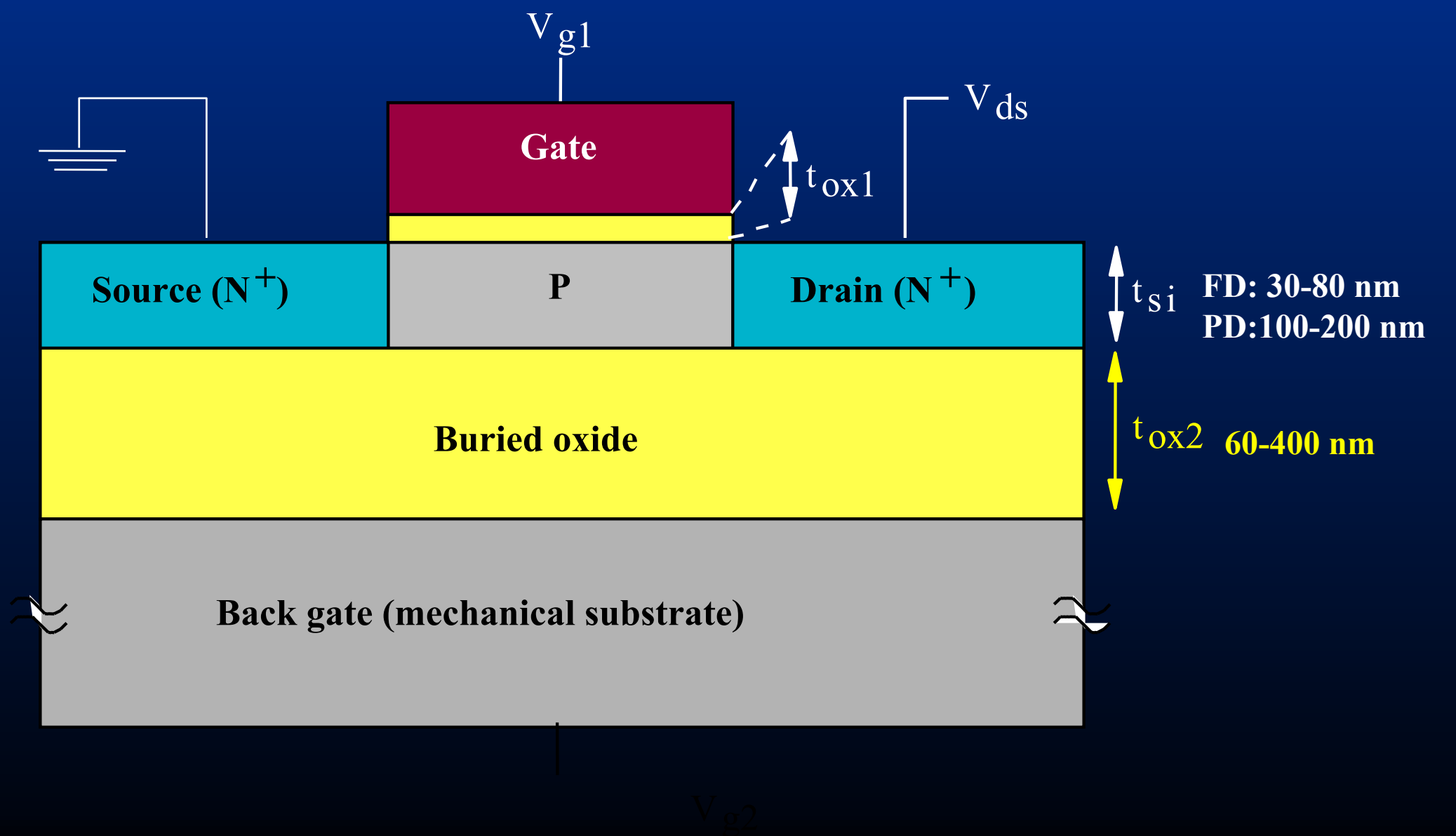


Fully Depleted SOI

Source and Drain Capacitance



SOI MOSFET: a few definitions



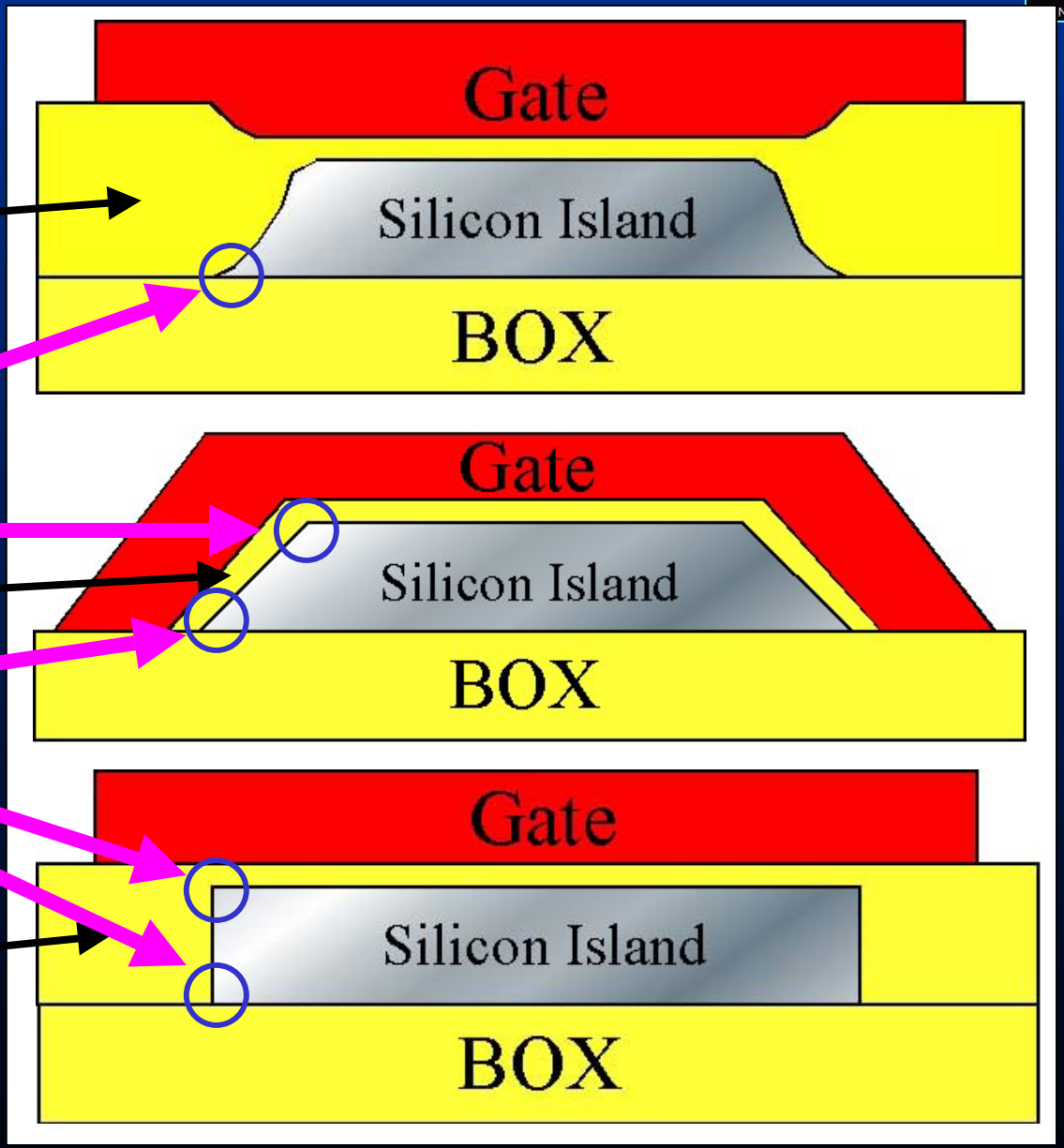
Field Isolation

LOCOS

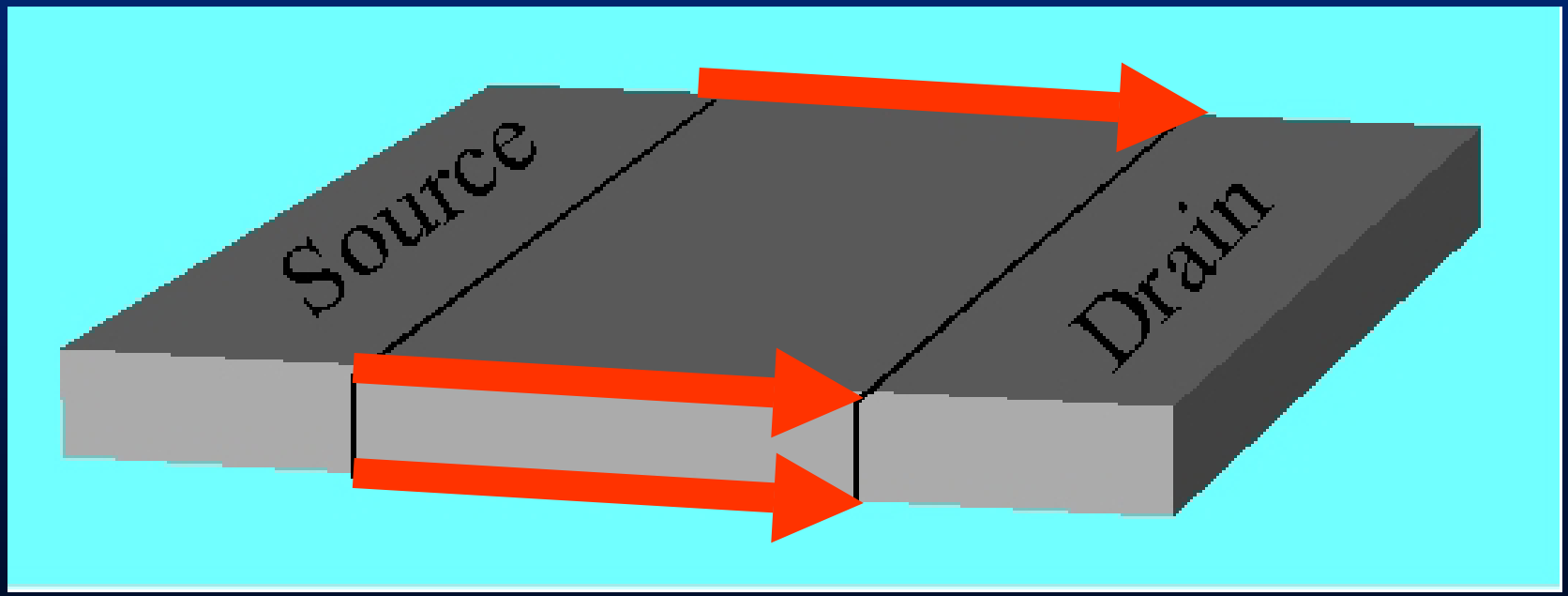
Possible Edge Leakage

Mesa

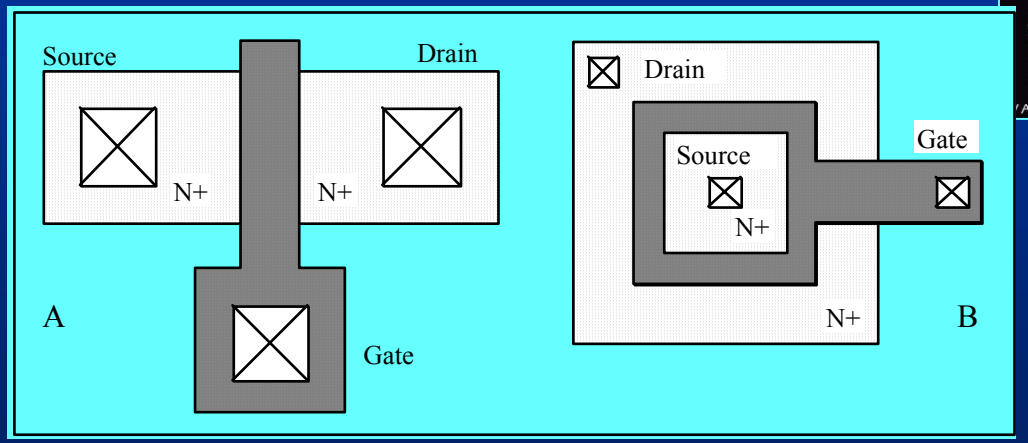
STI



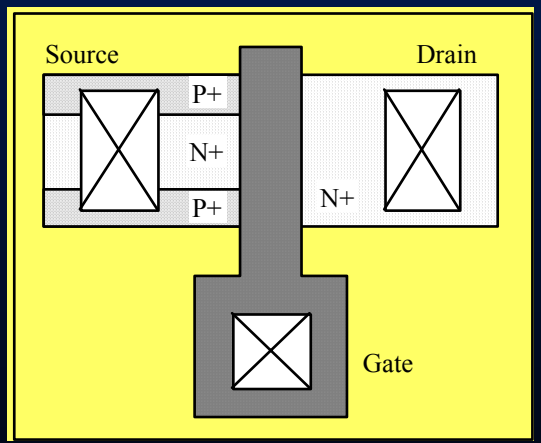
Edge Leakage



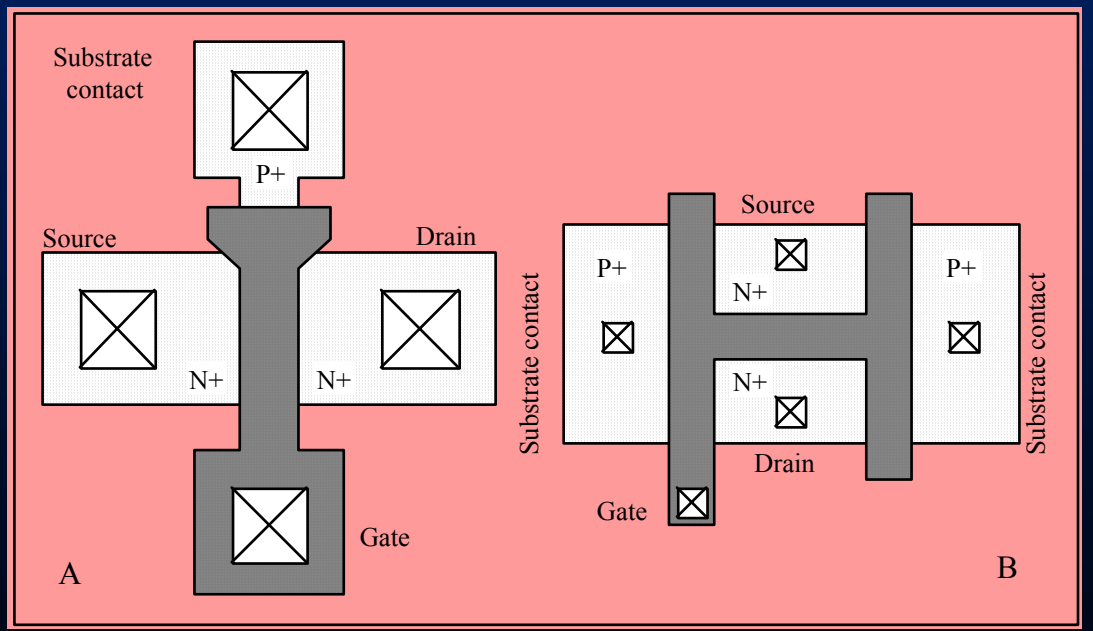
Edge Leakage Elimination And Body Ties



A: Regular SOI MOSFET; B: Edgeless device



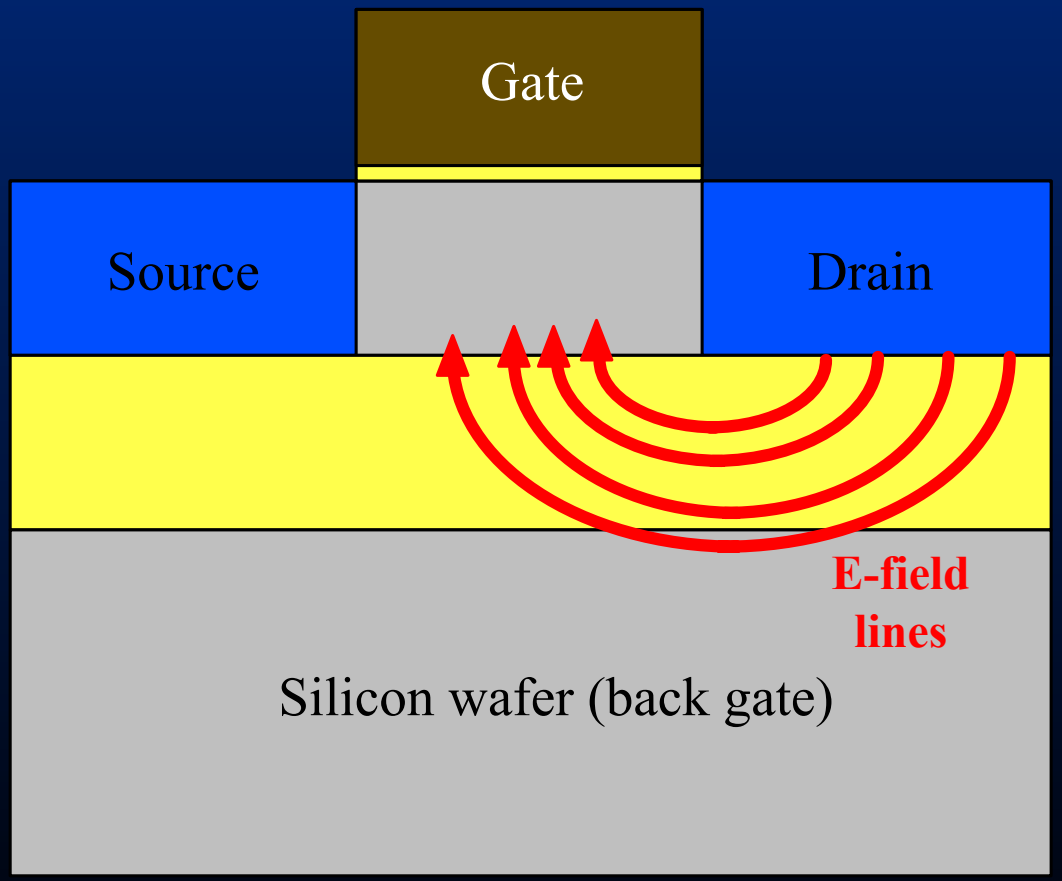
Body ties in source



A: Lateral body tie; B: H-gate body tie

SOI MOSFET: DIBL

or: Drain-Induced Barrier Lowering



Electric field lines from the drain encroach on the channel region. Any increase of drain voltage decreases the threshold voltage (the "NPN" potential barrier between source and drain is lowered).

SOI MOSFET

PDSOI MOSFET

Pro: better V_{TH} control
Con: floating substrate effects
Remedy: Body tie

OFFSPRING

Hybrid (DTMOS, MTCMOS)

FDSOI MOSFET

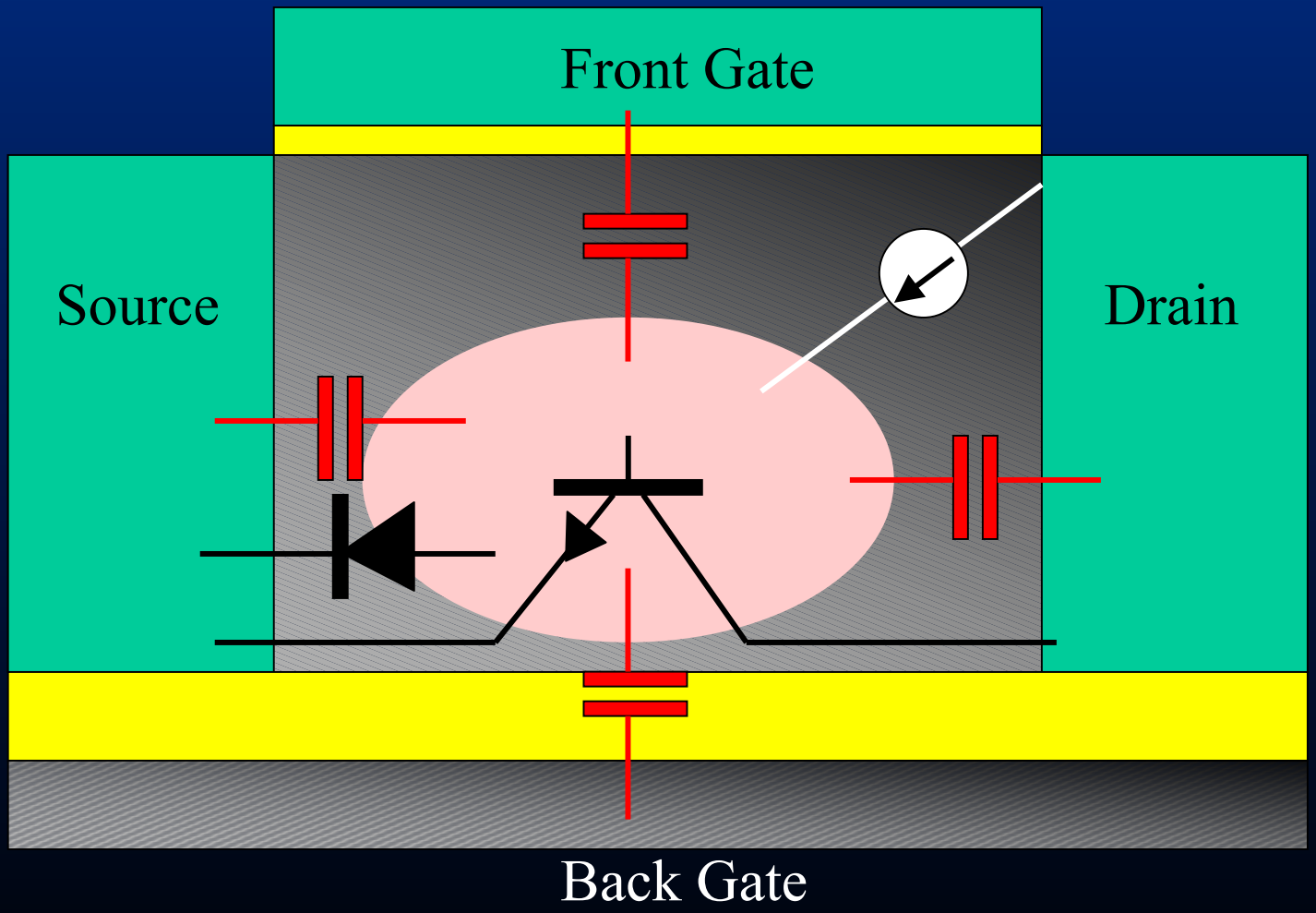
Pro: better electrical properties
Con: worse V_{TH} control*
Remedy: Uniform SOI material

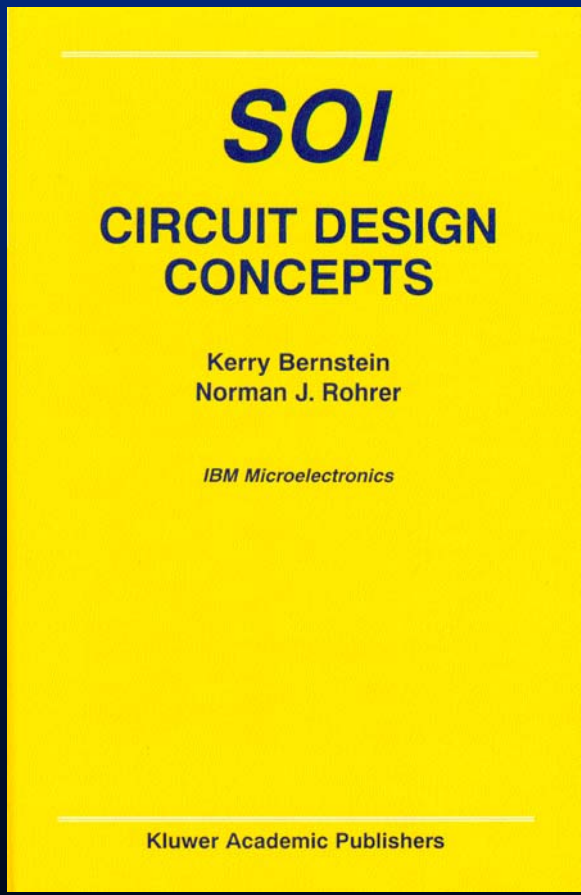
OFFSPRING

Double gate
Multiple gate
Buried ground plane electrode

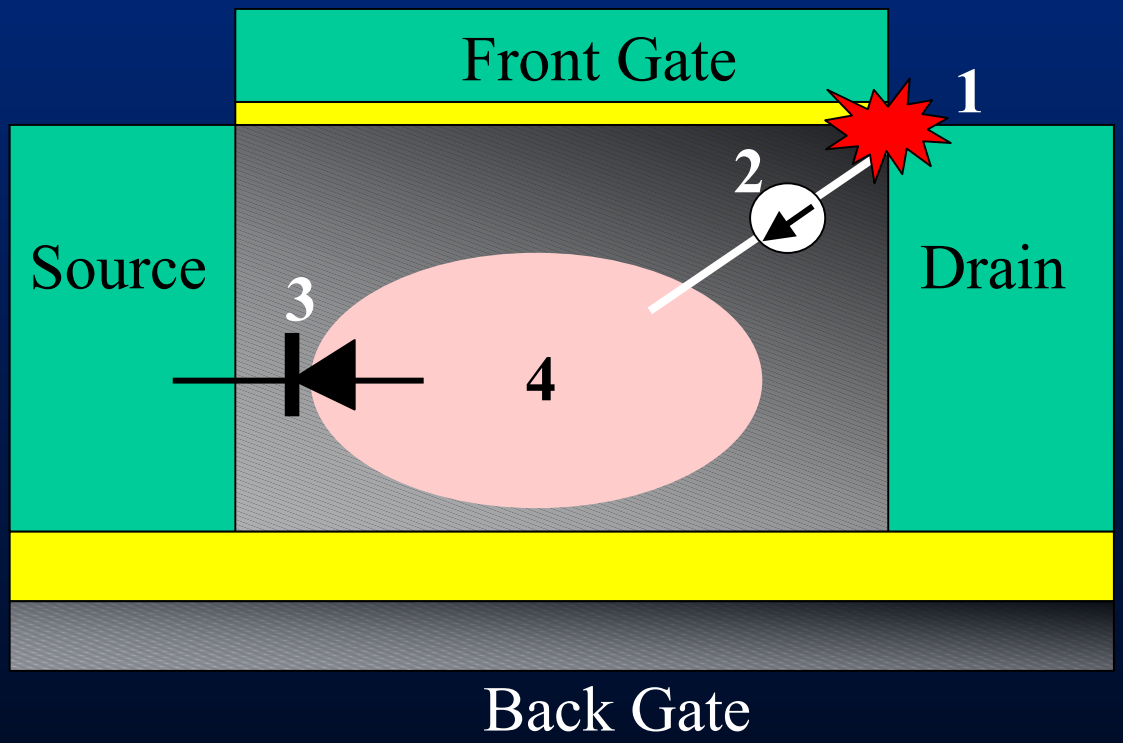
* $\sigma V_{TH} < 9$ mV in literature

PDSOI MOSFET



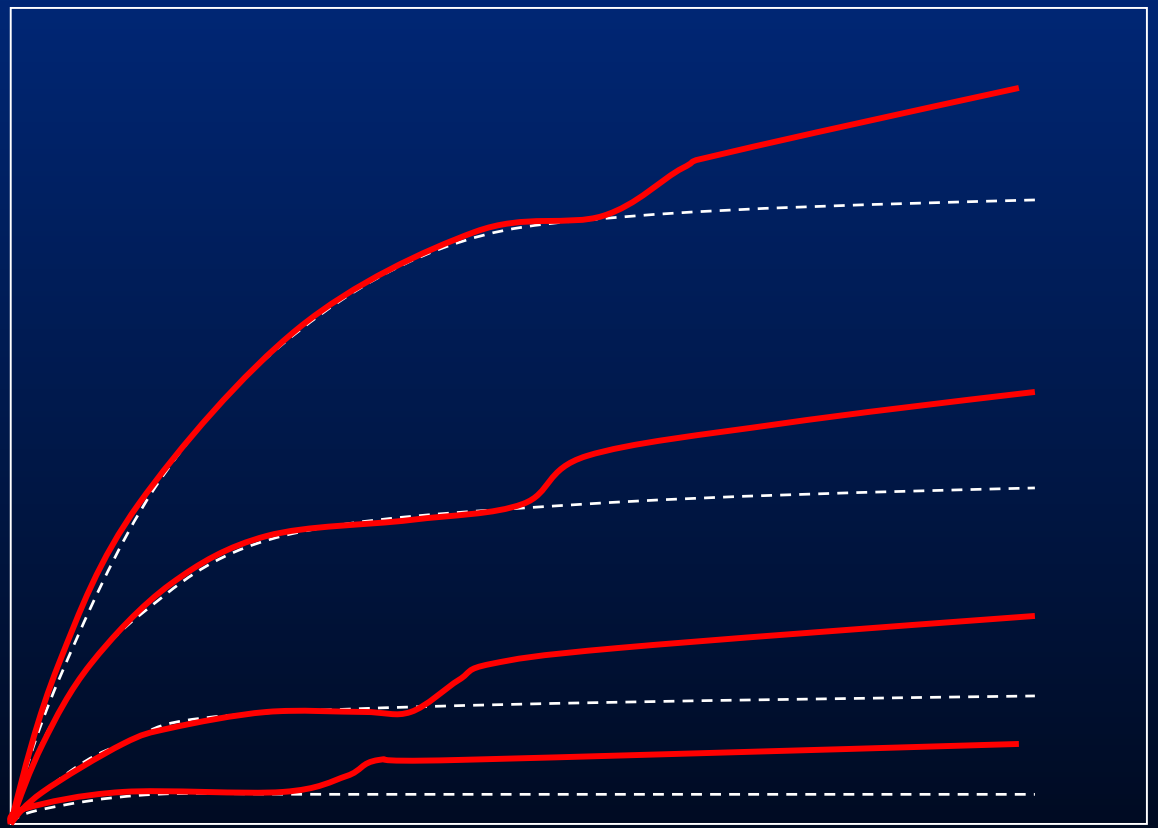


PDSOI MOSFET: Kink Effect



1. Impact ionization
2. Hole injection in floating substrate
3. Forward bias diode
4. Increase of floating body potential
5. Reduces V_{TH}
6. Increases current

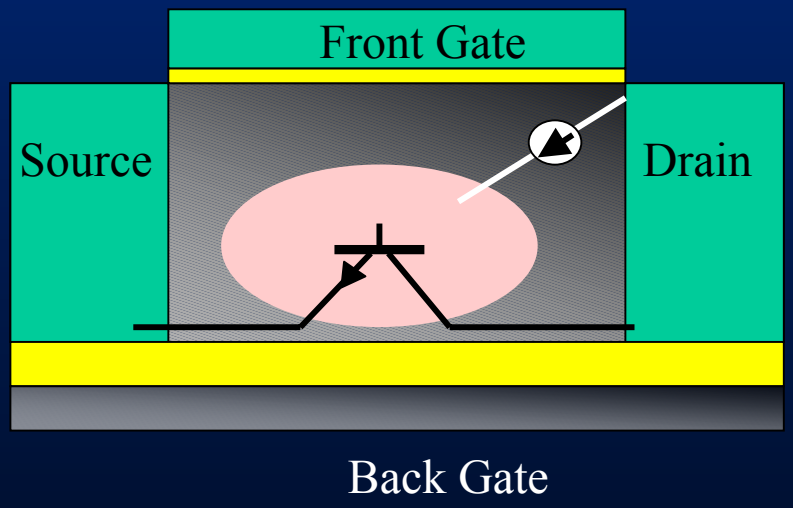
PDSOI MOSFET: Kink Effect



Current is increased (GOOD!)

Output conductance (or Early voltage) is very poor (BAD!)

SOI MOSFET: Single-Transistor Latchup



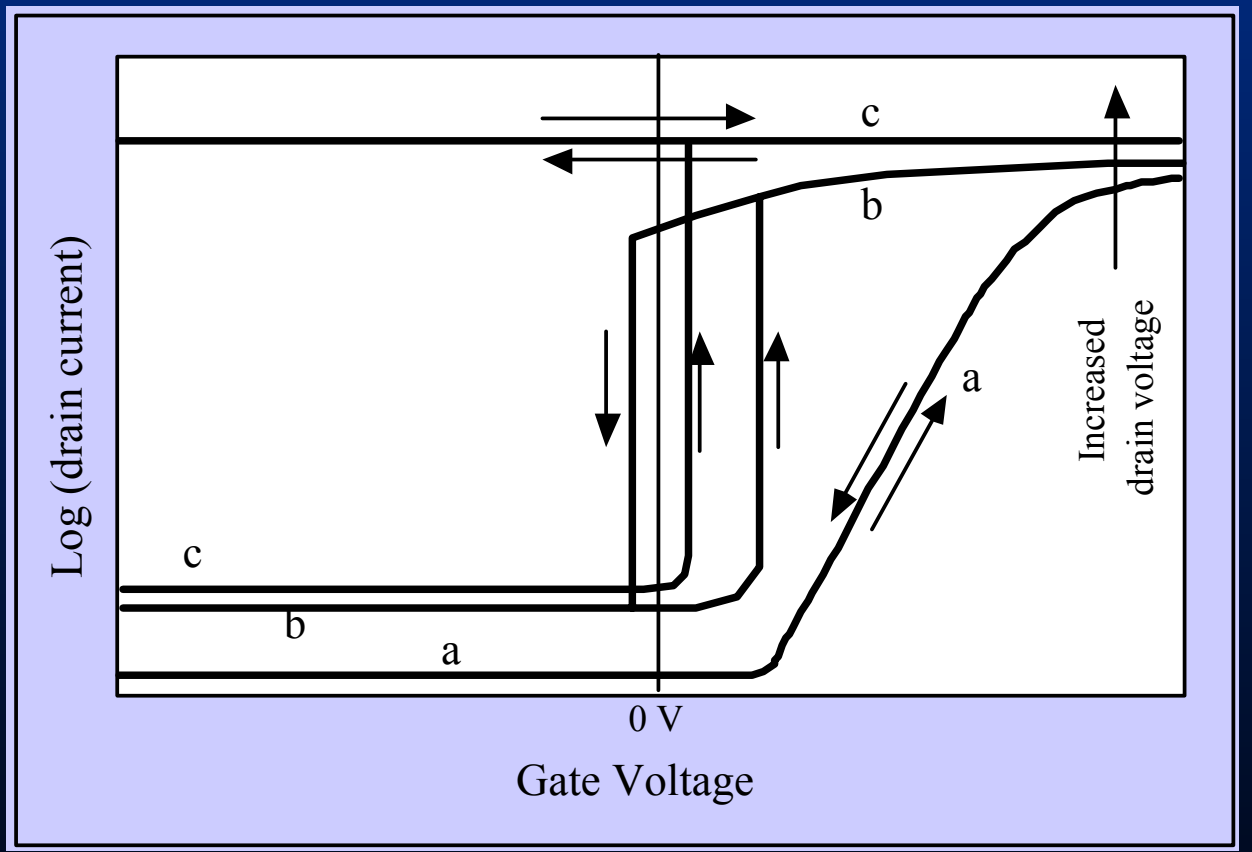
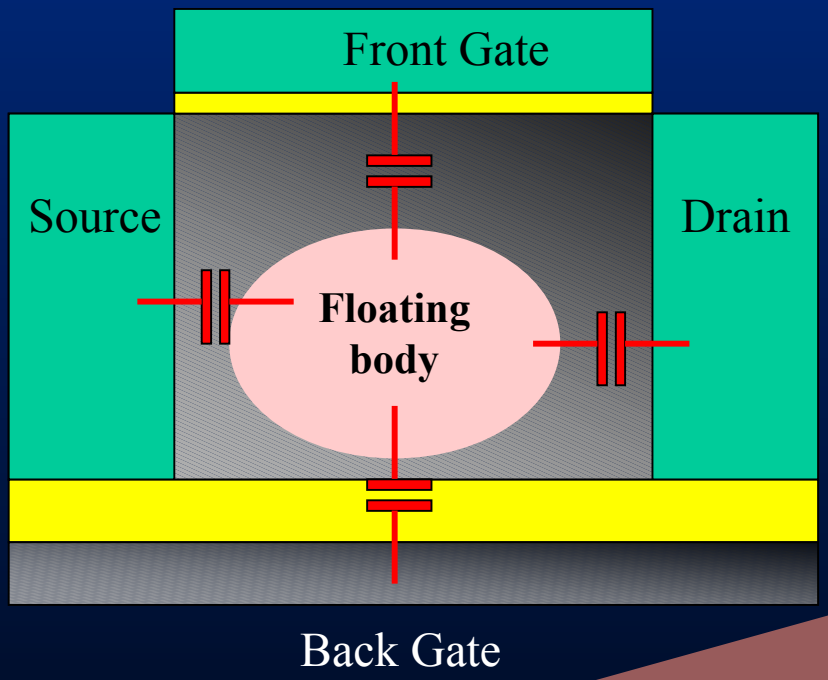
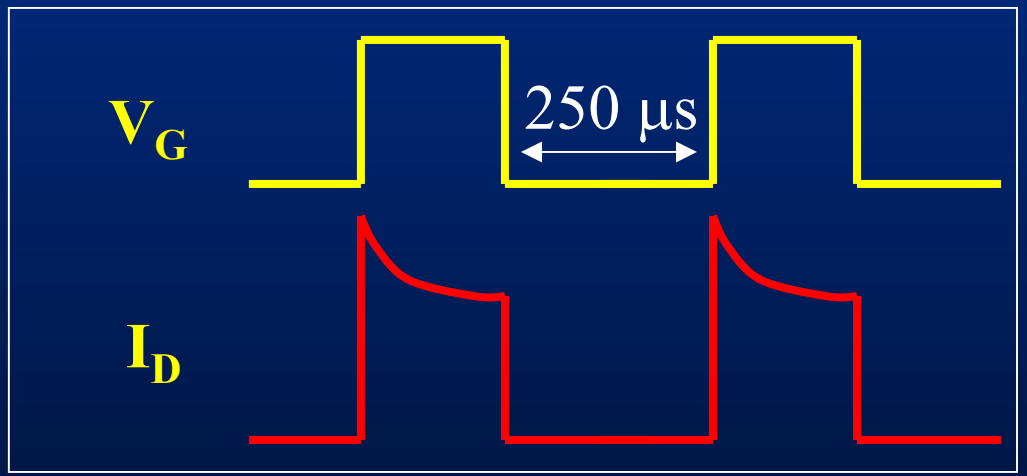
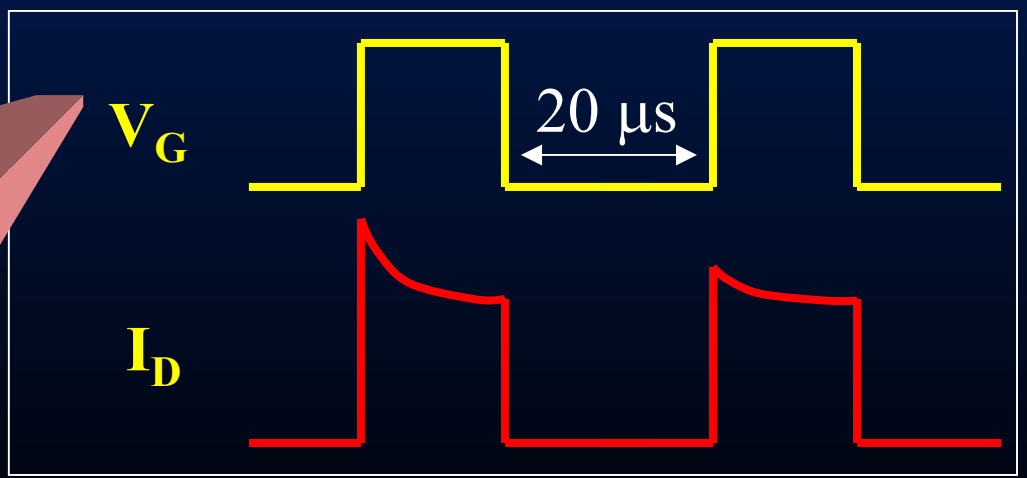


Illustration of the single-transistor latch. "Normal" subthreshold slope at low drain voltage (a), infinite subthreshold slope and hysteresis (b), and device "latch-up" (c).

PDSOI MOSFET: floating-body effects







This is only one example among MANY!

MOSFET Equations: **Body Factor**

Non saturation: $$I_D = \mu C_{ox} \frac{W}{L}\left((V_G - V_{TH})V_D - \frac{1}{2} n V_D^2\right)$$

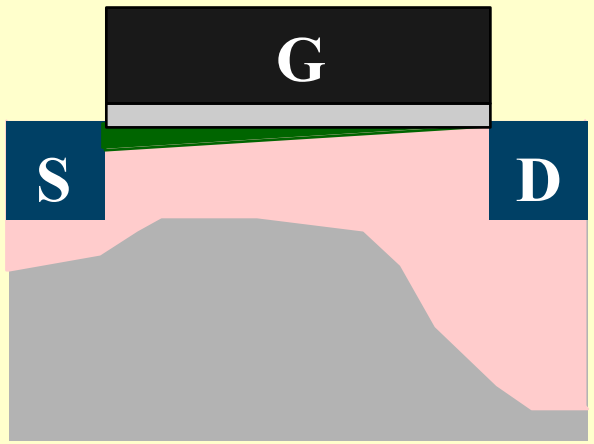
Saturation: $$I_{Dsat} = \frac{1}{2n} \mu C_{ox} \frac{W}{L}\left((V_G - V_{TH})^2\right)$$

Subthreshold swing: $$S = n \frac{kT}{q} \ln(10)$$

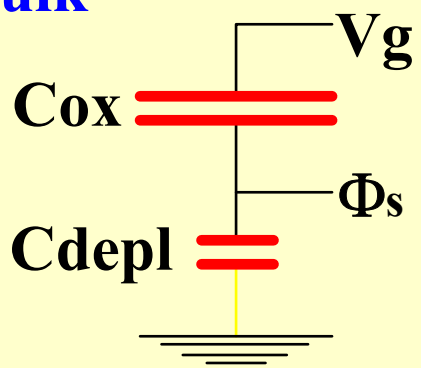
Gain (weak inversion): $$\frac{g_m}{I_D} V_A = \frac{q}{n kT} V_A \qquad (V_A = Early\,voltage)$$

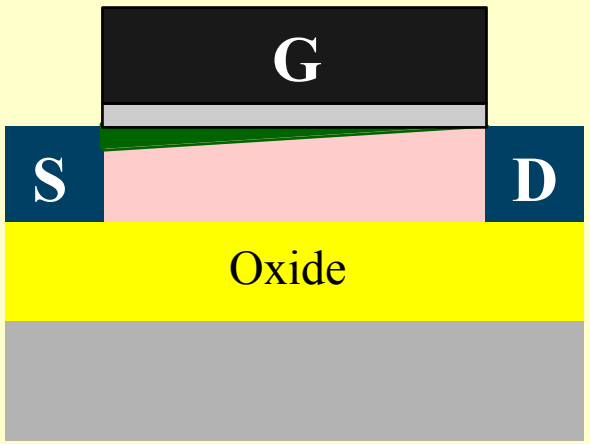
Gain (strong inversion): $$\frac{g_m}{I_D} V_A = \sqrt{\frac{2 \mu C_{ox} W L}{n I_D}} V_A$$

Gate - Channel Coupling

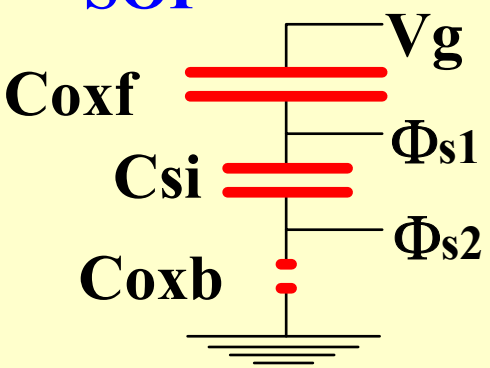


Bulk





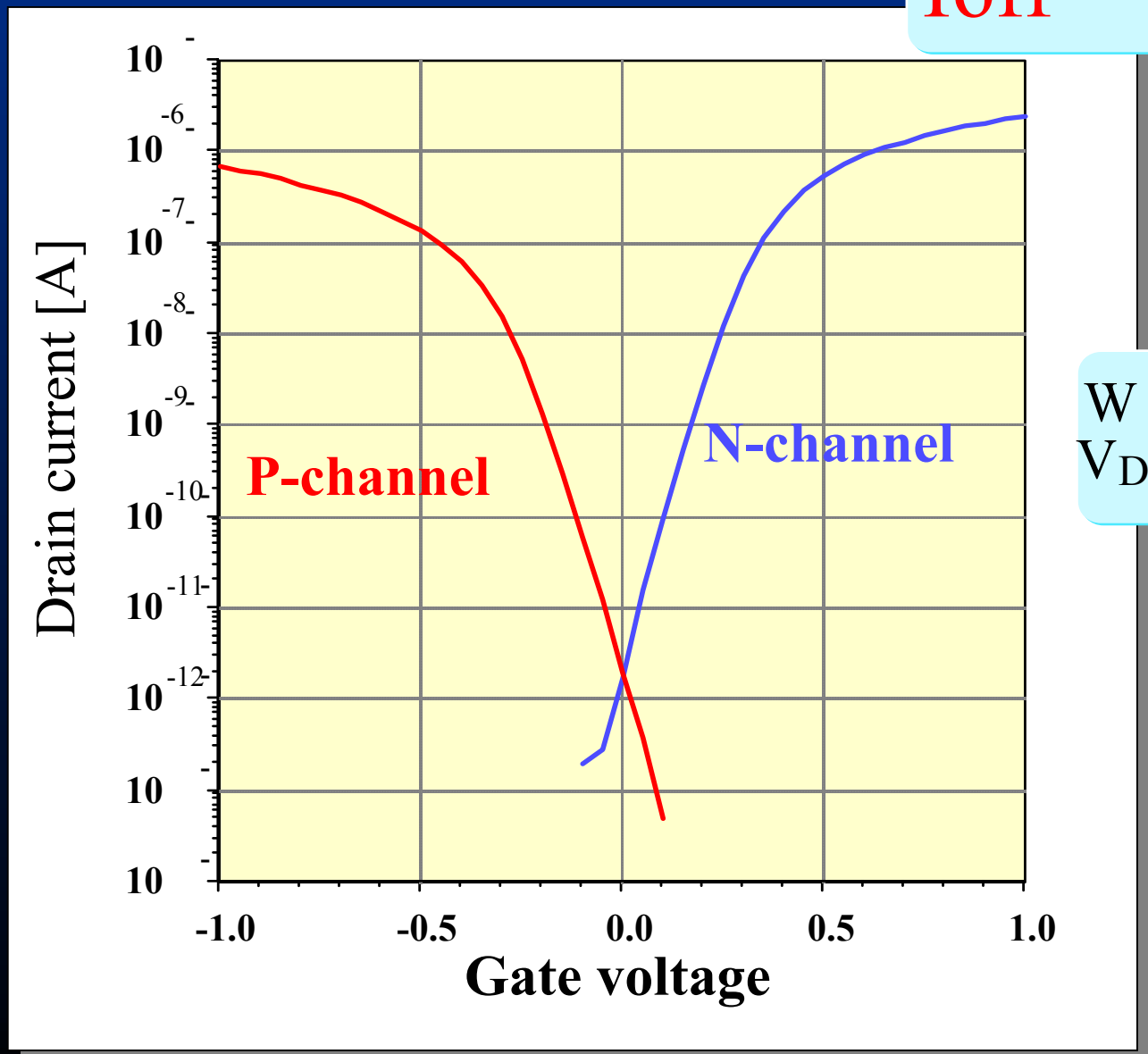
SOI



Body factor: n = …1.5… in Bulk; n = …1.05... in FDSOI

Transistor characteristics

V_{th} = □0.4V
Ioff = 1pA/瘦



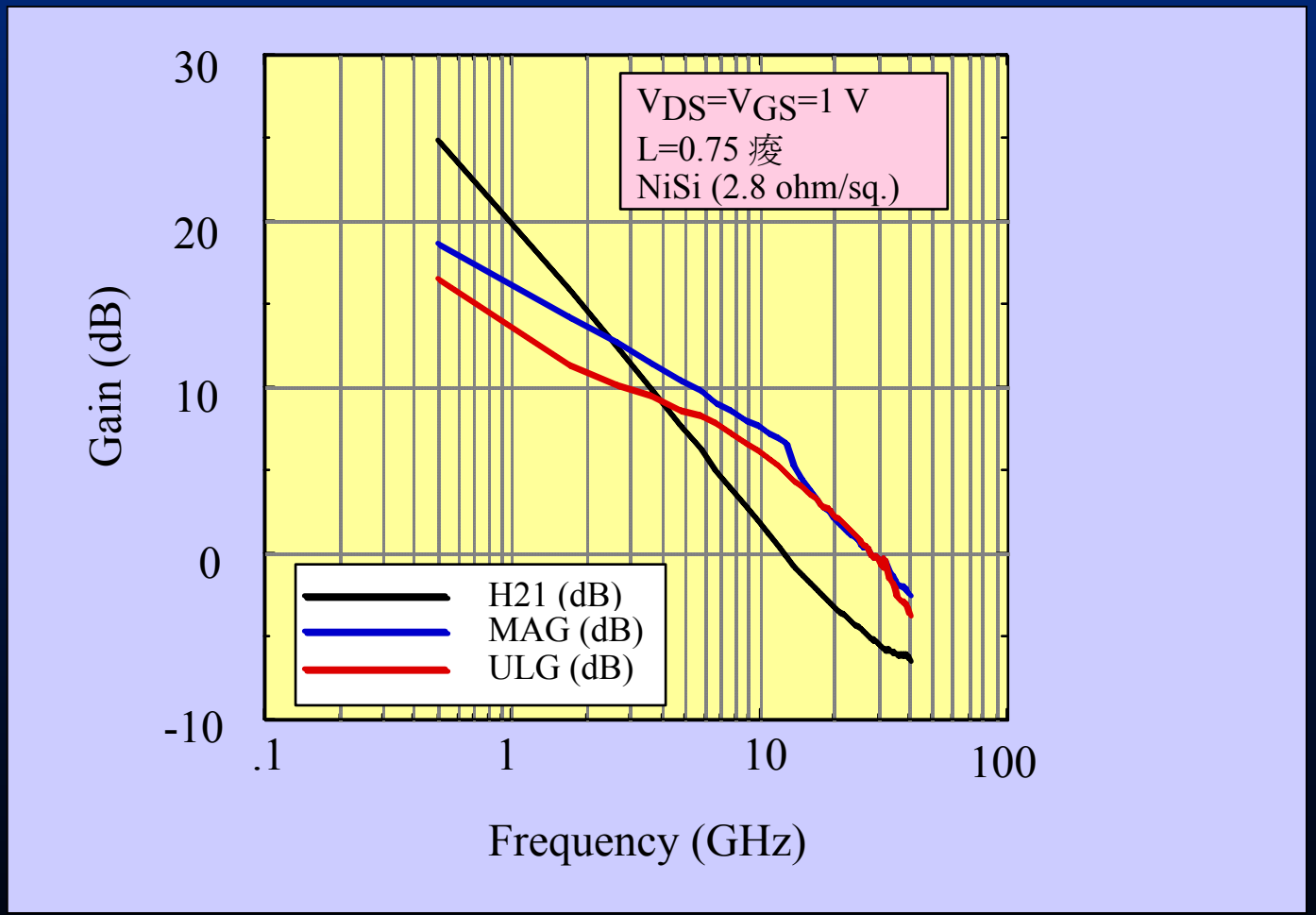
W = L = 3瘦
V_{DS} = ?0mV

Microwave SOI MOSFETs

SOI material	L (μm)	V_D (V)	I_D (mA)	f_T (GHz)	f_{max} (GHz)	Noise figure / Associated gain (dB) at 2GHz
BESOI	1	-	-	-	14	5 / 6.4
SIMOX	1	-	-	-	11	5 / 4.4
SOS	0.35	3	10	23	56	- / -
SIMOX	0.32	3	33	14	21	3 / 13.4
SIMOX	0.25	3	41	23.6	32	1.5 / 17.5
SIMOX	0.75	0.9	3	10	11	1.5 / 9
SIMOX	0.75	0.9	10	12.9	30	- / 13.9 (10.4¥)
SIMOX	0.3	2	-	-	24.3	0.9 / 14
SOS*	0.5	2	2	26	60	1.7 / 16.3
SIMOX	0.2	2	125	28.4	46	1/15.3†
SIMOX	0.07	1.5	5	150		
Unibond	0.25	1.5		50	75	

(*) Metal-gate technology is used; (†) at 3 GHz and (¥) at 5 GHz.

Low-voltage Microwave MOSFET



Rather unsophisticated device: t_{ox} = 30 nm …

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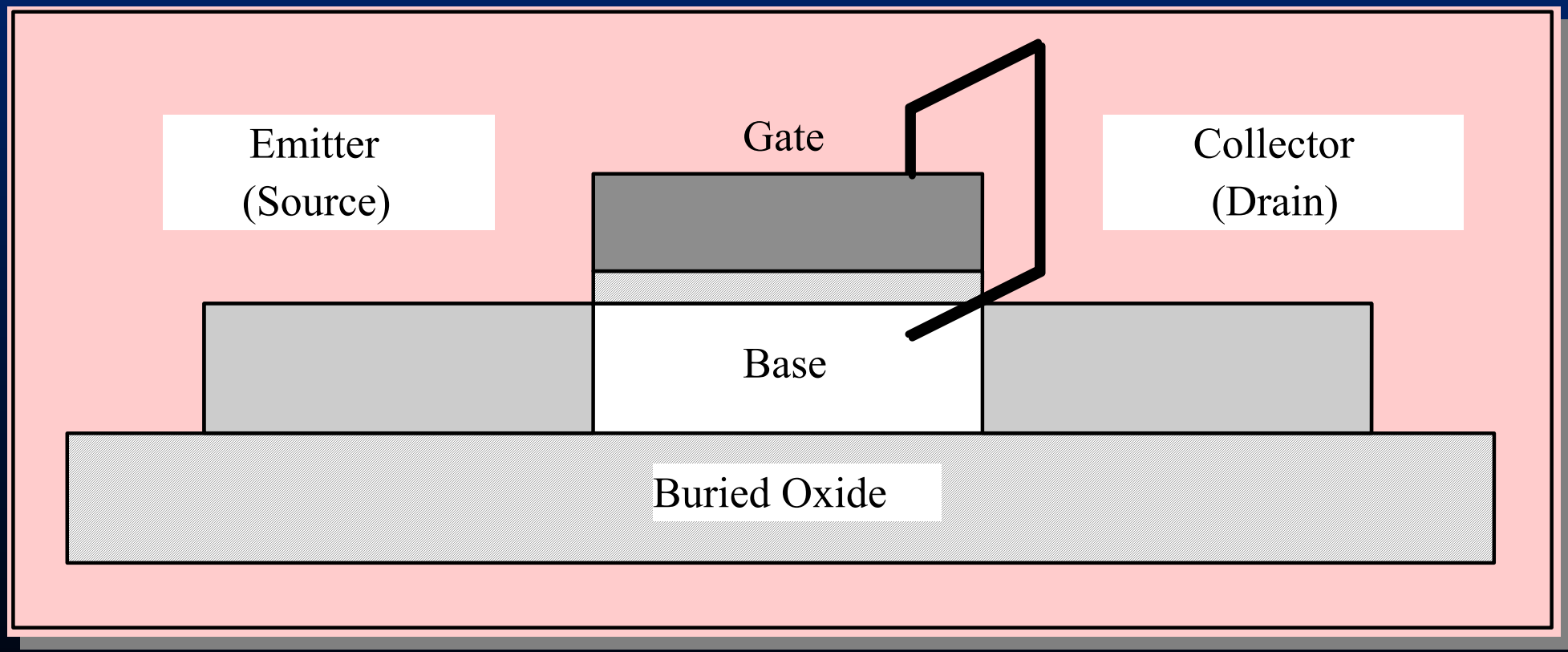
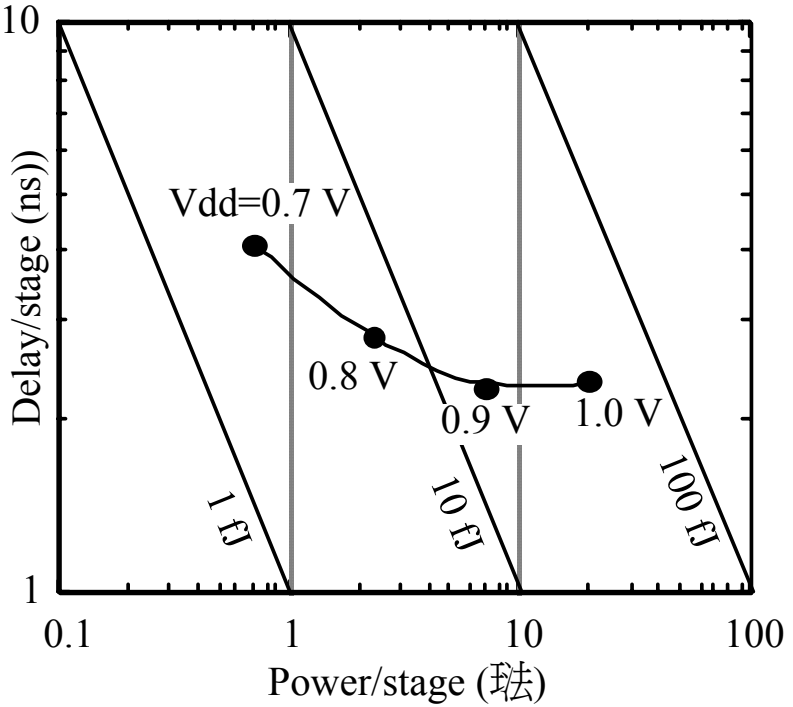
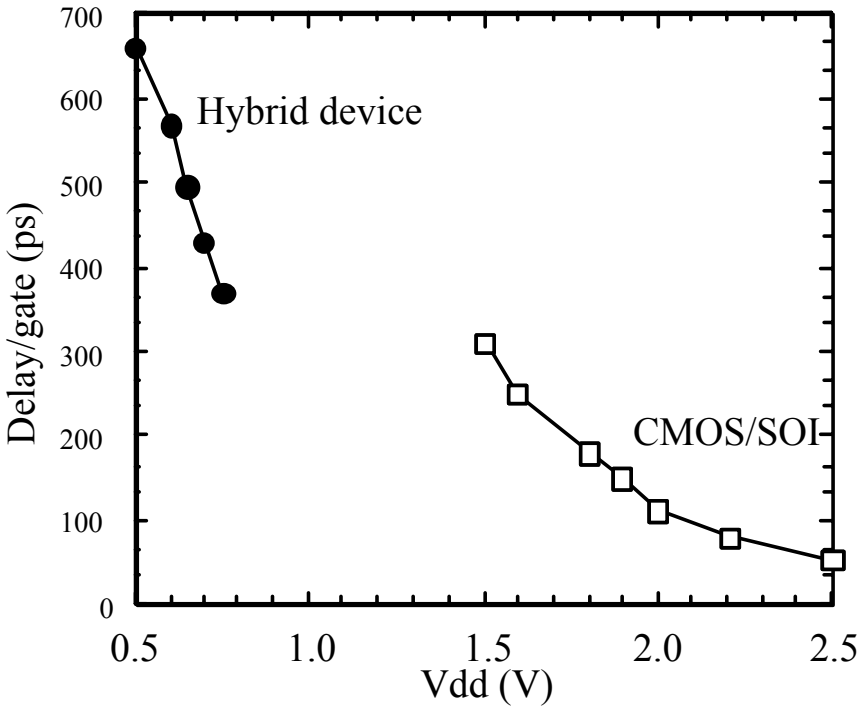
Hybrid bipolar-MOS
aka DTMOS (Dual-Threshold MOS)
aka MTCMOS (Multiple-Threshold CMOS)





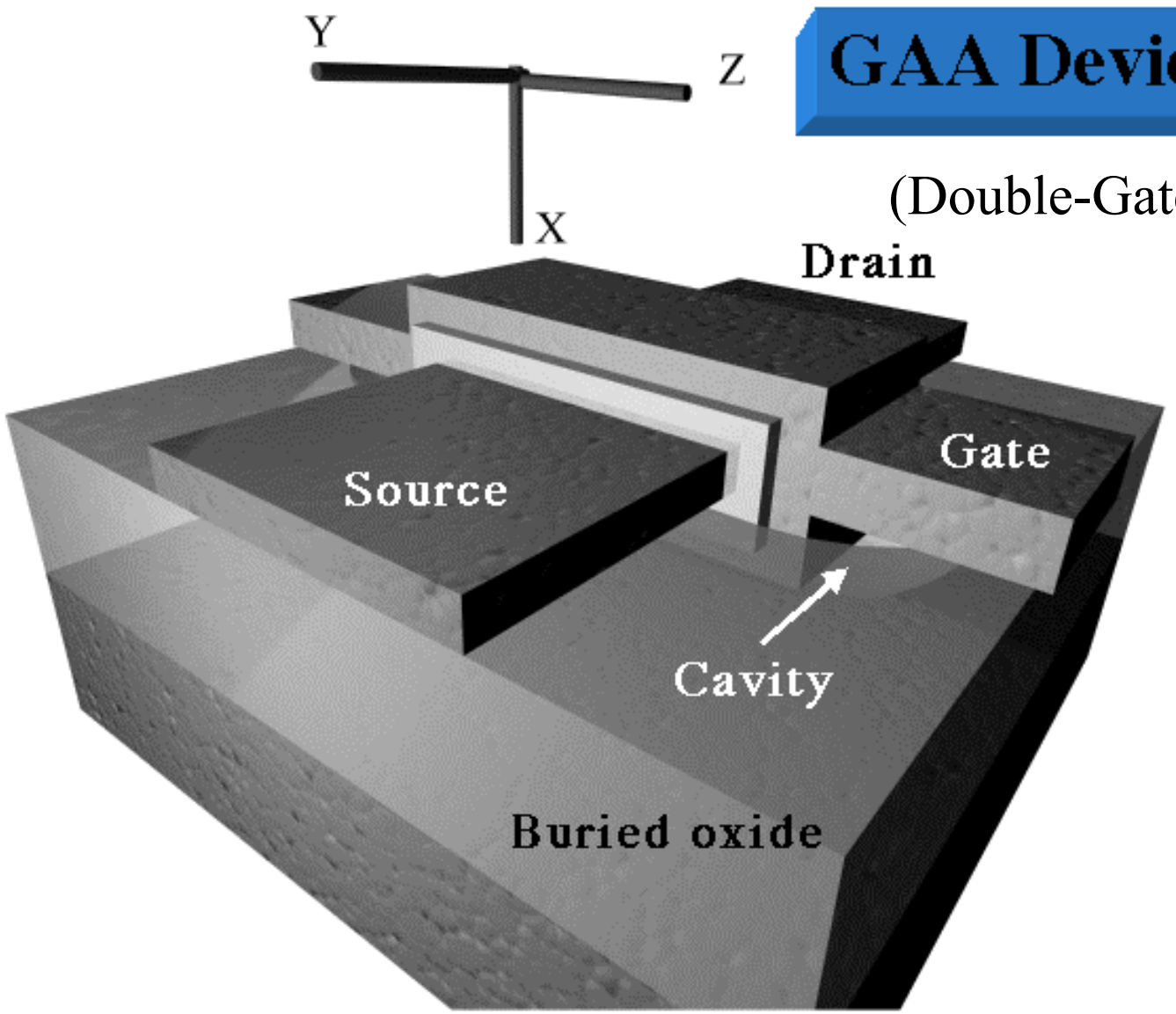
$L_{eff,N} = 0.45\ \mu m$, $L_{eff,P} = 0.58\ \mu m$
(1987)



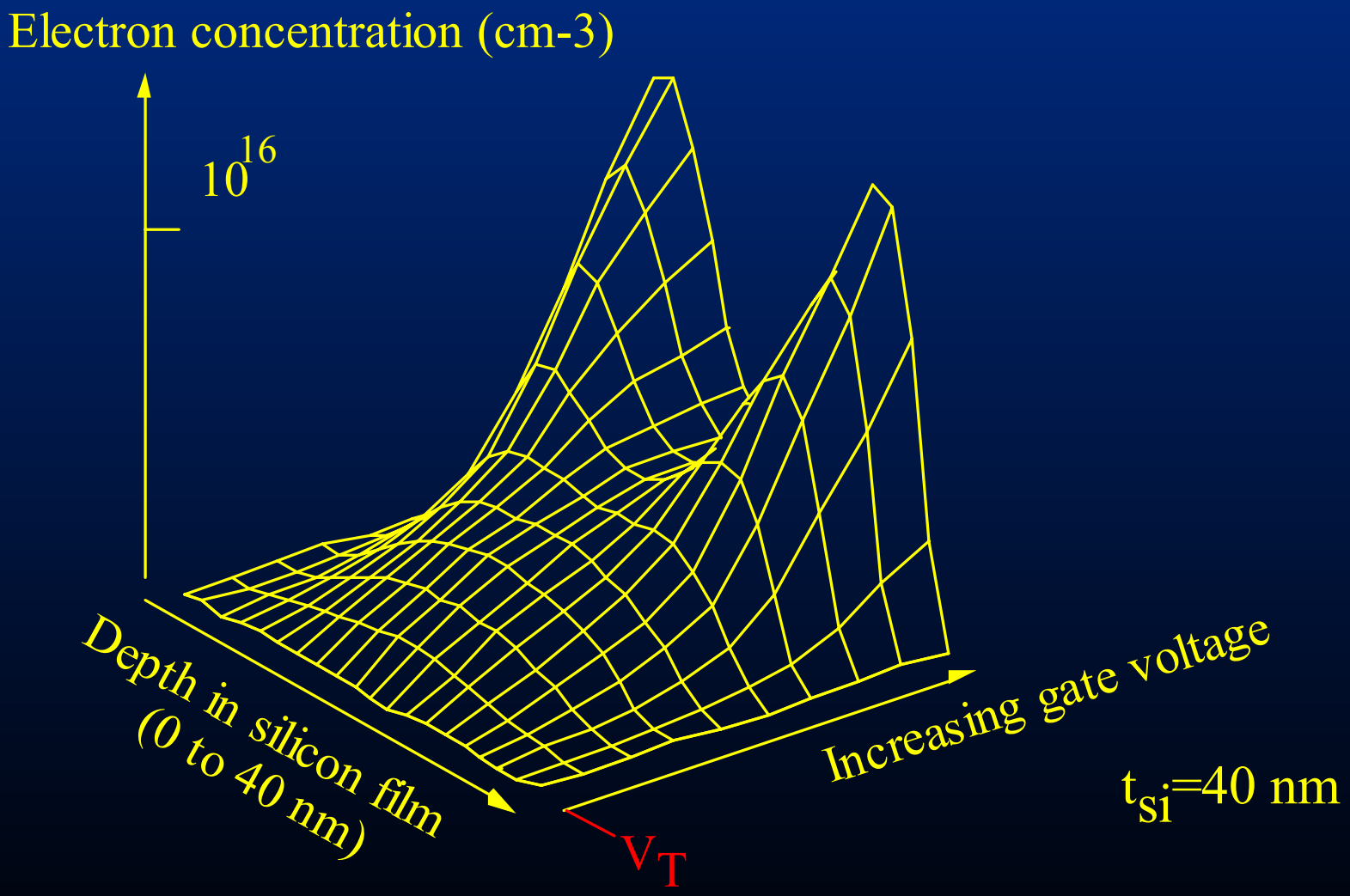
$L_{eff,N} = L_{eff,P} = 0.3\ \mu m$
(1994)

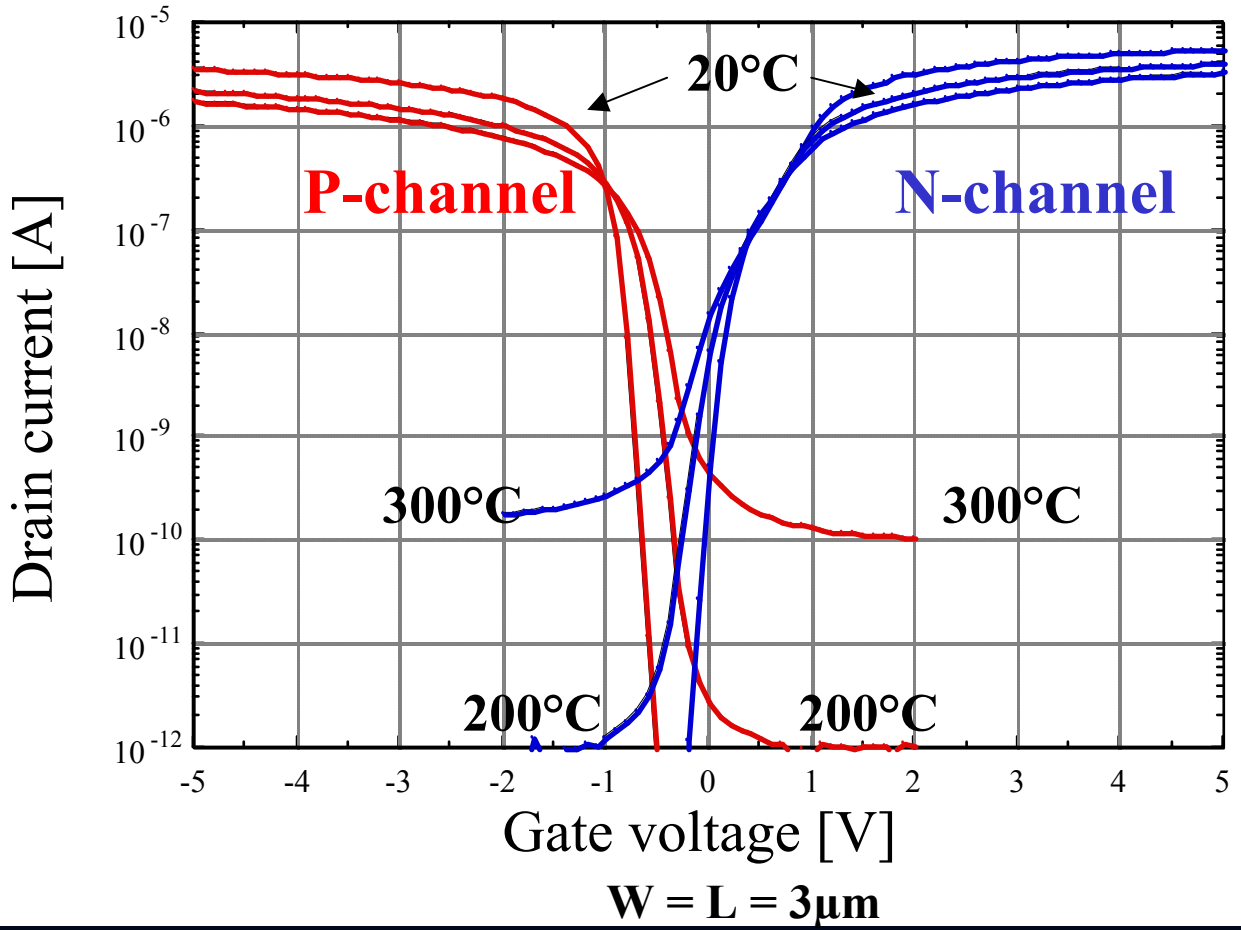
GAA Device

(Double-Gate MOSFET)

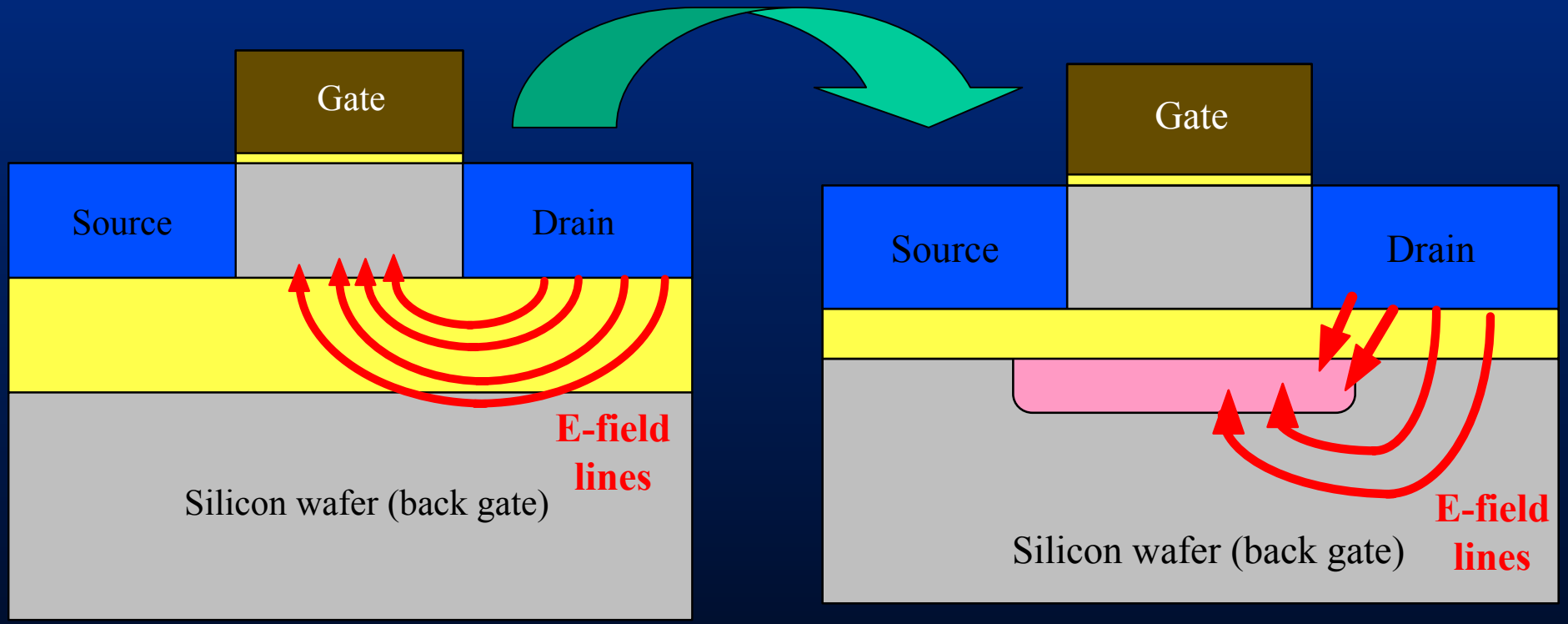


Double-Gate SOI MOSFET:
Volume Inversion



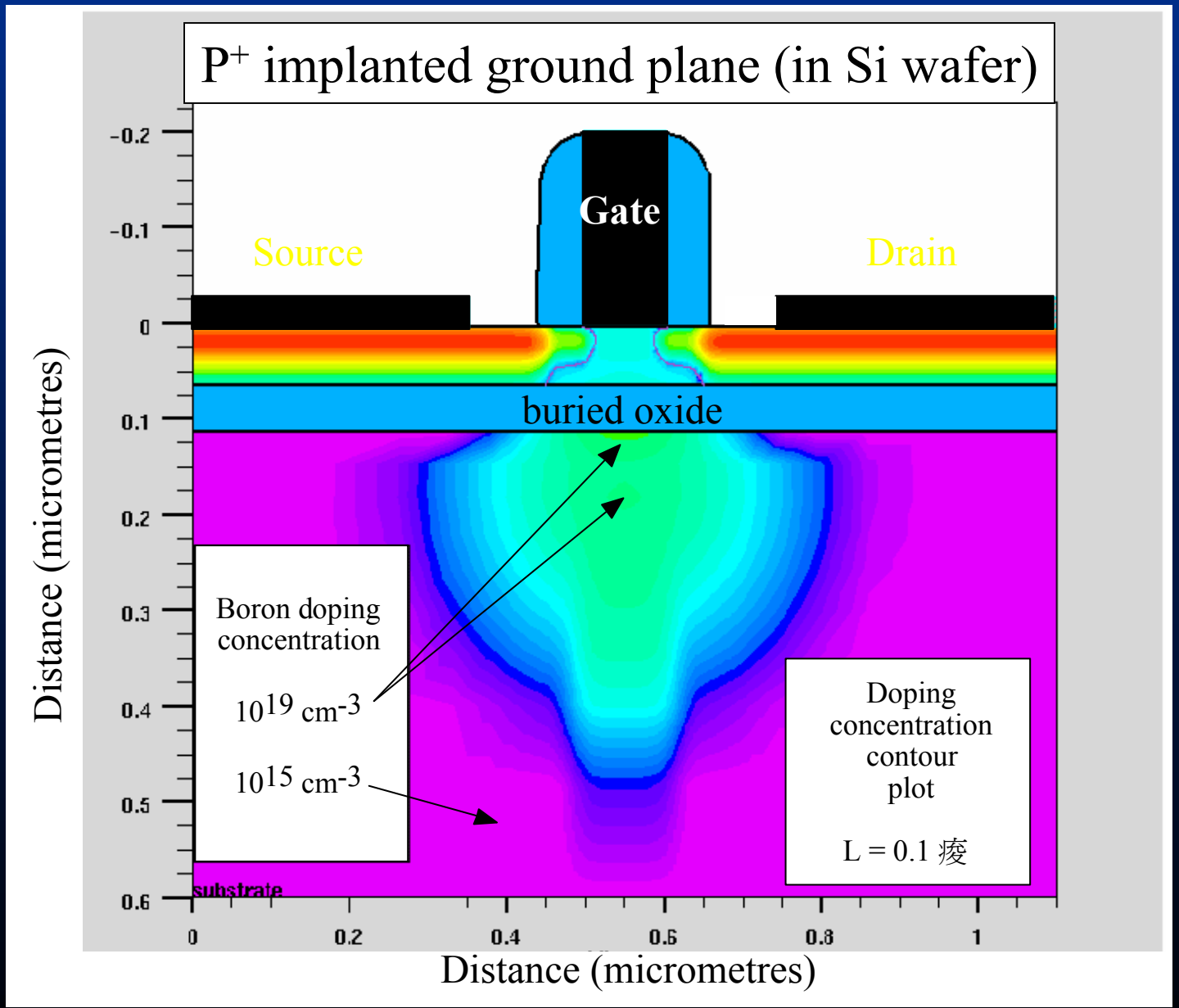

Drain current [A]
10 -5
10 -6
10 -7
10 -8
10 -9
10 -10
10 -11
10 -12
-5
-4
-3
-2
-1
0
1
2
3
4
5
Gate voltage [V]
20°C
P-channel
N-channel
300°C
300°C
200°C
200°C
W = L = 3µm

Ground Plane SOI MOSFET



"The ground-plane concept for the reduction of short-channel effects in fully depleted SOI devices", Ernst, T., and Cristoloveanu, S., Electrochemical Society Proceedings 99-3, p. 329, 1999

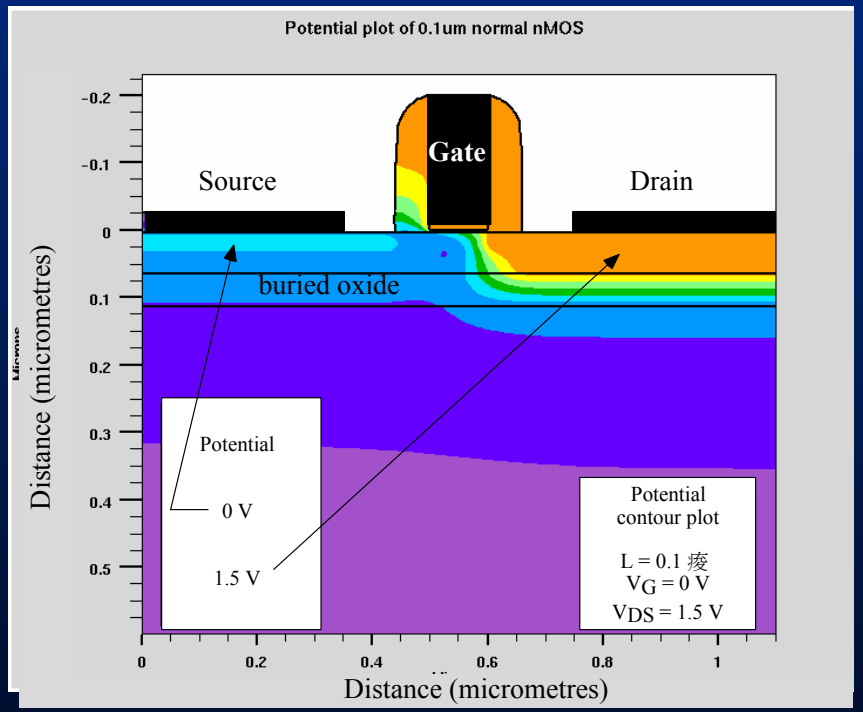
Ground-Plane SOI MOSFET



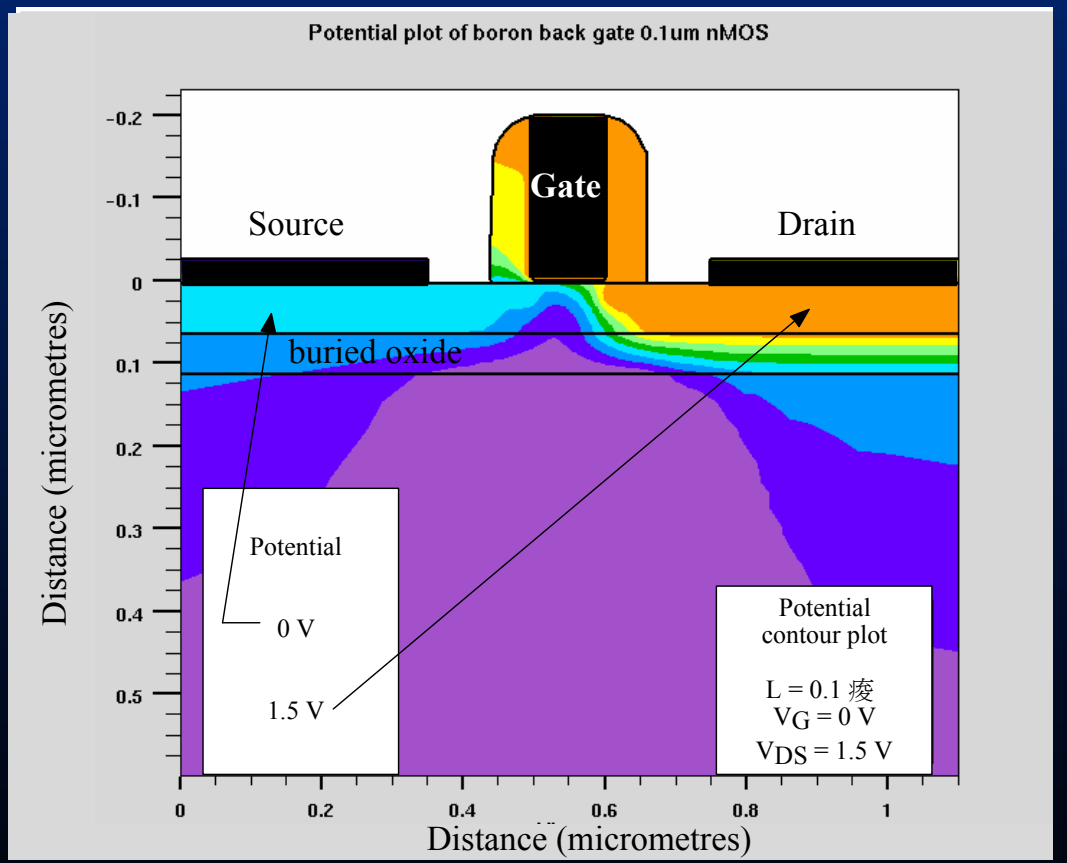
Ground-Plane SOI MOSFET

NSREC 2001 VANCOUVER BC

Equipotentials (Regular SOI MOSFET)



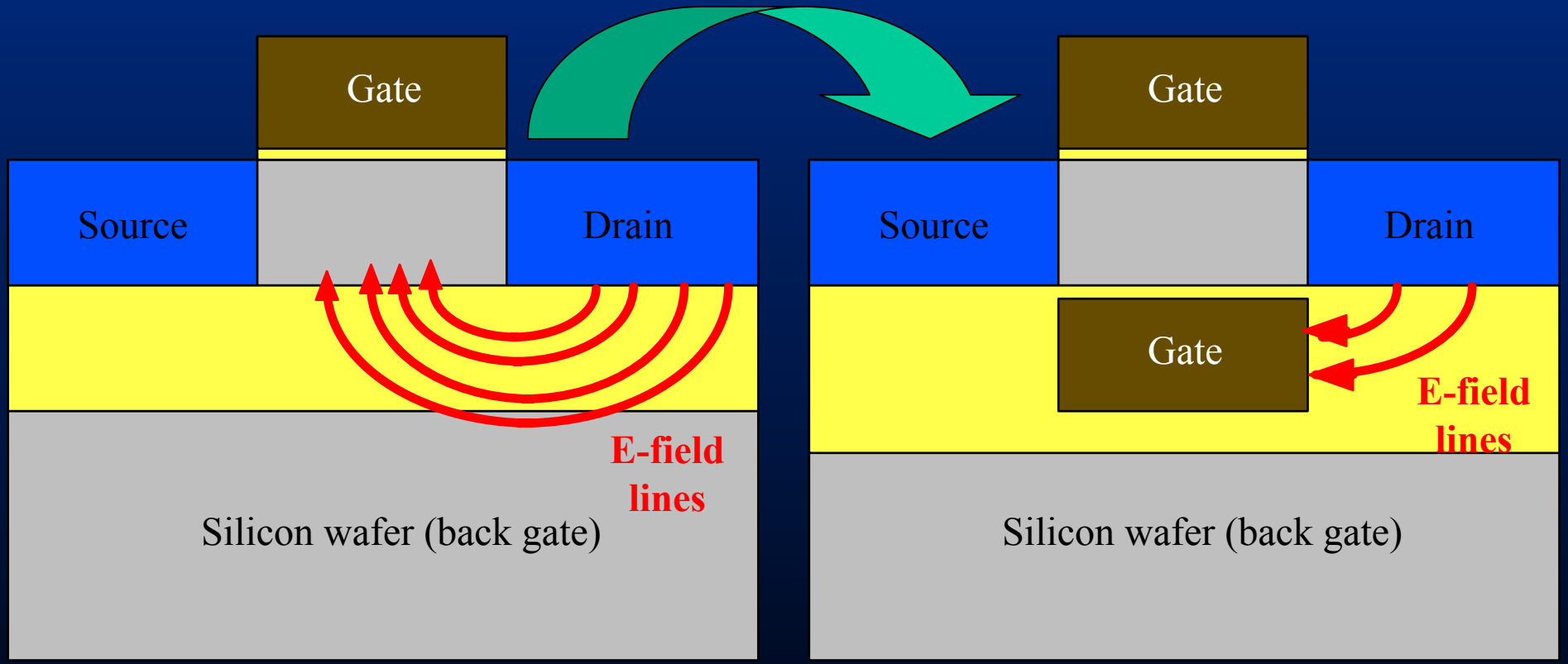
Equipotentials (Ground-Plane SOI MOSFET)



Regular FD SOI vs. Ground-Plane FD SOI

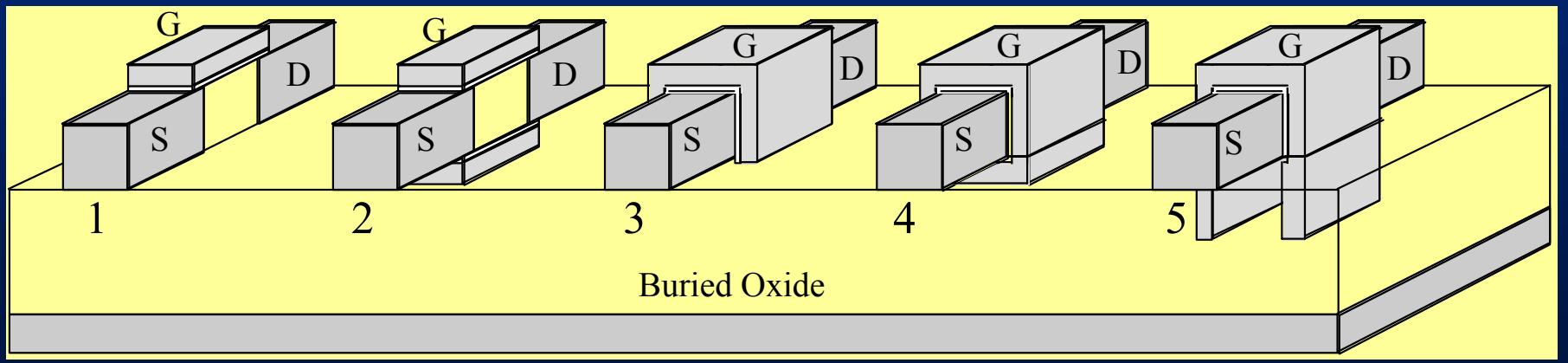
	Regular **SOI MOSFET**	Ground-Plane **SOI MOSFET**	Regular **SOI MOSFET**	Ground-Plane **SOI MOSFET**
L (nm)	S (mV/dec)	S_{GP} (mV/dec)	DIBL (mV)	$DIBL_{GP}$ (mV)
50	99	89	350	260
70	91	84	272	190
100	83	77	190	120
200	74	71	80	70
500	71	69	45	40

Double-Gate SOI MOSFET



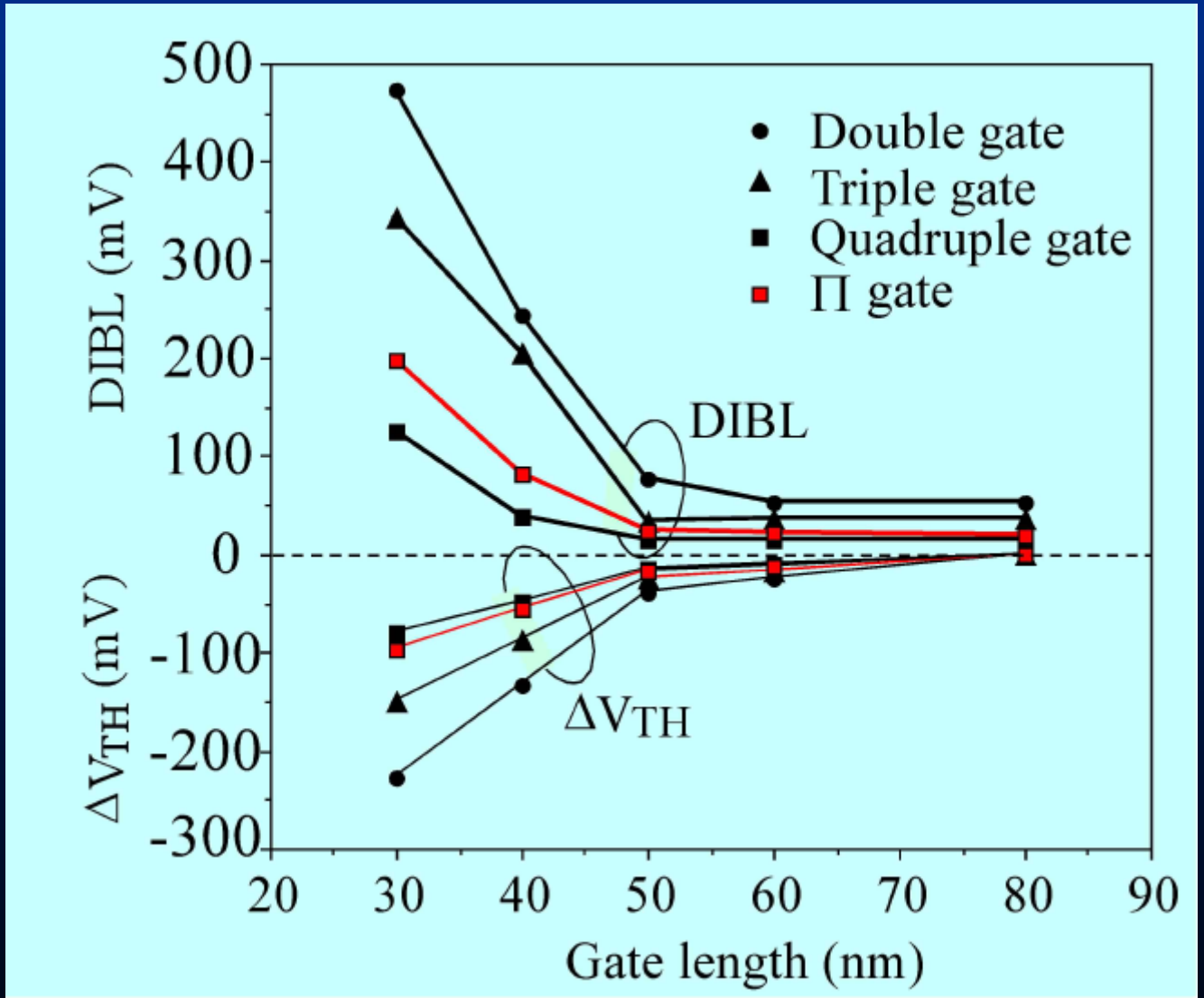
J.P. Colinge, M.H. Gao, A. Romano, H. Maes and C. Claeys, Technical Digest of IEDM, p. 595, 1990

Multiple-Gate SOI MOSFETsc



Different gate configurations for SOI devices:
1) single gate; 2) double gate; 3) triple gate; 4) quadruple gate (or: gate-all-around structure); 5) ∏-gate MOSFET.

Multiple-Gate SOI MOSFETsc

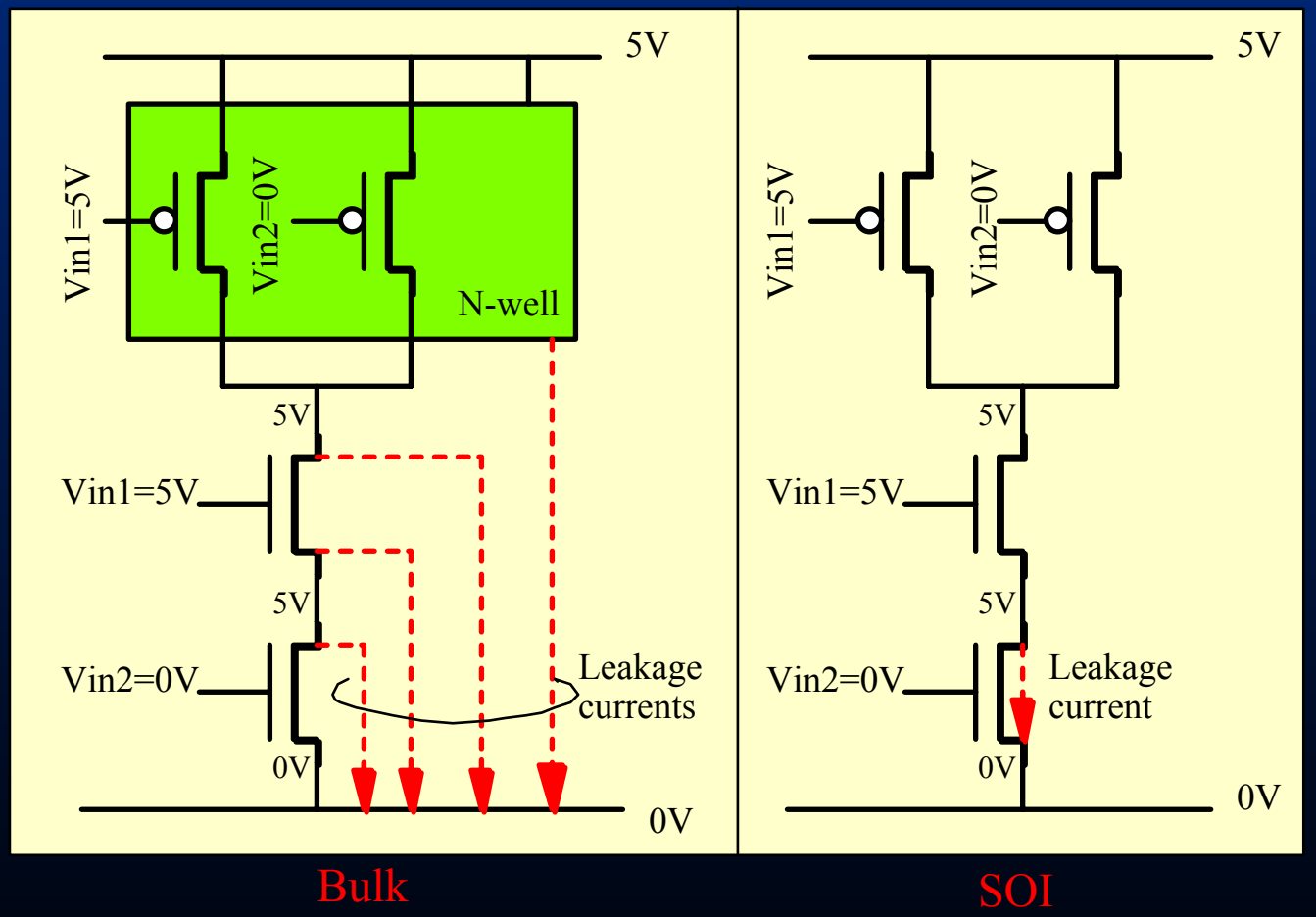


DIBL in fully depleted SOI MOSFETs with different gate structures and different effective gate lengths. V_{DS} = 100 mV.

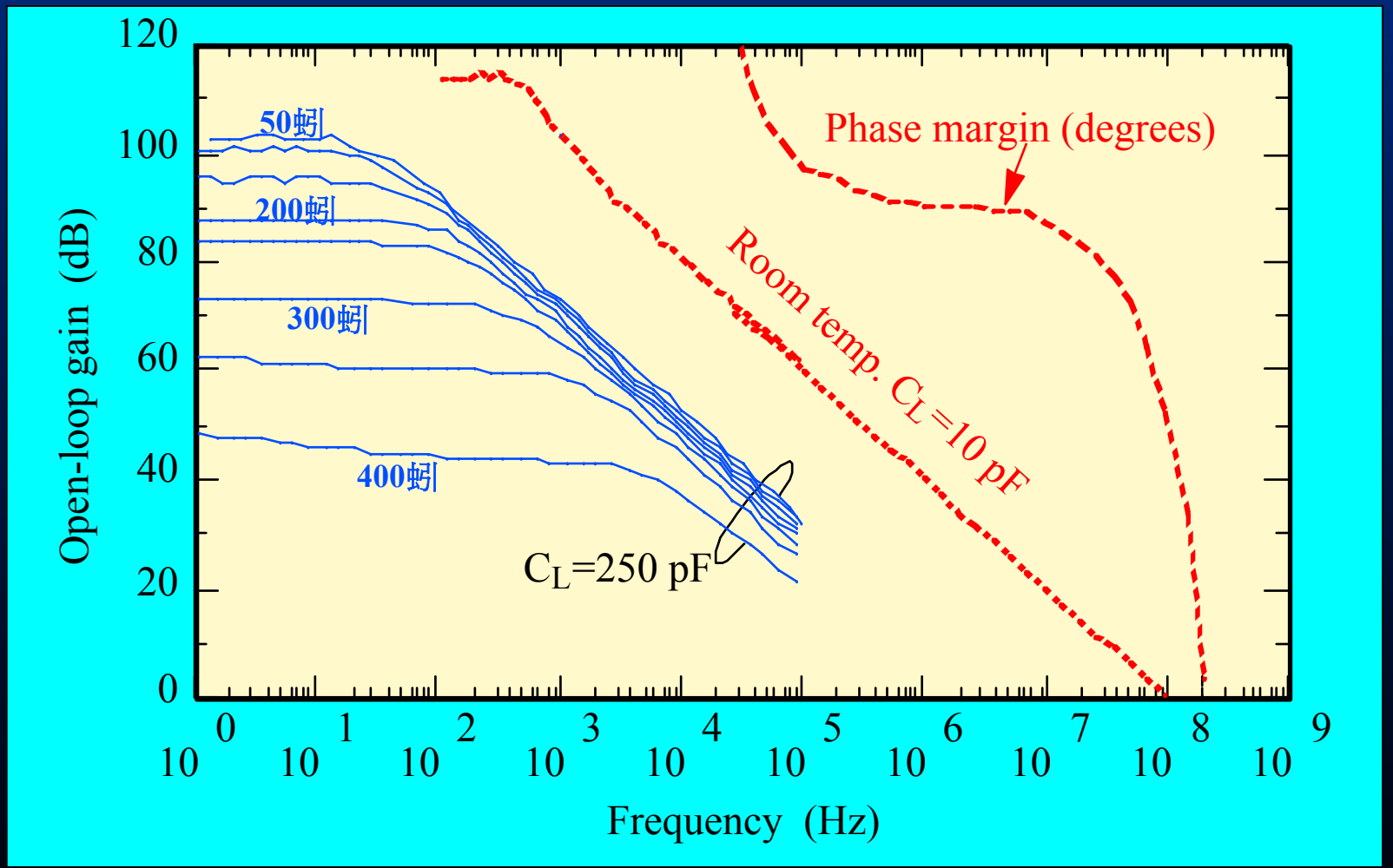
Outline

- ◊ Introduction (Where SOI Technology stands today)
- ◊ SOI Materials (SOS, SIMOX, Wafer Bonding, Unibond®)
- ◊ The "Classical" SOI MOSFET (Partially/Fully Depleted)
- ◊ Other SOI MOSFETs (Hybrid, Double Gate, Ground Plane, multiple gates)
- ◊ SOI Circuits (Hi-T°, Low-Power, RAMs)

Leakage currents: example of NAND gate



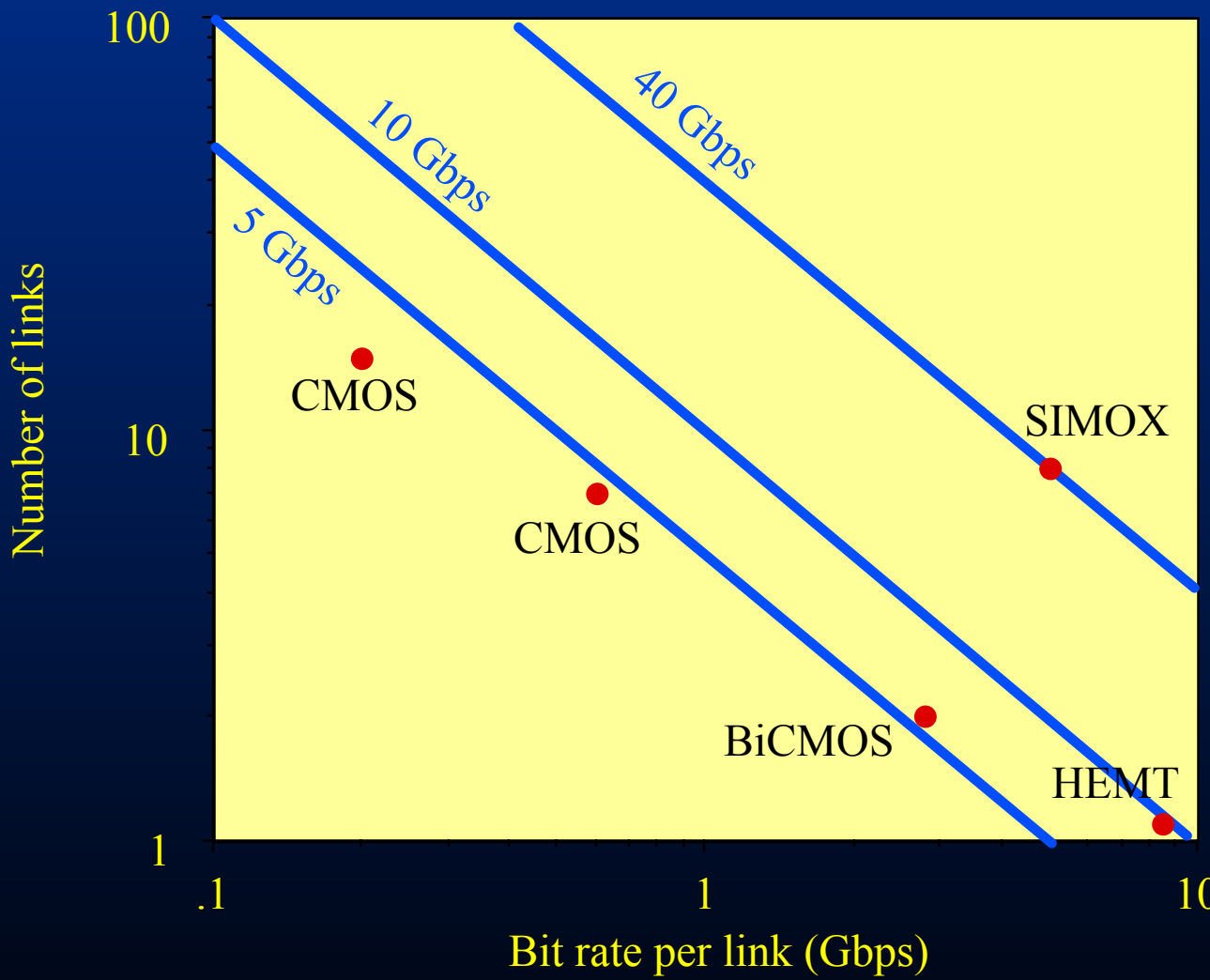
SOI CMOS operational amplifier: High-temperature operation



Low-Voltage Circuits

Circuit	V_{dd}	Speed	Company	
甥ontroller CPU	0.9V	5.7 MHz	Motorola	PD
8k-gate 16b ALU	0.5V	40 MHz	NTT	FD
300k gate array	1.2V	38 MHz	NTT	FD
16x16b multiplier	0.5V	18 ns	Toshiba	hybrid
PLL	1.5V	1.1 GHz	Sharp	FD
32-bit ALU	0.5V	260 MHz	Toshiba	hybrid
8x8 ATM switch	2V	40 Gb/s	NTT	FD
560k master array	1V	50 MHz	Mitsubishi	
0.2 瘦 64b PPC	1.8V	550 MHz	IBM	PD
0.25 瘦 64b ALPHA	1.5V	600 MHz	Samsung	FD

ATM Switch



Y. Ohtomo, S. Yasuda, M. Nogawa, J. Inoue, K. Yamakoshi, H. Sawada, M. Ino, S. Hino, Y. Sato, Y. Takei, T. Watanabe, and K. Takeya, Digest of Technical papers, International Solid-State Circuits Conference, p. 154, 1997

DRAMs

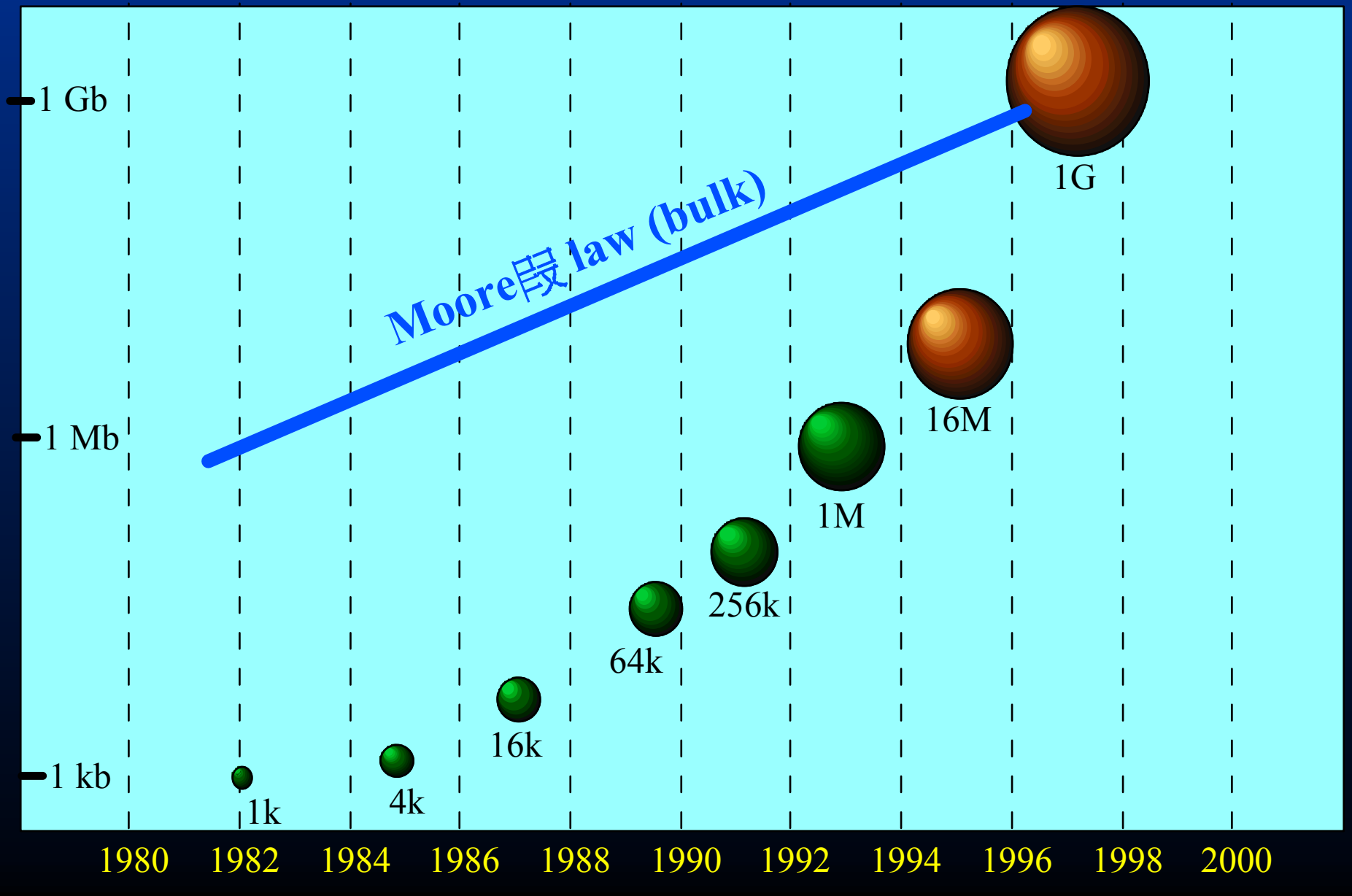
* Much lower rate of soft errors
* Less junction leakage
* Reduced bit line capacitance
* Higher pass-transistor transfer efficiency

Storage capacitance can be reduced 2-3 ×
Supply voltage can be reduced below 1 V

Low-Voltage Memories

Year	Company	Memory chip	V_{dd}
1993	IBM	512 kb SRAM	1V
1993	Mitsubishi	64 kb DRAM	1.5V
1995	Samsung	16 Mb DRAM	
1996	Mitsubishi	16Mb DRAM	0.9 V
1997	Hyundai	1 Gb DRAM	2 V

SOI RAMs


1 Gb
1 Mb
1 kb
Moore's law (bulk)
1k
4k
16k
64k
256k
1M
16M
1G
1980
1982
1984
1986
1988
1990
1992
1994
1996
1998
2000

Conclusion

SOI now used in commercial products

PD and FD SOI MOSFET physics

Advanced SOI MOSFET structures