Ultralow-power SRAM technology

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An ultralow-standby-power technology has been developed in both 0.18-μm and 0.13-μm lithography nodes for embedded and standalone SRAM applications. The ultralow-leakage six-transistor (6T) SRAM cell sizes are 4.81 μm^2 and 2.34 μm^2, corresponding respectively to the 0.18-μm and 0.13-μm design dimensions. The measured array standby leakage is equal to an average cell leakage current of less than 50 fA per cell at 1.5 V, 25°C and is less than 400 fA per cell at 1.5 V, 85°C. Dual gate oxides of 2.9 nm and 5.2 nm provide optimized cell leakage, I/O compatibility, and performance. Analyses of the critical parasitic leakage components and paths within the 6T SRAM cell are reviewed in this paper. In addition to the well-known gate-oxide leakage limitation for ULP technologies, three additional limits facing future scaled ULP technologies are discussed.

Introduction

Static random-access memory (SRAM) continues to be a critical component across a wide range of microelectronics applications from consumer wireless to high-end workstation and microprocessor applications. The increased demand for lighter portable electronic applications with extended battery life has fueled the need for technologies that provide low standby power [1, 2]. In this work, we describe specific components of the learning required to develop an ultralow-standby-power technology that offers more than three orders of magnitude lower standby power than conventional performance-driven technologies. The development effort was based on high-performance logic rather than DRAM technology [3]. As a result, much of the processing remained consistent with or identical to that used for the high-performance logic technology. The ULP technologies are therefore able to share the same shallow-trench isolation (STI), polysilicon gate definition, silicide, and post-device processing with the base high-performance logic technology [4]. This approach provides lower process cost, maintains a common tool set, and shares yield learning with the base high-performance logic processes. A low wafer-processing cost was maintained, since special SRAM cell features such as local interconnects (LIs) or self-aligned contacts (SACs) were not required.

Understanding the specific leakage mechanisms that govern the cell and array leakage as a function of temperature and applied voltage is crucial to controlling the SRAM array standby power. For the present discussion, the leakage mechanisms are classified as being either parametric (intrinsic) or defect-related in nature. The SRAM array parametric standby leakage contributors include well isolation leakage [5], subthreshold device leakage [6], gate-oxide tunneling [7], reverse-bias diffusion leakage [8], and gate-induced drain leakage (GIDL) [9, 10] for both n-FET and p-FET devices. Implant damage [11], STI stress-induced diffusion leakage [12], silicide defects [13], and contact-related defects [14] must be very carefully controlled or eliminated in order to achieve the ULP leakage obtained. In this paper we review each of the parasitic components and their impact on the overall cell and array standby power. We also discuss specific future challenges to achieving ultralow power for nodes less than 0.13 μm.

Technology overview

A brief summary of some of the more critical ULP technology characteristics of the technologies described in this paper for both the 0.18-μm and 0.13-μm lithography nodes is given in **Table 1**. Although the device widths and critical dimensions (contact size, n+ to p+ spacing, etc.)

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Table 1 Device parametrics for ULP technology.

Parameter	*1.5-V devices*		*2.5-V devices*	
	n-FET	*p-FET*	*n-FET*	*p-FET*
t_{ox} (nm)	2.9	2.9	5.2	5.2
I_{on} (μA/μm)	248	165	498	210
I_{off} @25°C (fA/μm)	10	10	100	100
I_{off} @85°C (fA/μm)	500	500	2500	3000
L_{poly} (μm)	0.13	0.13	0.23	0.23
V_{tsat} (V)	0.79	−0.79	0.67	−0.67
Junction cap. (fF/μm^2)	1.35	1.7	1.1	1.3
n+/p+ space	0.74 μm for 0.18-μm node 0.46 μm for 0.13-μm node		1.12 μm for 0.18-μm node 0.6 μm for 0.13-μm node	
GIDL (fA/μm)	2.5	30	30	100

were reduced for the 0.13-μm technology, the device design, the nominal L_{poly} dimension,[1] and gate-oxide thicknesses remained the same for both technology nodes. The dimensional tolerances were scaled in a manner consistent with the lithography generation. Both 1.5-V and 2.5-V devices are provided along with dual gate-oxide thicknesses of 2.9 nm and 5.2 nm, respectively. The devices optimized at 1.5 V exhibit a saturated threshold voltage (V_{tsat}) of 0.79 V for the n-FET and −0.79 V for the p-FET. This threshold voltage was selected to achieve the target off-current of <10 fA/μm at 25°C and still provide acceptable cell performance. The nominal on-current in saturation was 248 μA/μm for the n-FET and 165 μA/μm for the p-FET at 1.5 V with a value for L_{poly} of 0.13 μm. The gate-oxide thickness for the 1.5-V devices was established at 2.9 nm to minimize gate leakage. The nitrided gate oxide exhibited an inversion-equivalent oxide thickness of 3.7 nm for the n-FET and 3.8 nm for the p-FET. A significant effort was devoted to achieving low values for gate-bounded drain leakage. Because there is significantly more gate perimeter for the n-FET in the SRAM cell, it was important to reduce the n-FET GIDL as much as possible. The n-FET GIDL was reduced to <2.5 fA/μm and the p-FET GIDL was reduced to <30 fA/μm. The junction area capacitance (JAC) for the 1.5-V devices was 1.35 fF/μm^2 for the n-FET and 1.7 fF/μm^2 for the p-FET, slightly higher than is typical of high-performance technologies. The JAC was higher because of the halo dose used to maintain the device thresholds at the minimum drawn channel lengths. The 1.5-V device provided low-leakage SRAM cell characteristics.

The 2.5-V devices had a threshold voltage of 0.67 V for the n-FET and −0.67 V for the p-FET and a corresponding on-current of 498 μA/μm and 210 μA/μm for an L_{poly} of 0.23 μm. The off-current was less than 0.1 pA/μm at 25°C for both n-FET and p-FET. The GIDL was 30 fA/μm for the n-FET and 100 fA/μm for the p-FET. The gate oxide was 5.2 nm by extrapolated capacitance and provided an n-FET inversion oxide thickness of 6.2 nm and a p-FET inversion oxide thickness of 6.4 nm. The junction area capacitance was 1.1 fF/μm^2 for the n-FET and 1.3 fF/μm^2 for the p-FET. This device provided I/O and peripheral circuit performance for the stand-alone SRAM operation.

The technology offers the low-resistance contacts and interconnects associated with self-aligned $CoSi_2$ silicide processing and planar copper metallization back-end-of-line (BEOL) processing. Although blocking of silicide formation in the SRAM cell was evaluated, the array leakage targets were met with fully silicided arrays.

Cell design

The cell designs for 0.18-μm and 0.13-μm nodes are similar in layout, each containing a segmented polysilicon wordline strapped with the first level of metal and a shared ground contact between two adjacent cells. The cell sizes are (1.87 μm × 2.56 μm, or 4.81 μm^2) in 0.18-μm lithography, and (1.3 μm × 1.8 μm, or 2.34 μm^2) in 0.13-μm lithography. **Figure 1(a)** shows the cell layout for the 0.13-μm design optimized to achieve density and yield. The designs of the polysilicon, active silicon, and first level of metal were optimized using optical proximity correction (OPC) based on the aerial image modeling [15] shown in **Figure 1(b)**. The final cell design provides RAM density and preserves compatibility with the base logic process. Contact-related leakage mechanisms were mitigated by providing a border adequate to land the contact on the diffusion regions. In addition, the design includes a segmented polysilicon wordline which is strapped by M1. This choice of cell design permitted the addition of an optional nitride layer to block the growth of silicide over the four n-FET devices in the cell to further isolate or eliminate the specific mechanisms associated with silicide on the cell leakage. **Figure 1(c)** is an SEM image taken of

[1] L_{poly} = polysilicon line width.

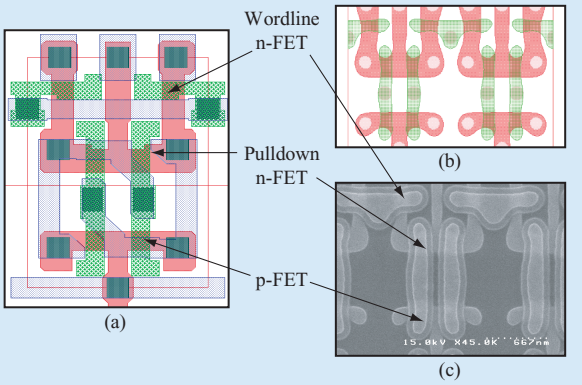

Figure 1

SRAM cell in 0.13-μm lithography (dimensions 1.3 × 1.8 μm, or 2.34 μm^2): (a) Design; (b) simulation of cell; (c) SEM taken just before silicide processing.

the cell region just prior to silicide processing; it shows the patterned diffusion and polysilicon regions in the cell that correspond to the drawn shapes in Figure 1(a).

Cell stability, as characterized by the static noise margin (SNM), was evaluated across a broad range of voltage and temperature conditions [16–18] for the cell designs selected. Cell design β ratios[2] of 1.37 and 1.3 were used for the 0.18-μm design and the 0.13-μm design, respectively. This design point provided the optimum cell stability and cell read current for proper signal development. The higher threshold voltage used in the ULP technologies results in an improved static noise margin in the cell, which allows reduced β ratios compared with the higher-performance device design points. This fact allows the β ratio for the ULP SRAM to be smaller than required for the high-performance technology and thereby enable improved cell read current. **Figures 2(a)** and **2(b)** respectively show the measured and modeled (SPICE) butterfly curves for the cell, with two different threshold voltages at 25°C for the 0.18-μm cell design. The simulation and measurements were done with the wordline held at high voltage (i.e., V_{DD}) and either internal node was ramped while the opposite node voltage was measured. The room-temperature static noise margin was measured to be ~500 mV for the high-V_t case and ~250 mV for the higher-performance devices with lower threshold.

Cell leakage mechanisms

To estimate the leakage associated with an array of cells, we first define the dominant leakage mechanisms and

[2] β ratio = width/length of a pull-down n-FET divided by the width/length of a wordline n-FET.

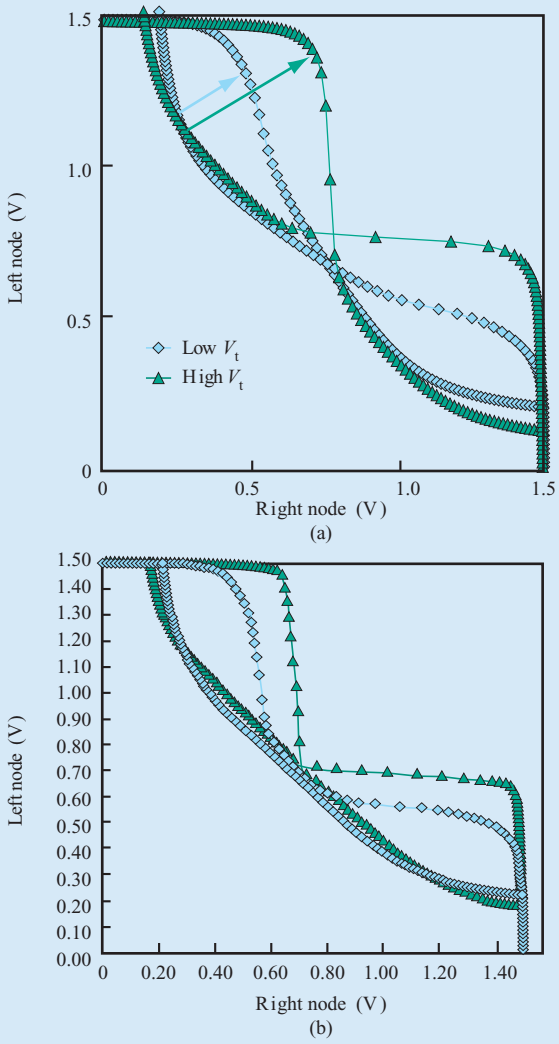

Figure 2

SRAM cell stability: (a) Measured butterfly curves on 0.18-μm technology cell with high-performance V_t and ULP V_t (±0.79 V). (b) Curves for the same cell, simulated using SPICE. Reprinted with permission from [18]; © 2002 IEEE.

critical paths within the cell. **Figure 3** shows schematically the significant parametric cell leakage paths and mechanisms operating in the 6T SRAM. By accounting for each leakage mechanism and resolving the leakage to the given cell dimensions, the total cell and/or array leakage can be calculated effectively, and the expected array leakage can be estimated adequately. In Figure 3, for the arbitrary state chosen, the internal node on the left side of the latch is maintained at ground while the node on the right is held at V_{DD} by the operation of the cross-coupled latch. The intent of this section is to describe briefly the critical parametric leakage sources within the cell derived

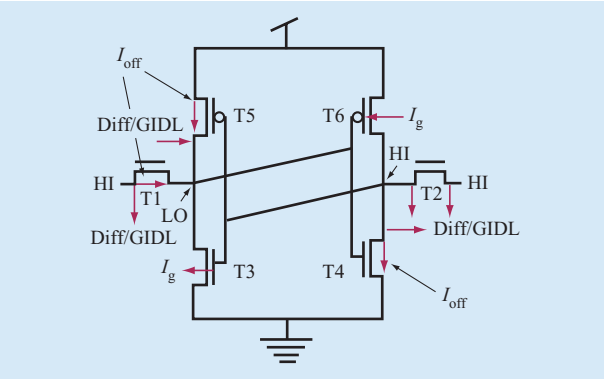

Figure 3

Schematic of leakage paths in a six-transistor SRAM cell on bulk silicon. HI = supply voltage (V_{DD}); LO = ground; Diff = diffusion leakage.

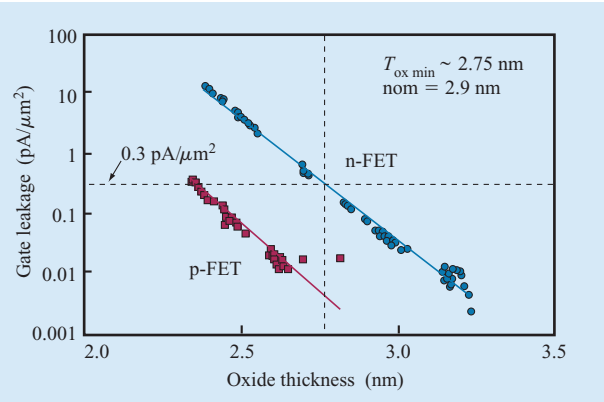

Figure 4

Measured gate-oxide tunneling current as a function of oxide thickness for both n-FET and p-FET.

from this latched configuration corresponding to memory array standby mode. Although the schematic in Figure 3 shows the gate leakage to substrate for transistor T3 and to the n-well for T6, it should be pointed out that the majority of the carriers are swept to the source nodes by the applied fields.

In the following paragraphs, we review the critical parametric leakage mechanisms operating within the SRAM cell and describe how the mechanism was addressed in the described ULP technology. The five dominant parametric mechanisms to be addressed are threshold voltage optimization, gate tunneling leakage, subthreshold leakage, reverse-bias diffusion leakage, and gate-induced drain leakage (GIDL). Of these mechanisms, most of the development effort was devoted to threshold voltage optimization and GIDL reduction.

Gate leakage

The gate oxide in the array was set at 2.9 ± 0.15 nm to reduce the electrical leakage associated with quantum-mechanical tunneling in the n-FET below 0.3 pA/μm. **Figure 4** shows the measured tunneling current through the gate dielectric as a function of oxide thickness for n-FET and p-FET devices. Gate-oxide tunneling leakage is observed to be roughly 1.5 orders of magnitude higher for the n-FET at the thickness and voltage conditions of interest. The gate leakage can become a significant contributor to the room-temperature cell leakage at thicknesses below 2.7 nm. For the arbitrary latched state chosen for Figure 4, the gate tunneling leakage mechanism is active for the n-FET (T3) and p-FET (T6) sites shown in Figure 3. For the purpose described in this paper, the leakage is generally found to be adequately modeled for a given voltage as a function of gate-oxide thickness from the empirical relationship

$$I_g(t_{ox}) = A_0 \exp(-B_0 t_{ox}) \quad (1)$$

for both n-FETs and p-FETs. Because this mechanism is governed by quantum-mechanical tunneling, this mechanism is virtually temperature-independent; while other leakage mechanisms dominate at higher temperatures, this mechanism was found to establish the minimum gate-oxide thickness for the technology on the basis of the established lower-temperature leakage targets. The values obtained for the constant A_0 from Equation (1) are 3.7×10^{10} pA/μm^2 for the n-FET and 3×10^9 pA/μm^2 for the p-FET. The constant B_0 was determined by least-squares fit to be (9.2/nm) for the n-FET and (9.9/nm) for the p-FET.

V_t and subthreshold leakage

The *I–V* characteristics with V_{ds} at 1.5 V taken on a structure with multiple 0.2-μm-wide devices in parallel for the n-FET and p-FET are shown at 25°C and 85°C in **Figures 5(a)** and **5(b)**, respectively. For the narrow-width devices used in the SRAM cell, the off-current of the device is elevated compared with that of a wide device because of the narrow-channel effect (NCE). The effective reduction in V_t associated with geometric constraints of the narrow channel is a significant challenge for future ULP technologies. In the example shown, the I_{source} at zero gate bias is below 10 fA/μm at room temperature and below 600 fA/μm at 85°C for both n-FET and p-FET devices. At 25°C it is clear that the drain current at room temperature is dominated by GIDL. Unlike gate-oxide tunneling leakage, subthreshold device off-current leakage is strongly temperature-dependent and is typically the

dominant leakage mechanism at higher temperatures. Figure 3 shows three transistors in which this mechanism is actively contributing to the standby leakage when the SRAM array is in the standby state. In the example given in Figure 4, the internal node transistors T4 (n-FET) and T5 (p-FET) and the wordline transistor T1 (n-FET) are being held in the off state and have a drain-to-source voltage of V_{DD}. Since it is most common for the bitlines to be held high (at V_{DD}) in standby mode, this is the mode shown for the sake of discussion. However, it is worth pointing out that if the bitlines were held low (at ground), there would still be three devices in the cell contributing to the off-state leakage, since the internal nodes of the SRAM cell are held in opposite states. The off-state leakage can be adequately characterized given the subthreshold slope parameter (B_1), an extracted parameter (A_1) and threshold voltage (V_t) for both the n-FET and the p-FET with the following relationship:

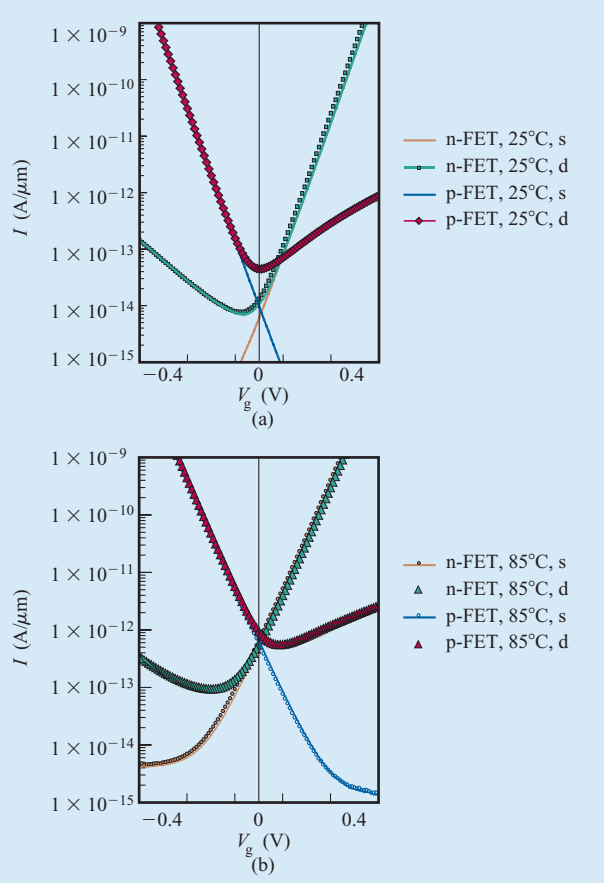

Figure 5

ULP subthreshold characteristics of the n-FET and p-FET at (a) 25°C and (b) 85°C (s = source, d = drain).

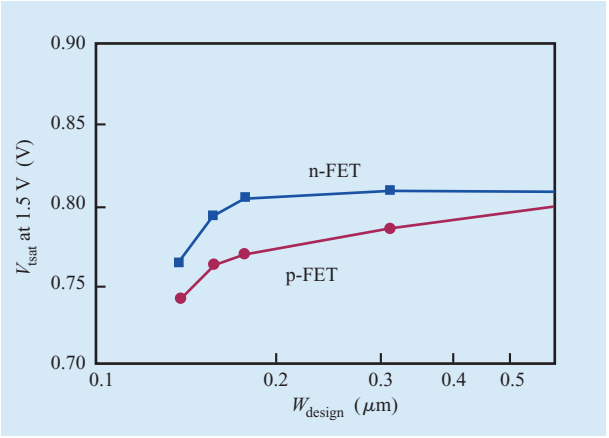

Figure 6

Measured narrow-channel effect for n-FET and p-FET. Saturated threshold voltage (V_{tsat}) as a function of device drawn width (W_{design}). Note: the actual width may be slightly different from the drawn or as-designed width due to normal process bias and tolerances.

$$I_{off}(V_t, T) = C(T)A_1 \exp(B_1 V_t), \quad (2)$$

where $C(T)$ is expressed as

$$C(T) = 10^{(V_t/S)-[V_t-(T-298)\gamma/(T/298)S]}, \quad (3)$$

where S is the subthreshold slope, γ is the slope of the V_t as a function of temperature, and T is the temperature in degrees Kelvin. Because of the obvious importance of V_t control for both array leakage and cell stability, two additional topics which relate to V_t control must be addressed for ULP technologies. These include the effect of device width on V_t, referred to as narrow-channel effect (NCE) [19, 20] and the treatment of statistical variations in V_t in narrow devices [21]. Both of these factors become increasingly important for the 0.13-μm node and below. The NCE as shown in **Figure 6** is a significant factor for the 2.34-μm^2 SRAM cell, since the device widths are between 0.16 μm and 0.22 μm. The narrow-channel V_t roll-off, or NCE, can result in an increase in the cell standby current below an active width of 0.20 μm for the n-FET and 0.4 μm for the p-FET. Simulations from the TSUPREM-4 program (**Figure 7**) indicate significant boron segregation into the STI oxide for narrow-channel n-FET devices. While this explanation is generally accepted for the n-FET, no complete explanation is currently proposed for the observed NCE in the ULP p-FET device. The observed p-FET behavior appears to be unique to the ULP technologies, since for high-performance devices the p-FET NCE typically results in a slightly higher V_t with narrower channels. As a result of this phenomenon, the threshold voltages must be

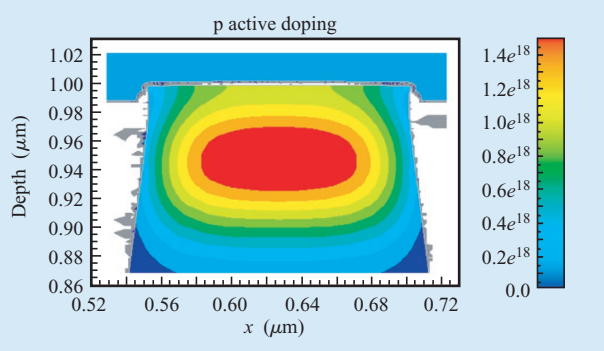

Figure 7

TSUPREM-4 model of boron segregation at the corner of a narrow n-FET.

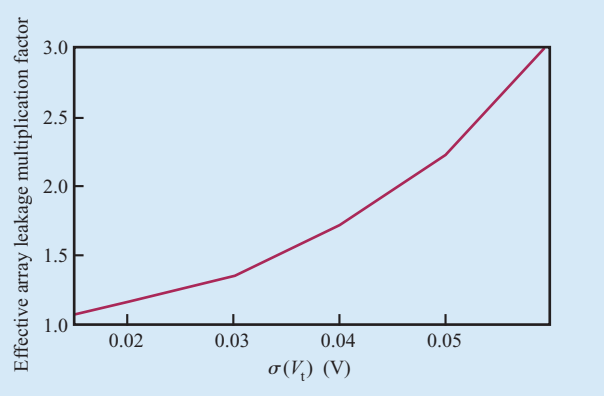

Figure 8

Calculated n-FET device leakage increase as a function of $\sigma(V_t)$ for a large array.

set higher than one might assume on the basis of the measured wide device off-current in order to achieve the cell leakage targets.

It is well known that the statistical variation in V_t will become an increasing concern as devices continue to scale [22, 23]. This is due not only to the physical dimension tolerances but also to statistical variations in channel dopant associated with the reduction in channel area. This variation can be compounded in the SRAM cell by V_t variations associated with overlay tolerances and corner-rounding effects due to aggressive scaling to achieve maximum density for the cell. Because of the exponential relationship of I_{off} with V_t, the contribution of the devices in the array with lower threshold voltage must be accounted for in calculating the overall array leakage. The array leakage increase associated with the variation in the standard deviation of V_t, i.e., $\sigma(V_t)$, can be estimated by means of the following equation:

$$I_{ddx}[V_{td}, \sigma(V_t)] = \frac{\int_{V_{t1}}^{V_{t2}} \frac{1}{\sqrt{2\pi}\sigma(V_t)} e^{\{[-1/2\sigma(V_t)^2](V_{td}-\bar{V}_t)^2\}} [A_1 e^{(-B_1 V_{td})}]\, dV_{td}}{A_1 e^{(-B_1 \bar{V}_t)}}, \quad (4)$$

where $\bar{V}_t$ is the V_t mean, V_{td} is the device V_t, and A_1, B_1 are defined in Equation (2).

Figure 8 shows the calculated array leakage contribution of the n-FET as a function of $\sigma(V_t)$ assuming a normal distribution function. This effect becomes significant for the array when the $\sigma(V_t)$ becomes larger than 30 mV and becomes a factor of 2 for a $\sigma(V_t)$ of 50 mV. This fundamental phenomenon poses a significant concern as device widths continue to scale and the dimensions of the SRAM cell are further reduced. Also, it should be noted that the increase in $\sigma(V_t)$ accompanying aggressive scaling may prove to be a significant limit for cell performance and SNM.

Diffusion leakage

Although diffusion leakage (I_{diff}) did not pose a significant technical challenge for the ULP technology leakage goals, some experimental optimization was required to reach them. Reverse-bias diffusion leakage (RBDL) is a function of defect population within the depletion region and the local stresses arising from sources such as STI processing parameters and silicide processing [24]. This leakage can be characterized as

$$I_{diff} = A_2 \exp(E_a/k_T), \quad (5)$$

where E_a is roughly equal to $E_g/2$ in the typical junction environment, and A_2 is defined as

$$A_2 = T^{3/2} V^{1/2}. \quad (6)$$

The diffusion leakage was minimized by optimizing the source/drain energy so that the junction depth was deep enough to avoid silicide defects. The relationship between the deep p-well retrograde implant and area diffusion leakage resulted in a reduction of the deep retrograde implant dose for the ULP technology. The TEM image (**Figure 9**) shows the type of silicon defects found to be associated with a ^{11}B implant dose greater than 1×10^{14} at/cm^2. This defect is associated with the end of the range damage region and is characterized by an extended dislocation loop. With sufficient stress during subsequent process steps, these dislocations glide up into the active silicon regions near the silicon surface, causing defect-related leakage particularly in the large-area diffusion capacitors. These defects were found to correlate to an increase in the large-area n+ diffusion

leakage and were completely eliminated when the ^{11}B dose was reduced by a factor of 10. **Figure 10** shows the reverse-bias leakage characteristics from samples with and without this higher-dose p-well retrograde implant. The retrograde well boron doping concentration was established such that no elevated diffusion leakage contribution from this mechanism was observed for the technology.

Gate-induced drain leakage (GIDL)

The process and device learning required to achieve the ULP technology leakage goals associated with GIDL were significant, because the SRAM array contains a relatively large critical area subject to this mechanism. GIDL and RBDL mechanisms contribute to the cell leakage on both the internal node and bitline contact regions of the SRAM cell when the bitlines are held at a high voltage (V_{DD}) during standby mode. Referring again to Figure 3, the gate perimeter associated with the drain of transistors T2, T4 (n-FETs) and T5 (p-FET) contributes GIDL in standby mode. Additionally, because we assume that the bitlines are to be held at a high voltage (V_{DD}) in standby mode, these mechanisms are also contributing on the bitline side of both wordline transistors T1 (n-FET) and T2 (n-FET). For the lightly doped drain (LDD) type of structure, GIDL has been shown to be dominated by band-to-band tunneling in the gate–drain overlap region. A 2D analytical model found to adequately describe the physics of the GIDL mechanism is presented in Reference [25].

This leakage mechanism is influenced by many processing parameters such as sidewall oxidation, t_{ox}, spacer width, LDD, silicidation, and halo dopant concentration gradients, depth, and placement. Band-to-band tunneling, trap-assisted tunneling, and interface-state-assisted tunneling may be contributing factors to the overall GIDL observed. Because the gate-bounded leakage is known to be influenced by many processing parameters, more learning with respect to these elements is clearly critical to obtaining ultralow-leakage CMOS. Although more heavily doped extension [26] and halo implants are beneficial for performance, the increased field accompanying that drain design results in an increased GIDL in both n-FETs and p-FETs. Band-to-band tunneling (BBT) has a weak temperature dependence and dominates at higher voltages, while band-to-defect tunneling (BDT) has a stronger temperature dependence and dominates at lower biases. High-performance designs tend to have higher fields, which increases the BBT component of GIDL. Defects and interface states are also generated with these higher-dose implants, increasing the BDT component. The ULP device design goal was to reduce GIDL by minimizing the field at the drain edge and at the same time retaining optimum short-channel effect (SCE) control and low series resistance.

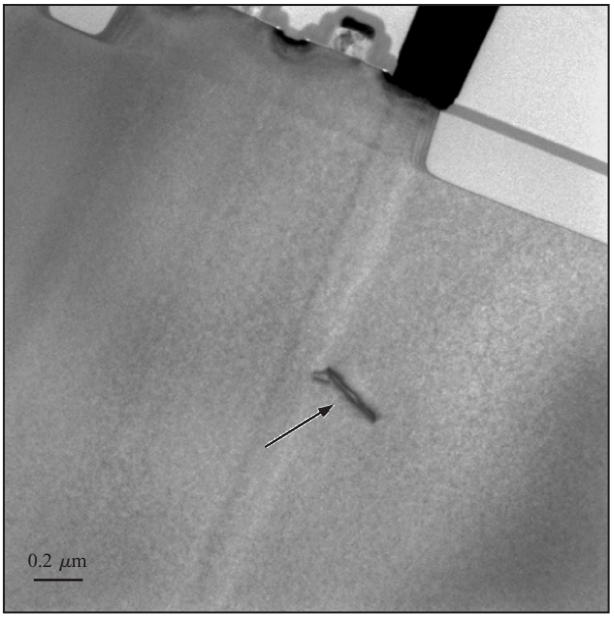

Figure 9

TEM cross-section image showing a silicon defect associated with a high-energy ^{11}B implant in the range of 1 to 5 × 10^{14} atoms/cm^2.

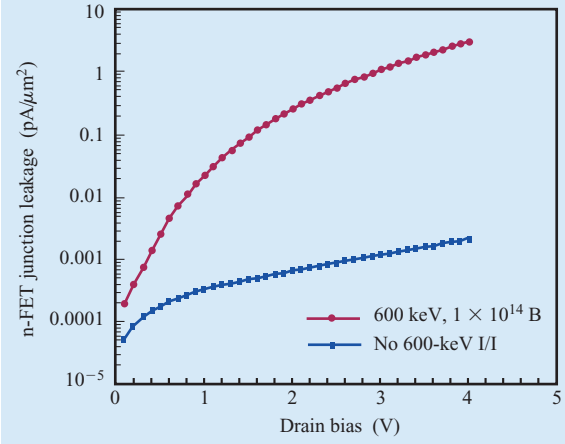

Figure 10

Reverse-bias n+ diffusion leakage measurements with and without the 600-keV ^{11}B implant.

Figure 11(a) shows n-FET GIDL as a function of drain bias for various process experiments. The first process experiment is plotted as blue squares (Curve 1) and would be more consistent with the higher-performance design point, with a high-dose arsenic extension and a highly doped halo comprising indium and boron. The indium

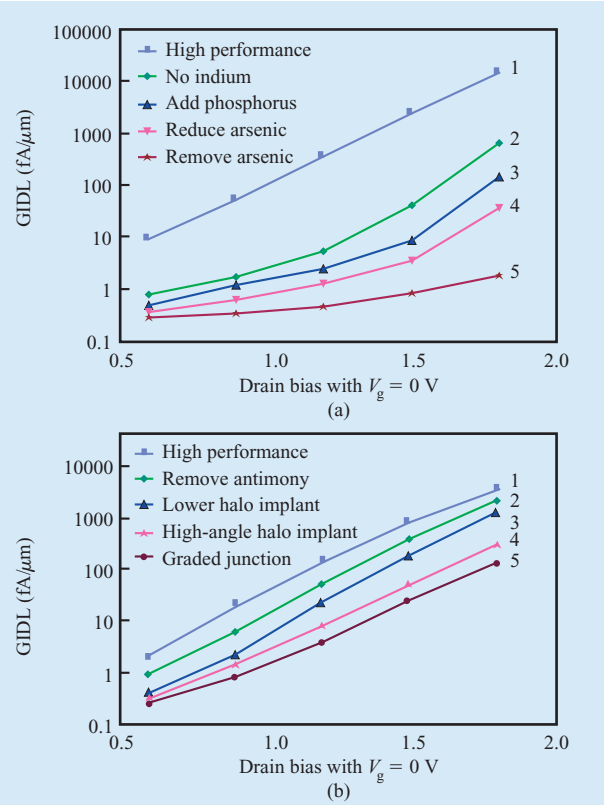

Figure 11

GIDL as a function of drain bias for various halo and extension implant experiments: (a) for n-FET; (b) for p-FET.

was removed from the halo, as indicated by the green diamonds (Curve 2), resulting in roughly an order of magnitude reduction in GIDL. Curve 3 (navy triangles) shows further reduction in GIDL, with phosphorus added to the extension and an increased implant angle for the boron halo. The arsenic extension dose was reduced further, as shown by Curve 4 (pink inverted triangles). The data points along the fifth curve (brown stars) exhibit the lowest amount of GIDL, with arsenic completely eliminated from the extension (phosphorus extension and a high implant tilt angle for the boron halo). It is clearly demonstrated that, by tailoring the halo and extensions, both the magnitude and the drain-bias-dependent slope can be significantly reduced for the n-FET.

The process experiment consistent with the higher-performance wafer containing indium in the halo showed a very weak gate-bias dependence, which suggests that the leakage is occurring deeper in the extension region, below the influence of the gate-induced surface potential. As the n-FET junction was graded further (n-FET GIDL curves 2–5), the gate-bias dependence decreased and the temperature dependence increased, suggesting reduced BBT and increased BDT components. The phosphorus-only extension (Curve 5) had a temperature dependence consistent with a mid-gap generation trap (E_a = 0.56 eV at V_d = 1.0 V) and had a very small BBT component, as indicated by a weak drain-bias dependence. A phosphorus-only extension produced optimum GIDL results, but this design point was not selected for the ULP technology because it also exhibited higher series resistance and was found to show prompt-shift under hot-carrier stress.

Figure 11(b) shows the p-FET GIDL as a function of drain bias for various process experiments conducted. The data corresponding to Curve 1 (blue squares) exhibits the characteristics of the higher-performance design point, with Sb as the V_t adjust implant, a high-dose BF_2 extension, and a highly doped As halo. The results indicated by Curve 2 (green diamonds) resulted when Sb was removed and the boron halo dose was reduced. Still further reduction in GIDL was obtained with a reduced BF_2 halo, as shown by Curve 3 (navy triangles). An increased halo implant angle along with a small dose reduction resulted in the behavior modeled by Curve 4 (pink inverted triangles). A reduced extension dose and increased energy to grade the junction, coupled with the higher halo implant angle, produced Curve 5 (brown circles). In general, the p-FET experiments showed less improvement in GIDL with junction grading than the n-FET experiments. The drain bias dependence for the p-FETs remained high even for low bias levels, and the gate bias dependence is significantly higher than for the n-FETs.

The higher-performance p-FET device experimental process, like its n-FET counterpart, showed a very weak gate-bias dependence. This could be explained by the fact that the Sb well implant produces a super-steep retrograde (SSR) well profile that increases the field deeper in the silicon, below the gate bias control. In contrast to the n-FET, there was little change in the temperature or bias voltage dependence for the p-FET as the junction was graded further (Curves 2–5). In general, the magnitude of the p-FET bias dependence (gate and drain) was greater than that of the n-FET, and the total reduction in GIDL across the experiments was less (a reduction of about three orders of magnitude) for the n-FET compared with a reduction of less than two orders of magnitude for the p-FET.

A surprising observation made during the course of this work was that GIDL was found to exhibit a geometric dependence and to be dependent upon the device width for n-FET and p-FET. The n-FET GIDL was found to increase by ~3× with reduced channel width, while the p-FET increased by 1.5–2×. GIDL is plotted in **Figure 12** as a function of channel width, showing the increase that must be taken into account for the narrow devices in the SRAM cell. Although the precise mechanism for this effect is not completely apparent, it is speculated that

the silicon stress associated with the STI boundary is influencing the dopant diffusion such that the effective electric field is higher near the STI boundaries. As in the case of NCE, this observation results in an increased challenge in scaling the ULP technologies to deep-submicron design nodes.

n+/p+ leakage

Punchthrough leakage associated with n+/p+ space is primarily a function of both the well doping concentration and profile and the STI depth. This leakage mechanism is characterized as a function of n+ to n-well and p+ to p-well space. For voltages beyond punchthrough voltage, the current increases exponentially with applied voltage as the barrier is lowered at the emitter side.

The n+ to n-well and p+ to p-well leakage must be kept very low for ULP applications. The contribution in leakage on a per-cell basis is less than 1 fA/μm across the voltage range of interest down to a spacing of 0.18 μm for n+ to n-well and p+ to p-well. To resolve this leakage to the cell level, one must determine the fraction of the cell width for which this leakage can occur. For the cell design as shown in Figure 1, this factor is approximately one half the total cell width. This is because, for the high internal node, the n+ diffusion to the adjacent n-well region, which is held at a high voltage (V_{DD}), and conversely, the p+ diffusion to the adjacent p-well region, which is held at a low potential (ground) by the latch operation, are at held the same potential during standby.

Array leakage

To measure the SRAM array leakage and better understand the impacts of various process conditions on the array standby power, an array leakage monitor (ALM) was designed. One of the unique advantages of the ALM was that all of the support circuitry associated with the SRAM addressing and read/write operations could be eliminated. This method for characterizing the array leakage was found to provide a greater degree of flexibility in analyzing the sources of leakage in the array than a standard functional array. The ALM contained an array of cells electrically connected in parallel with the V_{DD}, ground, bitline (BL) true, BL complement, and the wordline (WL) wired out to pads. With power supplied to the array, the bitlines held high, and the wordline held low, the sum of all leakage mechanisms active in the SRAM cell could be measured. Measurements were made at 1.2 V and 1.5 V for 25°C and 85°C.

The cell leakage as measured with the ALM was successfully predicted using device measurements taken at the first metal level. The method used as shown in **Table 2** was to sum columns at 25°C or 85°C to account for the total array leakage at these respective temperatures. The

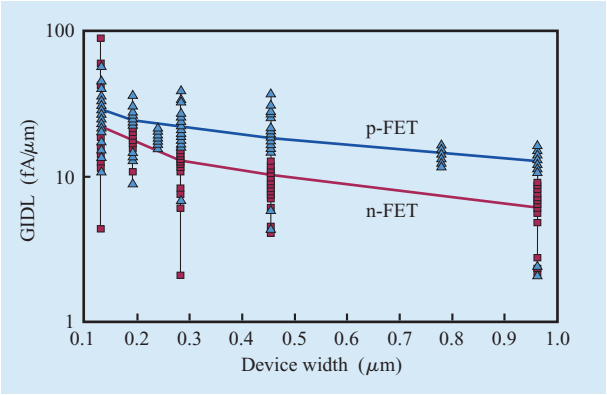

Figure 12

Measured narrow-channel-width effect on GIDL for n-FET (squares) and p-FET (triangles). GIDL increases as channel width is reduced for both devices.

Table 2 Procedure for calculating SRAM array leakage at 25°C and 85°C.

Leakage mechanism	*Leakage determination*	*Leakage per cell*	*Array*	
			25°C	*85°C*
WL n-FET I_{off}	Eq. (2)	W_{WL}	No. of cells × Eq. (4)	$C(T)$
PD n-FET I_{off}	Eq. (2)	W_{PD}	No. of cells × Eq. (4)	$C(T)$
PU p-FET I_{off}	Eq. (2)	W_{PU}	No. of cells × Eq. (4)	$C(T)$
n-FET I_g	Eq. (1)	$W_{PD} \times L_{PD}$	No. of cells	$I_g(T)$
p-FET I_g	Eq. (1)	$W_{PU} \times L_{PU}$	No. of cells	$I_g(T)$
n-FET I_{gidl}	Measurement	$3W_{WL} + W_{PD}$	No. of cells	$I_{gidl}n(T)$
p-FET I_{gidl}	Measurement	W_{PU}	No. of cells	$I_{gidl}p(T)$
n-FET I_{rbdl}	Measurement	$A_{BL} \times A_{PD}$	No. of cells	$I_{diff}n(T)$
p-FET I_{rbdl}	Measurement	A_{PU}	No. of cells	$I_{diff}p(T)$
n+/n-well current	Measurement	$R_{cell} \times W_{cell}$	No. of cells	$Rn(T)$
p+/p-well current	Measurement	$R_{cell} \times W_{cell}$	No. of cells	$Rp(T)$

W = width; L = length; A = area; R = resistance; WL = wordline; BL = bitline; PD = pull-down; PU = pull-up; g = gate; gidl = gate-induced drain leakage; rbdl = reverse-bias diffusion leakage; diff = diffusion

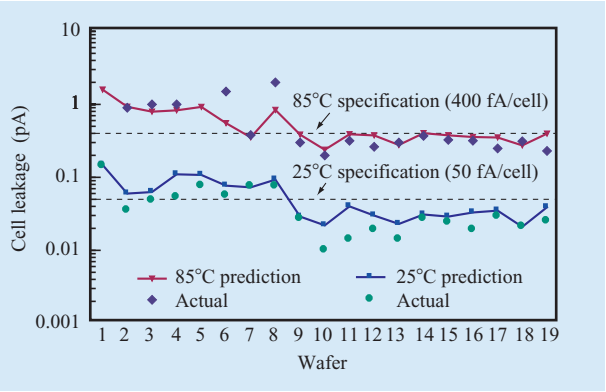

Figure 13

Prediction of array leakage as a function of the mean of the measured total array leakage at 25°C and 85°C at 1.5 V across a range of hardware. Wafers more recently measured reflect the learning described in this paper.

correlation between the predicted and measured values using this straightforward approach was considered adequate. By resolving the various leakage components to the cell dimensions and summing the components of cell leakage obtained at the first metal level, an understanding of the dominant leakage mechanisms can be obtained. The calculated leakage components using the method outlined in Table 2 are shown in **Figure 13** along with the measured array values.

Summary

An industry-leading, low-cost, ultralow-standby-power technology has been developed for foundry applications requiring low-power standalone or embedded SRAM in 0.18-μm and 0.13-μm lithography nodes. Because the ULP technology leakage goals are roughly three orders of magnitude lower than those for the standard high-performance technology, significant learning was required to achieve the array leakage that was demonstrated. A description of the work required to achieve the GIDL targets has been presented. In addition to the well-known gate-oxide leakage limitations, three unique challenges for future scaled ULP technologies have been described. These include channel-size-dependent threshold voltage variations and channel width dependence on both device threshold (NCE) and GIDL. We believe this to be the first literature account of the dependence of channel width on GIDL.

Key leakage components and paths within the 6T SRAM cell have been identified and evaluated; these include gate tunneling, GIDL, junction leakage, subthreshold leakage, and n+/p+ punchthrough leakage. The components of SRAM cell leakage have been quantified and accounted for in the context of the electrical operation of the cell; when these are resolved to the cell dimensions, good agreement between the measured and predicted leakage is observed. Array leakage consistent with less than 50 fA/cell at 1.5°C, 25°C and less than 400 fA/cell at 1.5 V, 85°C has been demonstrated in both 0.18-μm and 0.13-μm-technology nodes.

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