Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Region

- So far, we have discussed the MOSFET behavior in linear region and saturation region.
- Sub-threshold region is refer to region where $V_t$ is less than $V_t$.
- Sub-threshold region reflects how fast the MOSFET can switch.
Sub-Threshold Region Behavior of Long Channel MOSFET

**Sub-threshold Current**

Observation

- Sub-threshold current has an exponential relationship with $V_{gs}$.
Sub-Threshold Region Behavior of Long Channel MOSFET

**Sub-threshold Current**

- Unlike the strong inversion region, in which the drift current dominates, sub-threshold conduction is dominated by the diffusion conduction mechanism.

- Because $V_g$ is below $V_t$, almost no electrons inverted at the surface, so the surface potential is determined by the depletion region under that gate and has the nearly same value along the channel. Thus, the electric field along the channel direction is approaching zero, which makes almost no drift current.

- Besides, it is also clear from the simulation result of Charge-Sheet Model that diffusion current dominates at sub-threshold region.
Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Current

- Since the sub-threshold current is dominated by diffusion current. Then,

\[ I_{ds}(y) = WD_n \frac{dQ_i}{dy} = \mu_{eff}W \frac{kT}{q} \frac{dQ_i}{dy} \]

- Integrating from \( y=0 \) to \( y=L \)

\[ I_{ds} = \mu_{eff} \frac{W}{L} \frac{kT}{q} \int_{Q_i(0)}^{Q_i(L)} dQ_i = \frac{W}{L} \mu_{eff} \frac{kT}{q} [Q_i(y = L) - Q_i(y = 0)] \]

where, \( Q_i(y=0) \) and \( Q_i(y=L) \) are the inversion charge density at source and drain at sub-threshold region (or weak inversion)

- Recall: from MOS-C part, the inversion charge density at weak inversion

\[ Q_i = \frac{\sqrt{2qN_Ae_{Si}}}{2\sqrt{\psi_S}} kT q e^{q(\psi_S - 2\psi_N)/kT} \]
Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Current

- Then, with source grounded and drain bias of $V_{ds}$, the $Q_i$ source and drain ends of the channel in a MOSFET under weak inversion can be written as follows:

$$Q_i(y = 0) = q \sqrt{2qN_A e_{si}} \frac{\kappa T}{2 \sqrt{\psi_{s0}}} e^{q(\psi_{s0} - \psi_B)/kT}$$

$$= \frac{\gamma C_{ox} \kappa T}{2 \sqrt{\psi_{s0}}} e^{q(\psi_{s0} - \psi_B)/kT}$$

$$Q_i(y = L) = q \sqrt{2qN_A e_{st}} \frac{\kappa T}{2 \sqrt{\psi_{s0}}} e^{q(\psi_{s0} - \psi_B - V_d)/kT}$$

$$= \frac{\gamma C_{ox} \kappa T}{2 \sqrt{\psi_{s0}}} e^{q(\psi_{s0} - \psi_B - V_d)/kT}$$

Here, $\psi_{s0}$ is the surface potential at source end of the channel.

- The drain current can be solved as

$$I_{ds} = \frac{\mu_{eff} W}{2} \frac{C_{ox} \gamma}{L \sqrt{\psi_{s0}}} \left( \frac{kT}{q} \right)^2 e^{q(\psi_{s0} - \psi_B)/kT} \left( 1 - e^{-qV_d/kT} \right)$$
Sub-Thresholnd Region Behavior of Long Channel MOSFET

**Sub-threshold Current**

- Re-arranging the above equation and replacing the $\psi_B$ term, we have

$$I_{ds} = \frac{\mu_{\text{eff}} W}{2L} \frac{C_{ox}}{\sqrt{\psi_{S0}}} \left(\frac{kT}{q}\right)^2 \left(\frac{n_i}{N_A}\right)^2 e^{q \psi_{S0}/kT} \left(1 - e^{-qV_{ds}/kT}\right)$$

- Inside above equation, $\psi_{S0}$ can be calculated as below

$$V_g = V_{fb} + \psi_{S0} + V_{ox} = V_{fb} + \psi_{S0} - \frac{Q_S}{C_{ox}} \approx V_{fb} + \psi_{S0} + \frac{|Q_d|}{C_{ox}}$$

here we assume that $Q_S$=Qd due to weak inversion. Then

$$V_g = V_{fb} + \psi_{S0} + \frac{\sqrt{2e_{Si}qN_A\psi_{S0}}}{C_{ox}}$$

- For each $V_g$, we are able to calculate $\psi_{S0}$, and then drain current $I_{ds}$. 

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Discussion of Sub-threshold Current

Gate voltage dependence

- Sub-threshold current has an exponential relationship with $\psi_{S0}$, which is corresponding to $V_g$, so the sub-threshold current increases exponentially with gate voltage $V_g$. 
Sub-Threshold Region Behavior of Long Channel MOSFET

**Discussion of Sub-threshold Current**

Drain voltage dependence

- Sub-threshold current depends on $V_{ds}$ when $V_{ds}$ is small by
  \[ I_{ds} \propto \left(1 - e^{qV_{ds}/kT}\right) \]

- Sub-threshold current independent with $V_{ds}$ when $V_{ds}$ larger than a few $kT/q$. 

![Graph showing current vs. gate voltage with different $V_{ds}$ values]
**Sub-Threshold Region Behavior of Long Channel MOSFET**

**Sub-threshold Swing (S)**

**Alternating sub-threshold current form:**

- introducing two parameters:
  (i) depletion region capacitance $C_d$
  \[ C_d \equiv \frac{\partial Q_b}{\partial \psi_s} = \gamma \frac{C_{ox}}{(2\sqrt{\psi_s})} \]
  (ii) factor $\eta$:
    as $\psi_s$ is linearly related with $V_{gs}$, we introduce $\eta$ by:
    \[ \psi_s - 2\psi_B = (V_{gs} - V_t)/\eta \]

- physical view of $\eta$:
  capacitive coupling between the gate and silicon surface
  \[ \eta = 1 + \frac{C_d}{C_{ox}} = 1 + \frac{\gamma}{2\sqrt{2\psi_B}} \]

If there is a significant trap density ($C_{it}$: surface state capacitance)

\[ \eta = 1 + \frac{C_{it}}{C_{ox}} + \frac{C_d}{C_{ox}} \]

- sub-threshold current:

\[ I_{ds} = I_{pf} \exp\left[\frac{q(V_{gs}-V_t)}{\eta kT}\right]\left(1 - e^{-qV_{ds}/kT}\right), \ V_{gs}<V_t \]

where, $I_{pf} = \beta \left(\frac{C_d}{C_{ox}}\right)(kT/q)^2 = \beta (\eta-1)(kT/q)^2$, is a pre-factor term.
Sub-Threshold Swing (S)

- Sub-threshold swing is another important device characteristic in the sub-threshold region.
- Defined as the change in the gate voltage \( V_{gs} \) required to reduce sub-threshold current \( I_{ds} \) by one decade.
  \[ S = \frac{dV_{gs}}{d(\log I_{ds})} \]
- After detailed calculation, sub-threshold swing (S)
  \[ S = \eta \frac{kT}{q} \ln 10 \approx 2.3 \frac{kT}{q} \eta \]
- Smaller value of S, better turn-on performance of device.
- Minimum swing \( S_{\text{min}} \) is
  \[ S_{\text{min}} = 2.3 \frac{kT}{q} = 60 \text{ mV/dec} \]
  at 300K when the oxide thickness approaches to zero.
- S is a convenient measure of the importance of the interface traps on device performance.
Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Swing (S)

\[ S = 2.3 \frac{kT}{q} \eta = 2.3 \frac{kT}{q} \left( 1 + \frac{C_d}{C_{ox}} + \frac{C_{it}}{C_{ox}} \right) \]

Key dependences of sub-threshold swing (S)

- Gate oxide thickness
  \( t_{ox} \downarrow \rightarrow C_{ox} \uparrow \rightarrow \eta \downarrow \rightarrow \) sharper sub-threshold

- Substrate doping
  \( N_A \uparrow \rightarrow C_d \uparrow \rightarrow \eta \uparrow \rightarrow \) softer sub-threshold

- Substrate bias
  \( |V_{bs}| \uparrow \rightarrow C_d \downarrow \rightarrow \eta \downarrow \rightarrow \) sharper sub-threshold

- Temperature
  \( T \uparrow \rightarrow \) softer sub-threshold

\( \eta \) reflect electrostatic competition between the top gate and body (bottom gate)
Sub-Threshold Region Behavior of Long Channel MOSFET

**Sub-threshold Swing (S)**

Substrate doping dependence
- Lower substrate doping can have a thicker depletion layer, a lower depletion capacitance, and a smaller S.
- This also reflects that it is easier for the gate electrode to control the lower doping substrate.
Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Swing (S)

Temperature dependence
- At room temperature (300K), the ideal limit of S is 60mV/dec
- Normally, devices always work in a higher temperature ambient due to heat dissipation; the S at higher temperature will be higher than room temperature
- S at low temperature can be lowered down significantly
- This is due to that the sub-threshold drain current vs. gate voltage curve is indeed proportional to 1/T
Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Swing (S)

Substrate bias dependence

- Since the depletion thickness increases when a substrate bias is applied, the sub-threshold swing decreases also

$S_t = 83 \quad S_t = 67 \quad S_t = 63 \text{mV/dec}$
**Sub-Threshold Region Behavior of Long Channel MOSFET**

**Sub-threshold Swing (S)**

Off current

- Sub-threshold region is important since it determines the off current

\[
I_{off} = I_{ds}(V_{gs} = 0V) \approx \mu_{eff} \frac{W}{L} \left( \frac{kT}{q} \right)^2 \exp(-qV_{t}/\eta kT)
\]

- To achieve \( I_{off} \)

  (i) \( L \uparrow \rightarrow \text{Performance} \downarrow \)

  (ii) \( V_{t} \uparrow \rightarrow \text{Performance} \downarrow \)

  (iii) \( \eta \downarrow \rightarrow N_{A} \downarrow \rightarrow \text{“short channel” effect} \uparrow \)

  \[ \rightarrow t_{ox} \downarrow \rightarrow \text{field on gate oxide} \uparrow \rightarrow \text{reliability issue} \]

- \( I_{off} \) is a critical design goal in logic devices since it contributes to DC power dissipation in CMOS
Gate Induced Drain Leakage (GIDL) Current

Observation

- It was observed that the excess drain current exist when gate bias further reduce below $V_t$ and move to negative side, which is called Gate Induced Leakage (GIDL) current.

- The GIDL current dominates at a negative bias of $V_{gs}$ and positive bias of $V_{ds}$. The larger difference between $V_{ds}$ and $V_{gs}$ (i.e., $V_{ds}-V_{gs}$), the higher GIDL current will have.

- Since the GIDL current can generate excessive heat dissipation, it needs to be maintained below some specified value, for example, $10\text{pA/}\mu\text{m}$. 

Sub-Threshold Region Behavior of Long Channel MOSFET
Sub-Threshold Region Behavior of Long Channel MOSFET

Gate Induced Drain Leakage (GIDL) Current

Depletion regions at MOS gated diode

Case (a): $V_{ds}>0$, $V_{gs}>>0$: channel Inversion
Case (b): $V_{ds}>0$, $V_{gs}<0$: channel accumulation
Case (c): $V_{ds}>0$, $V_{gs}<<0$: surface of n+ region is depleted or inverted
Gate Induced Drain Leakage (GIDL) Current

Analysis of GIDL Current

- Tunneling creates electron and hole pairs
- Electron will tunnel through the barrier height and collected by the n+ drain, which positive biased.
- Hole will be collected by substrate since it is grounded
- A lot of mechanisms may involve during the electron tunneling, such as band-to-band direct tunneling, trap assisted tunneling, etc, depending on the biases of Vgs and Vds.

Sub-Threshhold Region Behavior of Long Channel MOSFET

Gate Induced Drain Leakage (GIDL) Current
Analysis of GIDL Current

- For the same $V_{gs}$, higher $V_{ds}$ (more positive) will make the barrier more steeper and cause the tunneling easier to happen, so leads to a higher GIDL current.
- For the same $V_{ds}$, a more negative $V_{gs}$ will also make the barrier more steeper and causes the tunneling easier to happen, so also leads to a higher GIDL current.
- When a lot of impurities are involved in the drain region, more traps will be introduced, make the trap-assisted tunneling easier to happen, and hence a higher GIDL current.
How to reduce GIDL Current

- Increase the oxide thickness $t_{ox}$ to reduce the electric field

- Using LDD (lightly doped drain: LDD) structure to reduce the electric field near the drain side

- Decrease the trap density

- Increase the doping concentration of the drain to decrease the depletion layer width
Beyond Saturation Behavior of Long Channel MOSFET

**Channel Length Modulation (CLM)**

As $V_{ds}$ increase and beyond $V_{dssat}$

- $V_{ds}-V_{dssat} \uparrow \rightarrow$ effective channel length $\downarrow$ (L→L-$\Delta$L) $\rightarrow$ drain current $\uparrow \rightarrow$ no more saturated

![Diagrams illustrating CLM and saturation behavior](image-url)
Beyond Saturation Behavior of Long Channel MOSFET

Channel Length Modulation (CLM)

- Considering CLM, the drain current in saturation region becomes

\[ I_{ds} = \frac{I_{dsat}}{1 - \frac{\Delta L}{L}} \approx I_{dsat} \left( 1 + \frac{\Delta L}{L} \right) \]

- Introducing an empirical relation

\[ 1 + \frac{\Delta L}{L} = 1 + \lambda V_{ds} \]

we can obtain

\[ I_{ds} = I_{dsat} \left( 1 + \lambda V_{ds} \right) \]

where \( \lambda \) is defined as Channel Length Modulation Parameter, representing small influence of drain voltage on drain current.

- The \( \lambda \) can be determined by extrapolating the \( I_{ds}-V_{ds} \) curves backward, as shown in the figure above.
Beyond Saturation Behavior of Long Channel MOSFET

MOSFET Breakdown
- impact of high channel field
  ⇒ high field leads to energetic (hot) electrons
  ⇒ hot electrons cause impact ionization
  ⇒ and leading electrons go to drain and holes go to substrate to form the substrate current

- high E field
- energetic electrons
- impact ionization (E>1.5eV)
- avalanche breakdown
  - substrate current
  - bipolar breakdown
Beyond Saturation Behavior of Long Channel MOSFET

MOSFET Breakdown

- MOSFET breakdown
  ⇒ as $I_{sub}$ flows to the body terminal, a body potential of $I_{sub}R_{sub}$ is developed

⇒ when $I_{sub}R_{sub} < 0.6$ V (the turn-on voltage of a PN junction), the increase in body potential reduces $V_{th}$ (same as applying a body bias) and leading to drain current increase

⇒ when $I_{sub}R_{sub} > 0.6$ V, source/body junction turns on and electrons injected from source to body

⇒ these injected electrons diffuse through the substrate and collected at the reverse biased drain/body junction (in fact, leading parasitic bipolar transistor npn action)

⇒ thus, the maximum drain voltage is limited
Different Types of MOSFET

Classification of MOSFETs

- Enhancement mode
  ⇒ normally off
  ⇒ channel doping is same as substrate doping type
  ⇒ always called inversion mode

- Depletion mode
  ⇒ normally on
  ⇒ channel doping is opposite of the substrate doping type
## Different Types of MOSFET

### Classification of MOSFETs

<table>
<thead>
<tr>
<th>TYPE</th>
<th>CROSS SECTION</th>
<th>OUTPUT CHARACTERISTICS</th>
<th>TRANSFER CHARACTERISTICS</th>
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<tbody>
<tr>
<td>n-CHANNEL ENHANCEMENT</td>
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<tr>
<td>(NORMALLY OFF)</td>
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<td>$I_D$ ( V_G = 4V )</td>
<td>$I_D$ ( -V_Tn )</td>
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<td>n-CHANNEL DEPLETION</td>
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<td>$V_Tn$ ( +V_G )</td>
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<tr>
<td>(NORMALLY ON)</td>
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<tr>
<td>p-CHANNEL ENHANCEMENT</td>
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<td>$-V_D$ ( -V_G = -4V )</td>
<td>$V_D$ ( +V_G )</td>
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<tr>
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<td>$I_D$</td>
</tr>
<tr>
<td>p-CHANNEL DEPLETION</td>
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<td>(NORMALLY ON)</td>
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<td>$I_D$ ( 0 )</td>
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