Summer Public Conference
ORTC 2010 Update Messages

A. Allan, 07/14/10, Rev 8

Summer Update to the 4/3 Italy 2009 ITRS ORTC

1) ORTC Model Proposals to TWGs for TWG Interdependency Preparation for **other** ORTC section features:
   1) **"Beyond CMOS" timing unchanged in 2010** for ERD/ERM early research and transfer to PIDS; **however need for continued discussion about transfer of III/V Gate Material technology in 2011 Renewal**
   2) **Logic "Equivalent Scaling" Roadmap Timing Update underway, and ongoing discussion of alignment of "node" and dimensional Trends for 2011 Renewal**
   3) **New "More than Moore" (MtM) white paper draft review and discussion underway for 2011 ITRS Renewal impact** and added to the ITRS website at www.itrs.net
2) MPU contacted M1
   1) **Unchanged for 2010 [validated by FEP data]**
   2) 2-year cycle trend through 2013
   3) Cross-over DRAM M1 2010/45nm
   4) Smaller 60f^2 SRAM 6t cell Design Factor
   5) Smaller 175f^2 Logic Gate 4t Design Factor
   6) **Proposal** from Taiwan **[2011 Renewal]: Design TWG evaluate 1-year pull-in of M1**
3) DRAM contacted M1
   1) **Unchanged for 2010**: Dimensional M1 half-pitch trends remain unchanged from 2007/08/09 ITRS; new 4f2 Design factor begins 2011
   2) **Proposal [2011 Renewal]: 1-year pull-in of M1 and bits/chip trends; 4f2 push out**
4) Flash Un-contacted Poly
   1) **Unchanged for 2010**: 2yr cycle trend through 2010/32nm; then 3yr cycle and also added "equivalent scaling" bit design:
      1) Inserted 3bits/cell MLC 2009-11; and delayed 4bits/cell (2 companies in production) until 2012
   2) **Proposal [2011 Renewal]: 1-year pull-in of Poly; however 3bits/cell extended to 2018; 4bits/cell delay to 2019**

Italy 4/9 Update to the 12/16 Taiwan 2009 ITRS ORTC (cont.)

5) **Unchanged for 2010 Tables:** MPU GLpr – '08-'09 2-yr flat; Low operating and standby line items track changes

6) **Unchanged for 2010 Tables:** MPU GLph – '08-'09 2-yr flat with equiv. scaling process tradeoffs; Low operating and standby line items track changes

1) Performance targets (speed, power) on track with tradeoffs

7) **Unchanged for 2010 Tables:** MPU Functions/Chip and Chip Size Models

1) Utilized Design TWG Model for Chip Size and Density Model trends – tied to technology cycle timing trends and updated cell design factors
2) ORTC line item OverHead (OH) area model, includes non-active area
3) **ORTC model impact from Taiwan proposal will be evaluated for 2011 Renewal**

8) DRAM Bits/Chip and Chip Size Model **Unchanged for 2010 Tables -** 3-year generation "Moore's Law" doubling cycle;

1) smaller Chip Sizes (<60mm2) with 4f2 design factor included
2) **ORTC model impact updating from PIDS/FEP Survey proposals will be evaluated for 2011 Renewal**

9) Flash Bits/Chip and Chip Size Model **Unchanged for 2010 Tables**

1) 2-year generation "Moore's Law" doubling cycle;
2) growing Chip Sizes after return to 3-year technology cycle
3) **ORTC model impact updating from PIDS/FEP Survey proposals will be evaluated for 2011 Renewal]**

10) IRC 450mm Position: Pilot lines/2012; Production/2014-16 **Unchanged for 2010; also Unchanged:** "double S-curve" graphic in 2009 Executive Summary

1) **450mm Program status and Long-Range IEM v12 Demand Update Scenario was presented by ISMI to IRC for 2011 ITRS Renewal preparation**
2) **ISMI believes the 450mm program is presently on track to meet ITRS Timing**

2009 Unchanged

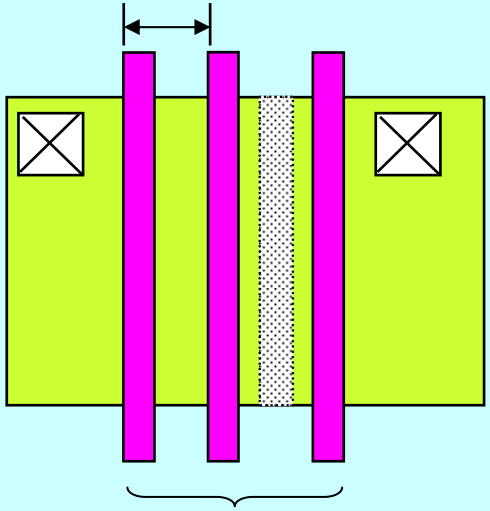
2009 Definition of the Half Pitch – unchanged

[No single-product "node" designation; DRAM half-pitch still litho driver; however, other product technology trends may be drivers on individual TWG tables]

FLASH Poly Silicon ½ Pitch
= Flash Poly Pitch/2

Poly

Pitch



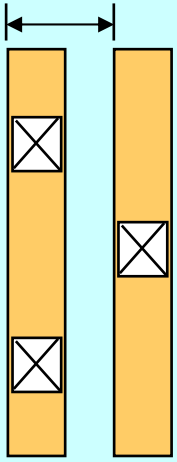
8-16 Lines

Typical flash
Un-contacted Poly

DRAM ½ Pitch
= DRAM Metal Pitch/2
MPU/ASIC M1 ½ Pitch
= MPU/ASIC M1 Pitch/2

Metal

Pitch

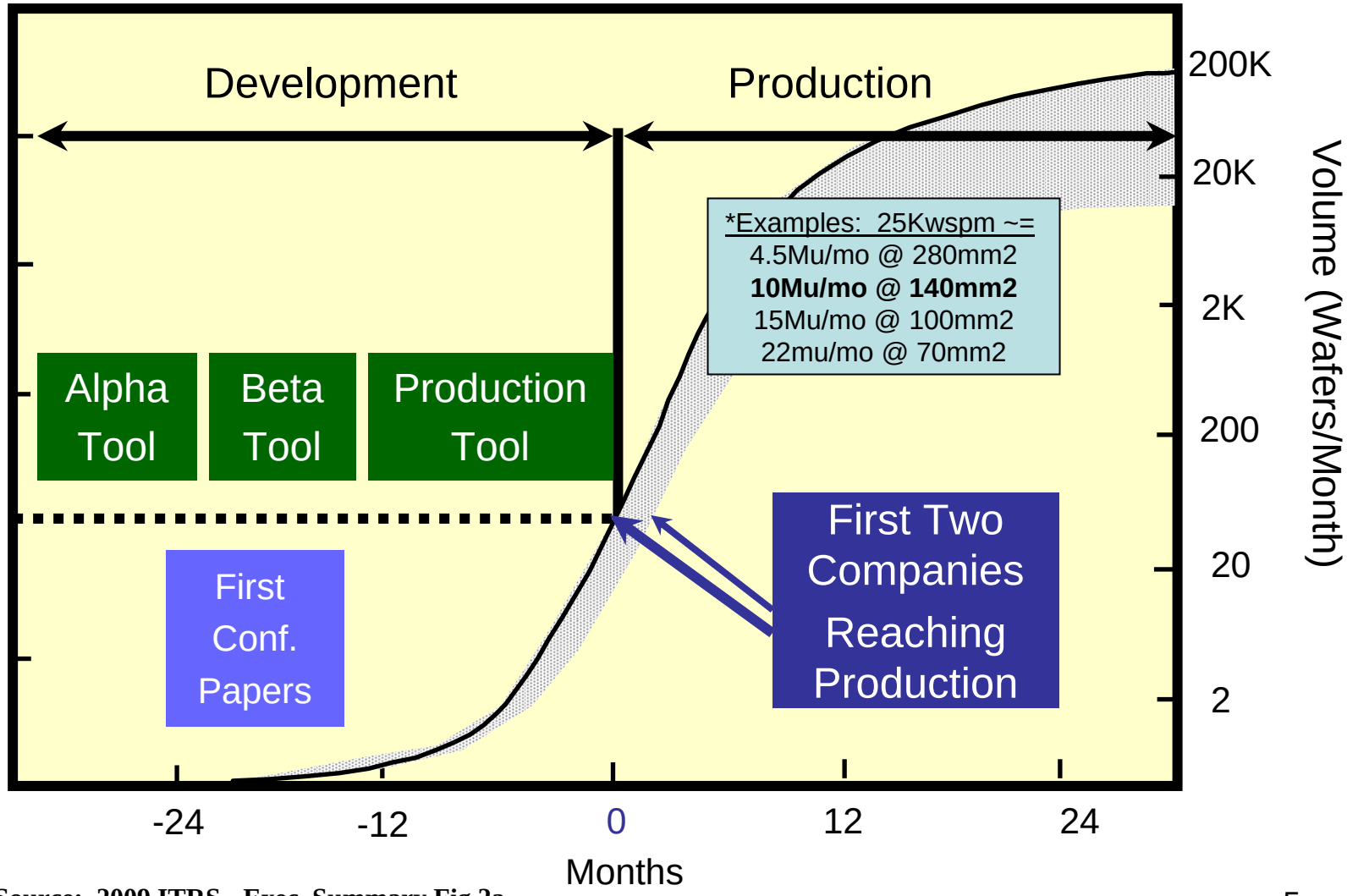


Typical DRAM/MPU/ASIC
Metal Bit Line

Source: 2009 ITRS - Exec. Summary Fig 1

2009 – Unchanged

Production Ramp-up Model and Technology Cycle Timing



Additional Lead-time: ERD/ERM Research and PIDS Transfer

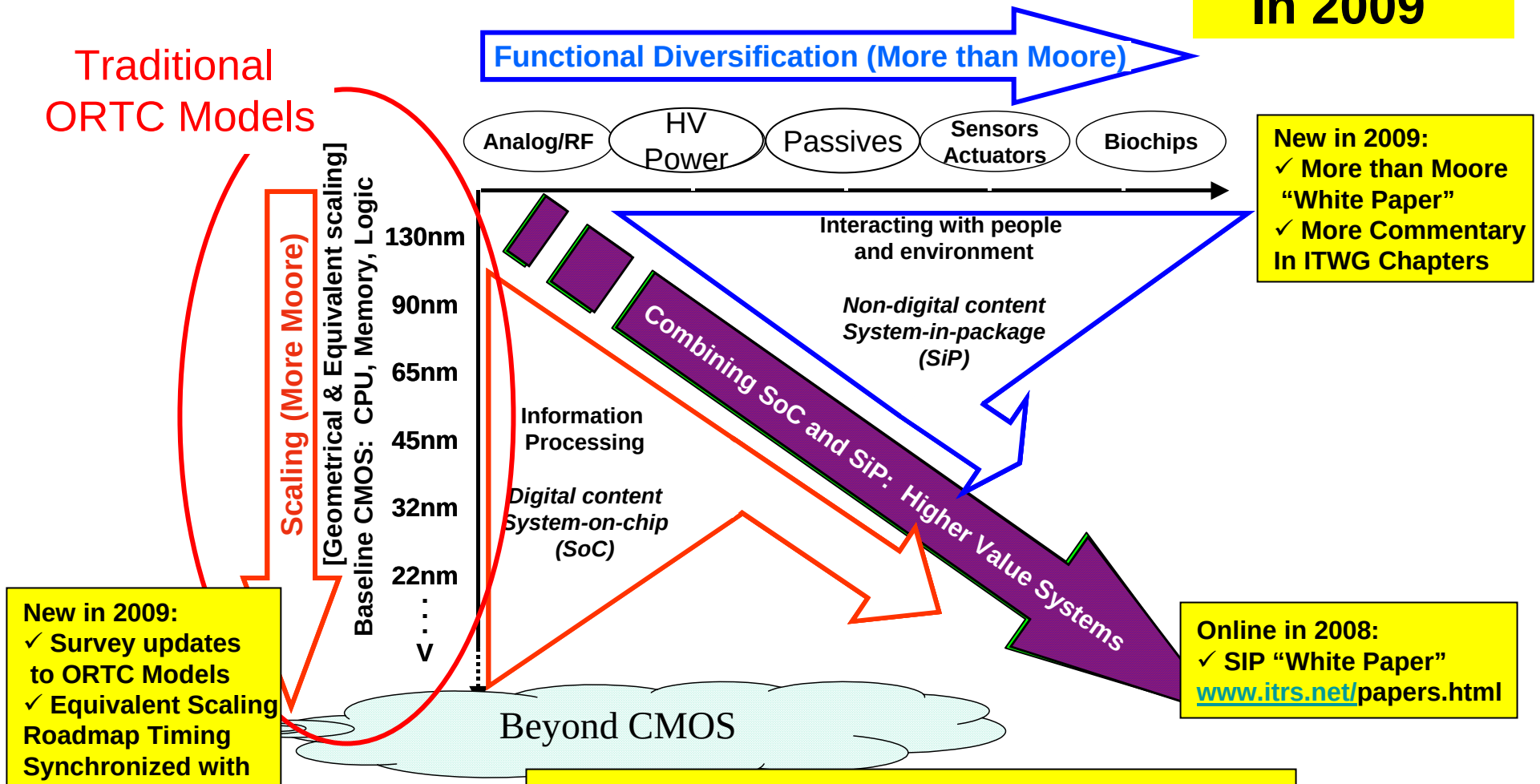
Source: 2009 ITRS - Exec. Summary Fig 2a

2009 WAS

2007 ITRS Executive Summary Fig 4

Moore's Law & More

✓New work In 2009



New in 2009:
✓ More than Moore "White Paper"
✓ More Commentary In ITWG Chapters

Online in 2008:
✓ SIP "White Paper"
www.itrs.net/papers.html

New in 2009:
✓ Survey updates to ORTC Models
✓ Equivalent Scaling Roadmap Timing Synchronized with PIDS and FEP

New in 2009:
✓ Research and PIDS transfer timing clarified
✓ Work underway to identify next storage element

Source: 2009 ITRS - Executive Summary Fig 1

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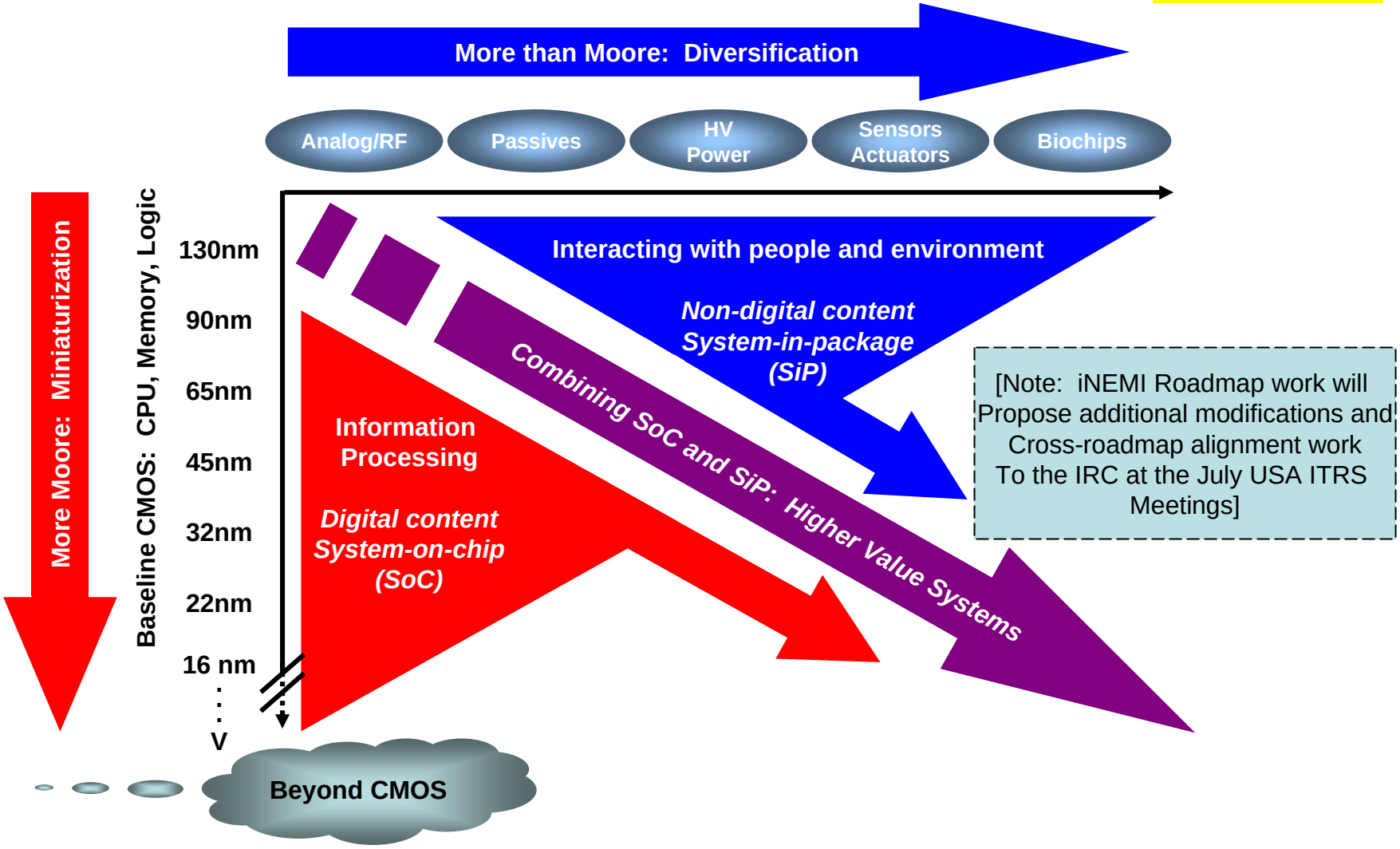
Moore's Law & More

2010 MtM White Paper Update



[Note: iNEMI Roadmap work will Propose additional modifications and Cross-roadmap alignment work To the IRC at the July USA ITRS Meetings]

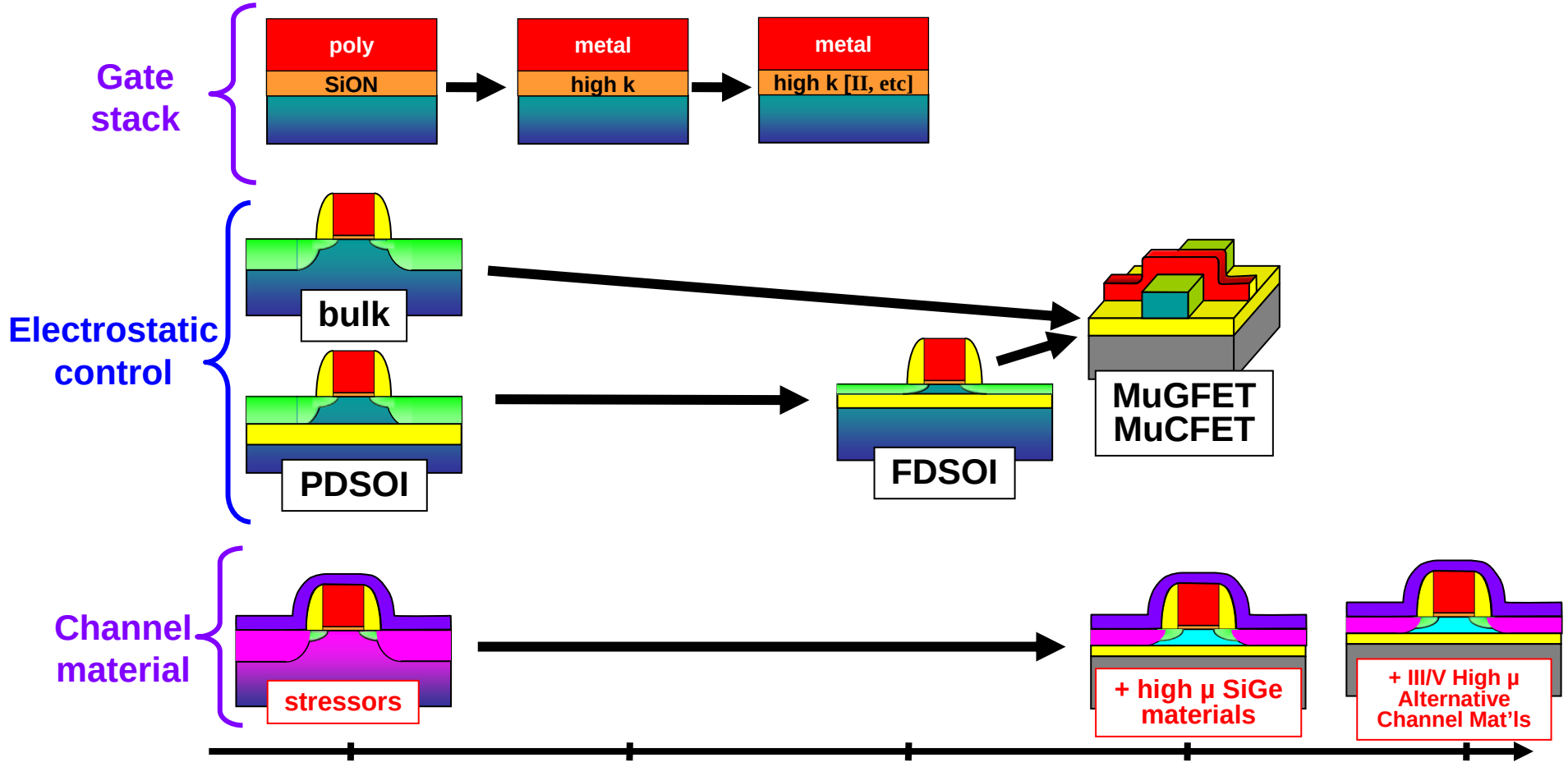
Equivalent Scaling Process Technologies Timing

WAS 2009

Current figure 8c in ITRS executive summary (page 69)

Source: 2009 ITRS - Exec. Summary, Fig 8c, Equivalent Scaling Process Technologies Timing

[Orig. Source: ITRS, European Nanoelectronics Initiative Advisory Council] (ENIAC)

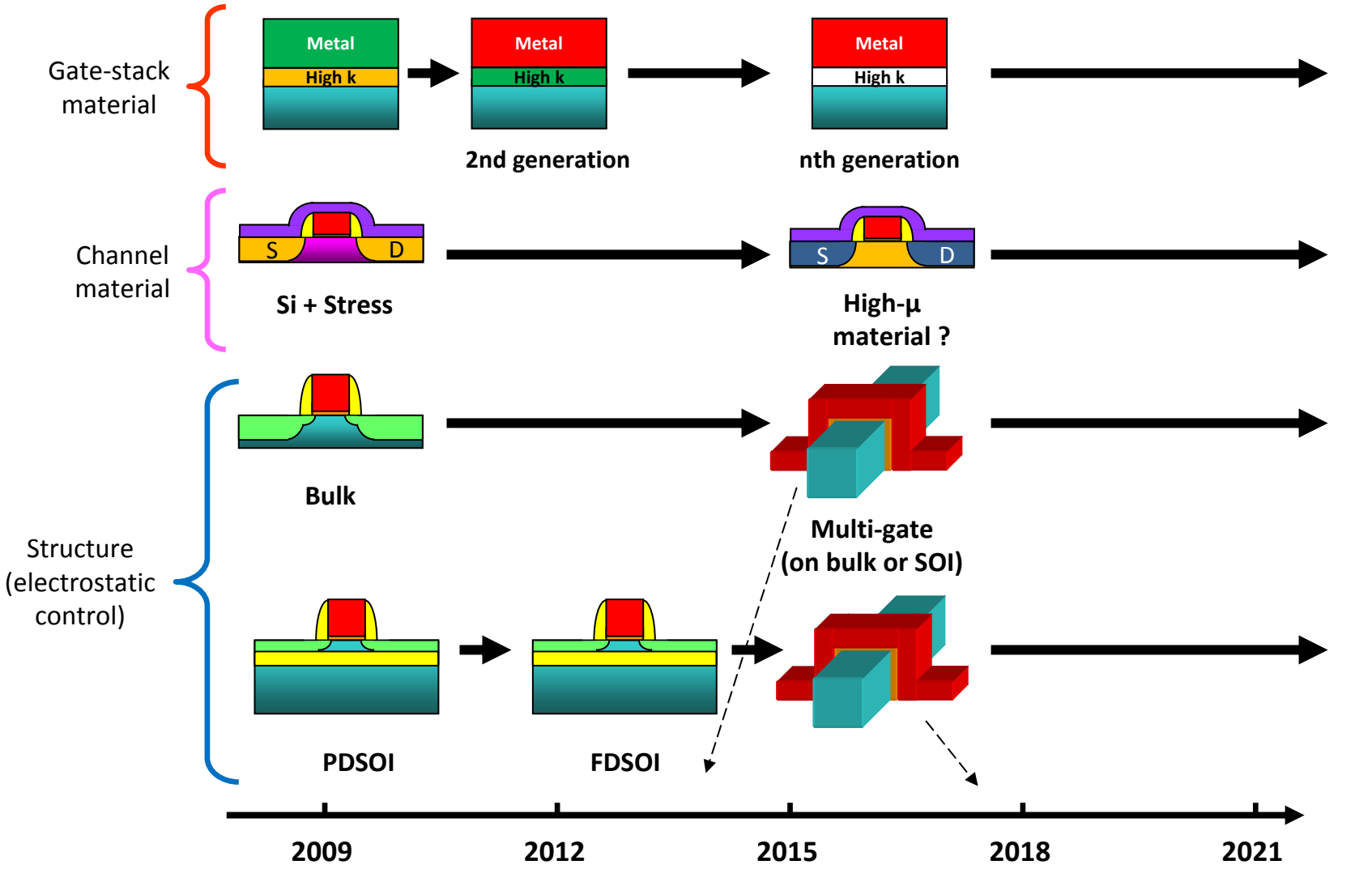


(See also PIDS, FEP, ERD, and ERM chapters' text and tables for additional detail)

Equivalent Scaling Process Technologies Timing

Final Proposal
- for 2011 work

Proposed figure 8c in ITRS executive summary



See also PIDS, FEP, ERD, and ERM chapters' text and tables for additional detail)

= Additional timing movement considerations for 2011 ITRS work

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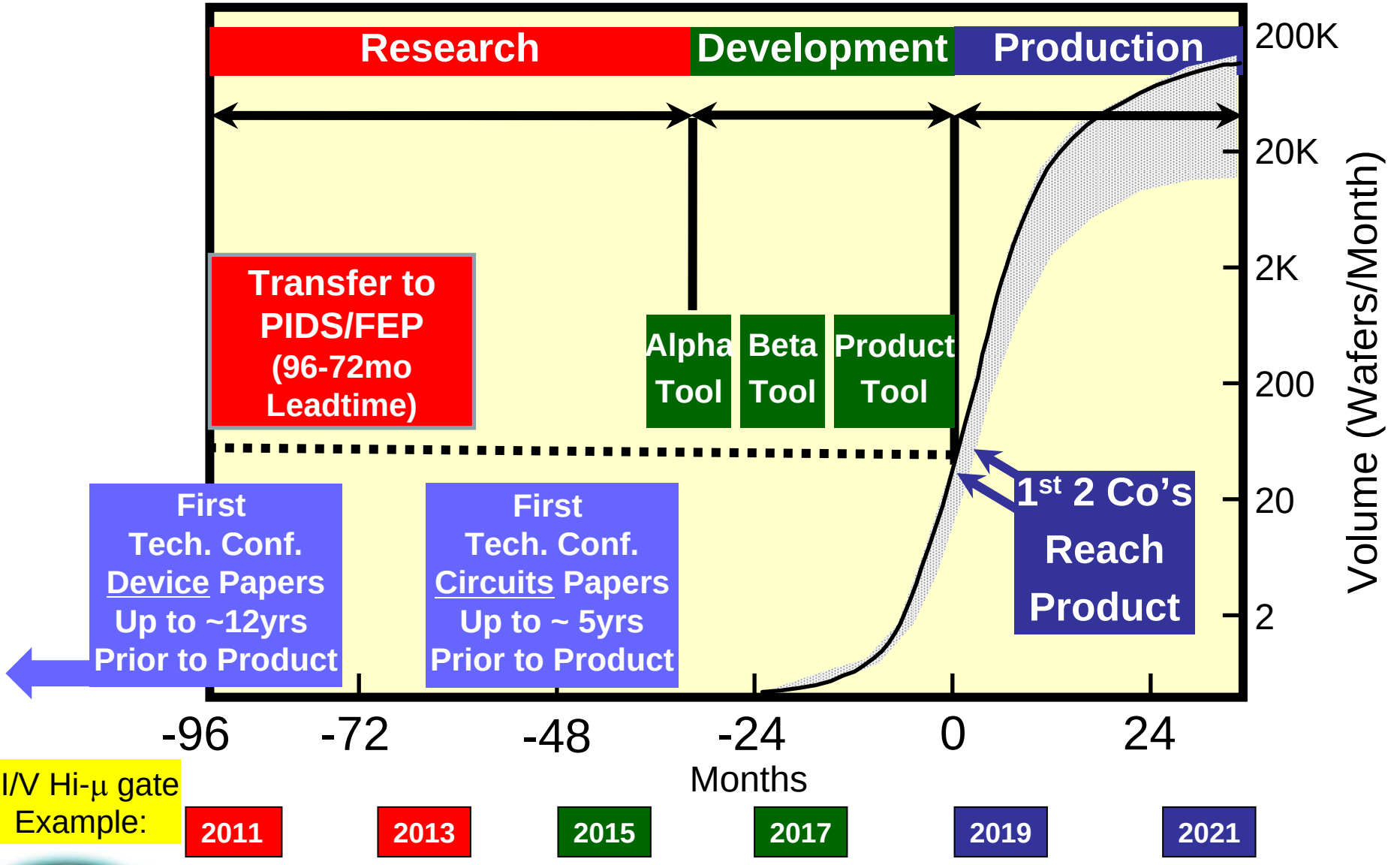
ERD/ERM Long-Range R&D and PIDS Transfer Timing Model Technology Cycle Timing

[Example: III-V MOSFET High-mobility Channel Replacement Materials]

2009 Unchanged

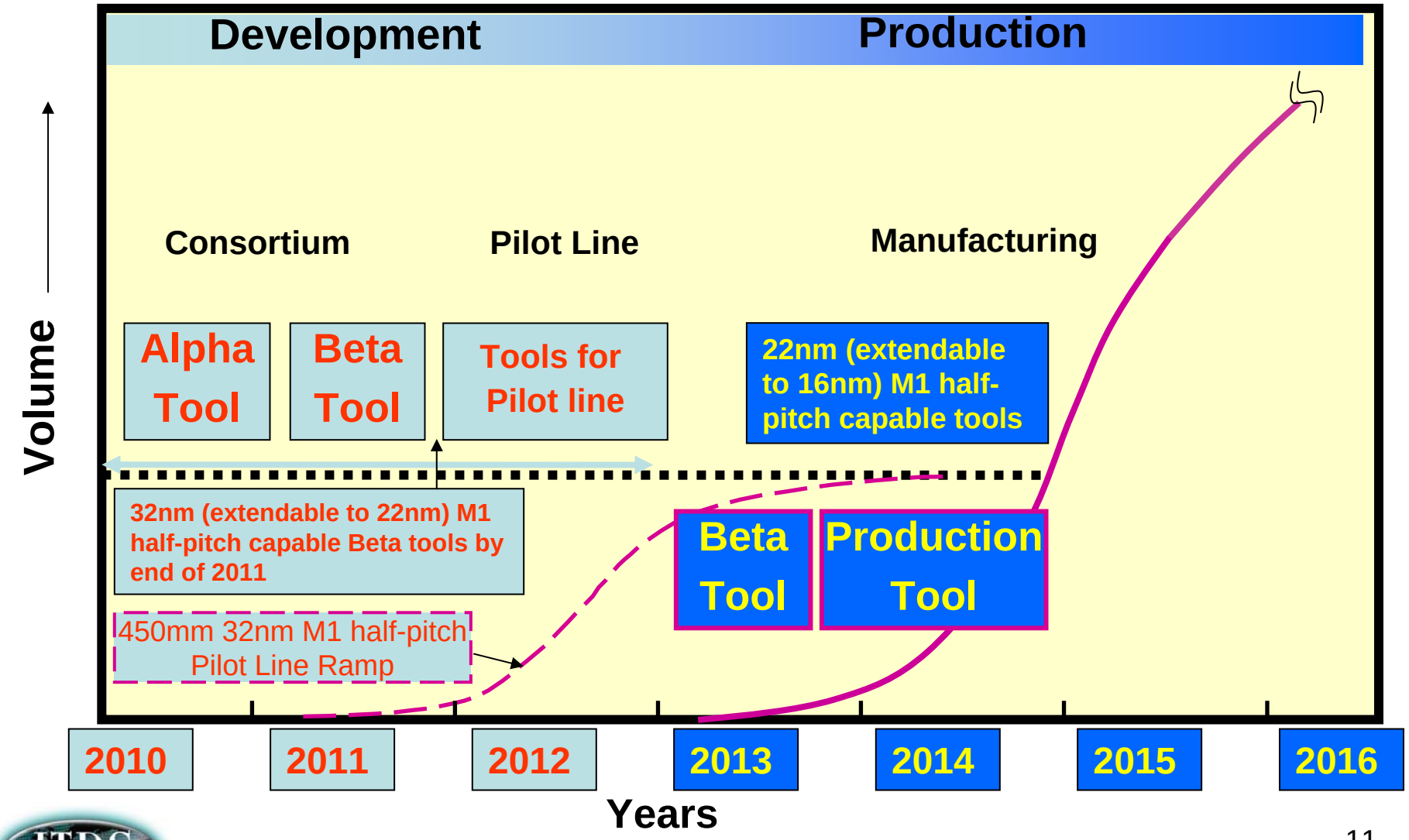


Source: 2009 ITRS - Executive Summary Fig 2b

2009
Unchanged

450mm Production Ramp-up Model

[2009 Figure 2c A Typical Wafer Generation Pilot Line and Production "Ramp" Curve]



Source: 2009 ITRS - Executive Summary Fig 2c

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IRC Graphic update Proposal Considerations

Also 450mm “Dual S-Curve” and possible alignment with “Node vs. Technology Trends”

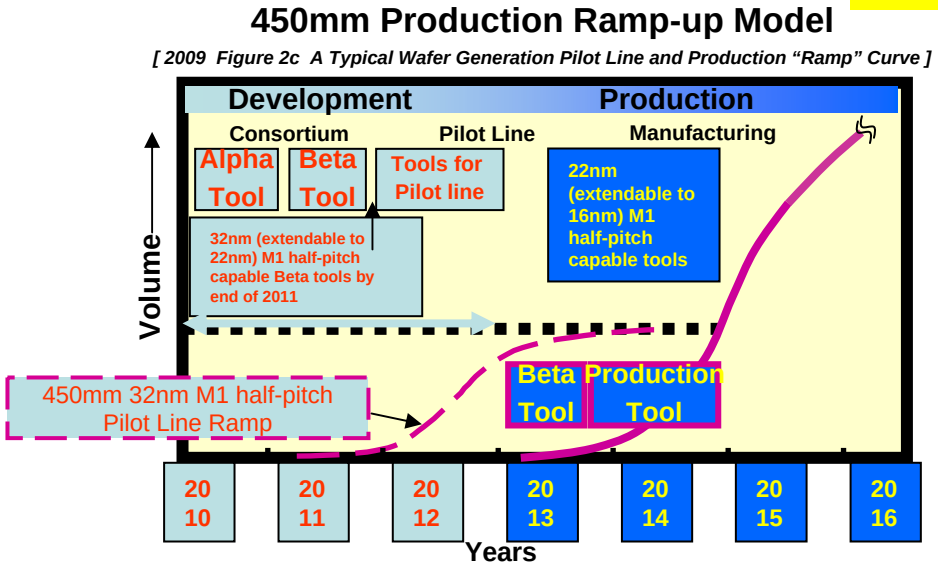
450mm Production Ramp-up Model

2009 WAS

[2009 ITRS Figure 2c A Typical Wafer Generation Pilot Line and Production "Ramp" Curve]

Versus "Node"/actual contacted M1 and un-contacted Poly Half-Pitch alignment

New for 2009



Source: 2009 ITRS - Executive Summary Fig 2c

2009 ITWG Table Timing:	2007		2010		2013		2016	2019
2009 IS ITRS Flash Poly :	54nm	45nm	32nm		22nm		16nm	11nm
2009 IS ITRS DRAM M1 :	68nm		45nm		32nm		22nm	16nm
MPU/hpASIC "Node":	"45nm"		"32nm"		"22nm"		"16nm"	"11nm"	"8nm"
2009 ITRS MPU/hpASIC M1 :	76nm	65nm	54nm	45nm	38nm	32nm	27nm	19nm	13nm
2009 ITRS hi-perf GLpr :	54nm	47nm	47nm	41nm	35nm	31nm	28nm	20nm	14nm
2009 ITRS hi-perf GLph :	32nm	29nm	29nm	27nm	24nm	22nm	20nm	15nm	12nm

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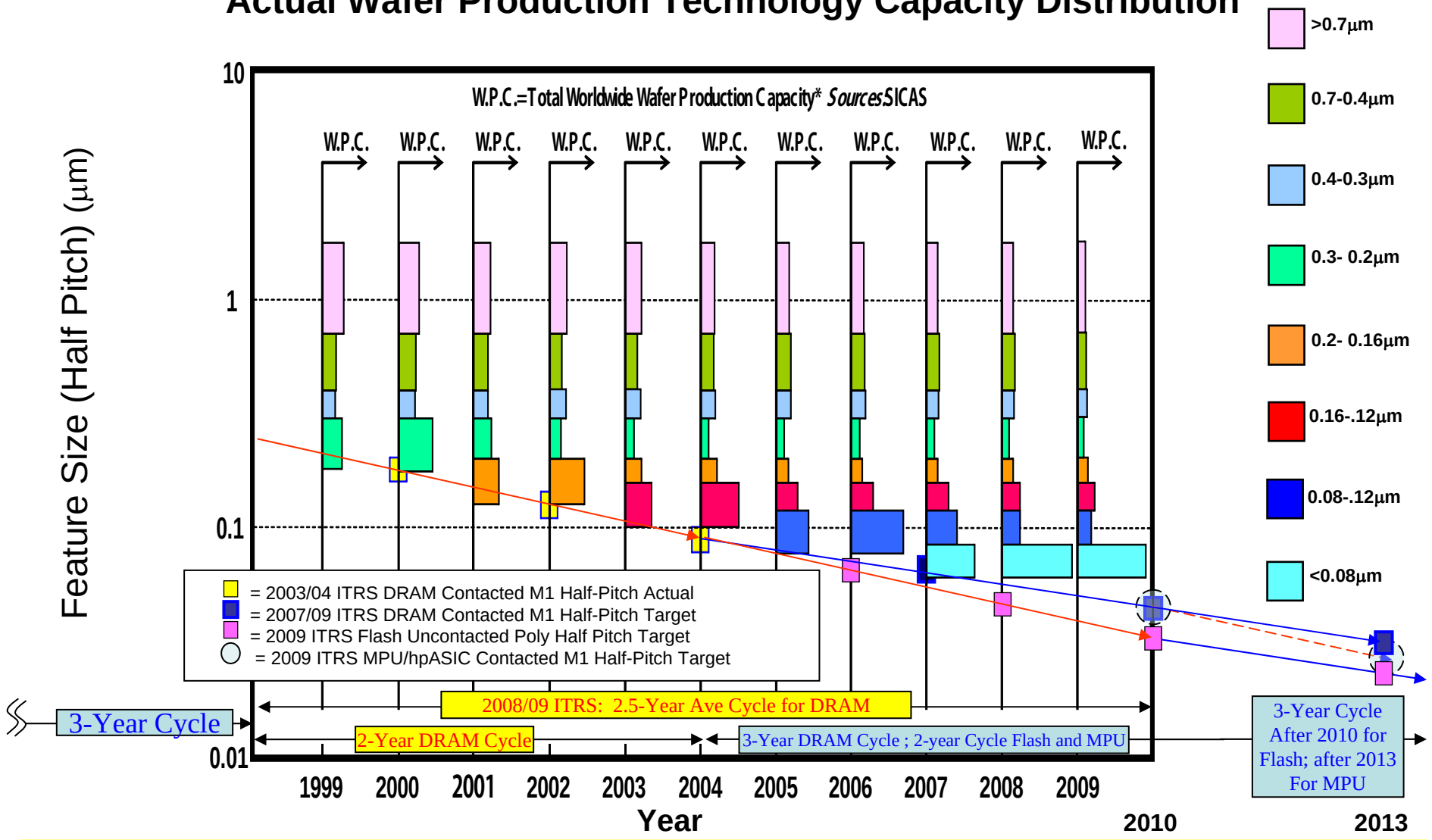
Technology Cycle Timing Compared to Actual Wafer Production Technology Capacity Distribution

2009 WAS

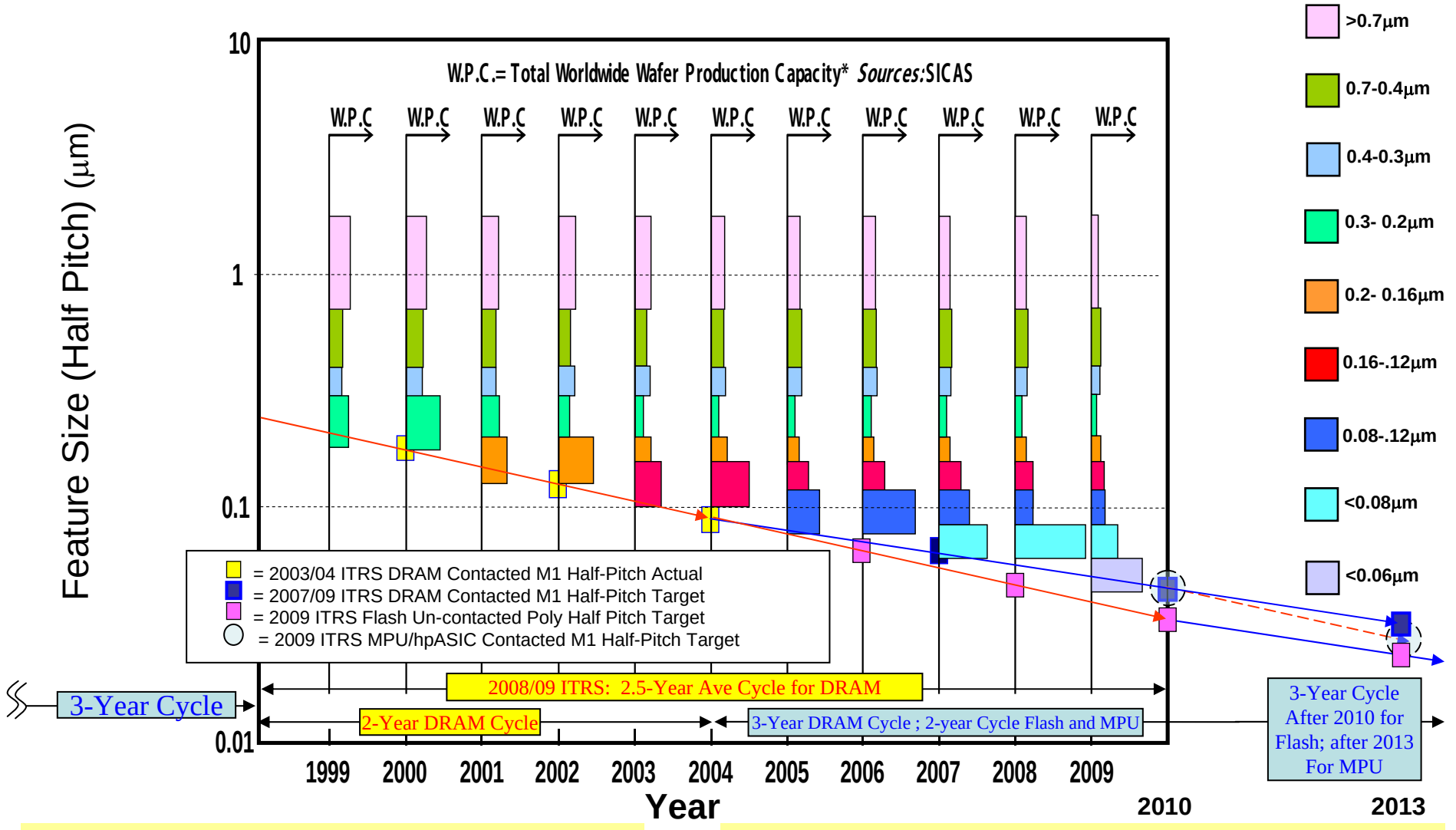


** Note: The wafer production capacity data are plotted from the SICAS* 4Q data for each year, except 2Q data for 2009. The width of each of the production capacity bars corresponds to the MOS IC production start silicon area for that range of the feature size (y-axis). Data are based upon capacity if fully utilized.*

Source: 2009 ITRS - Executive Summary Fig 3

Technology Cycle Timing Compared to Actual Wafer Production Technology Capacity Distribution

4Q09 SICAS Update Proposal
From Furukawa-san/Japan
To IRC 3/28/10 (modified by AA)



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Source: 2009 ITRS - Executive Summary Fig 3

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