Intel's Breakthrough in High-K Gate Dielectric Drives Moore's Law Well into the Future

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Overview

In a groundbreaking article written in 1965, Gordon Moore described exponential growth in the number of transistors per integrated circuit and predicted this trend would continue. "Moore's Law," states that the number of transistors on integrated circuits doubles approximately every 24 months, resulting in higher performance at lower cost.

This simple but profound statement is the foundation of semiconductor and computing industries. It is the basis for the exponential growth of computing power, component integration that has stimulated the emergence of generation after generation of PCs and intelligent devices.

Perhaps the most vital question for the industry is: how much longer can Moore's Law continue?

As transistor geometries scale to the point where the traditional silicon dioxide (SiO_2) gate dielectric becomes just a few atomic layers thick, tunneling current leakage and the resulting increase in power dissipation and heat become critical issues. The mission of Intel's technology development team in Components Research is to break down the barriers and keep Moore's Law rolling forward. Solving the gate dielectric problem is a critical issue for the industry.

After several years of intensive effort the Intel research team has identified a new material known as "high-K" to replace SiO_2 as the gate dielectric. To resolve compatibility issues with this new high-K dielectric, Intel also needed to discover new metals to replace the traditional polysilicon gate electrode used in NMOS (negative polarity metal oxide semiconductor) and PMOS (positive polarity metal oxide semiconductors) transistors.

Intel has successfully demonstrated that these new materials can reduce gate leakage by over 100-fold, while delivering record transistor performance. This breakthrough is expected to drive Moore's Law well into the future.

Running Out of Atoms

For three decades, SiO_2 formed the perfect gate dielectric material, successfully scaling from a thickness of 1,000 Å (100 nm) 30 years ago to a mere 12 Å (1.2 nm) at today's 90 nm process node. This represents a layer only four atoms thick (**Figure 1**).

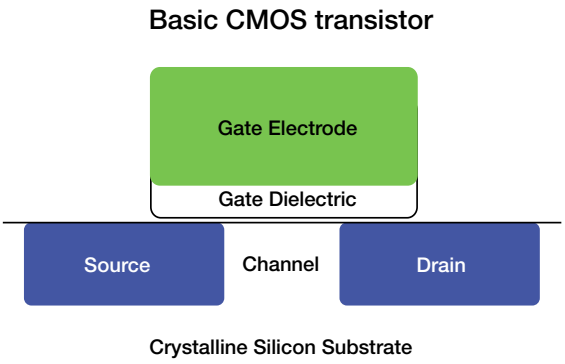

Figure 1. Basic CMOS transistor. At the 90 nm process node, the thickness of the SiO_2 gate dielectric is 1.2 nm, or only about four atomic layers. Current leakage due to tunneling imposes significant power dissipation, which motivated the search for a suitable alternative dielectric material. The incompatibility of high-K dielectric materials with the polysilicon traditionally used for the gate electrode also required alternative metal materials in both NMOS and PMOS transistors.

The problem is that as the oxide layer gets thinner, the rate of gate leakage tunneling goes up. Current leakage contributes to power dissipation and heat.

In addition to implementing 1.2 nm physical SiO_2 in our 90 nm logic technology node and products, Intel has demonstrated 0.8 nm physical SiO_2 in its research laboratory. Although transistors with the 0.8 nm gate oxide still show the expected device characteristics, at this point the dielectric has become so thin, we are literally running out of atoms for further scaling. Without a new dielectric material with increased thickness and a higher K value, Moore's Law would inevitably hit a wall.

Search for New Materials

In addition to its dielectric properties, SiO_2 has an almost defect-free dielectric interface, which ensures good compatibility with the silicon substrate and also the polysilicon gate electrode. The task of finding a replacement for SiO_2 is a challenge I would compare to performing a heart transplant for the semiconductor industry.

The effort to find a replacement material in both industry and academia has gone on for more than 10 years. While hafnium and zirconium oxides have good dielectric properties, these compounds are not compatible with the polysilicon material used for gate electrodes.

There are two fundamental side-effects:

- *Threshold voltage pinning*, also known as "Fermi-level pinning," results when a high-K gate dielectric, including oxides of hafnium and zirconium, are combined with a polysilicon gate electrode. Defects at the gate dielectric/gate electrode interface cause relatively high threshold voltages, which causes reduced drive current and impaired performance. To solve this problem we need to replace the polysilicon gate electrode material with new metal materials—one new metal for NMOS transistors and another new metal for PMOS transistors.
- *Phonon scattering* results from the inherent polarization characteristic of metallic oxides. The higher the dielectric constant, or "K" value, the higher the polarization, which creates surface optical (SO) phonon vibration. Phonon vibration interferes with electron mobility in the transistor channel, thereby reducing performance. Metal gate electrodes can reduce the mobility degradation problem by screening the high-K SO phonons from coupling to the inversion channel charge carriers. For high performance, the high-K/metal-gate solution requires metal gate electrodes with the correct work functions, (measured by the transistor flatband or threshold voltage) on high-K for both PMOS and NMOS transistors (**Figure 2**).

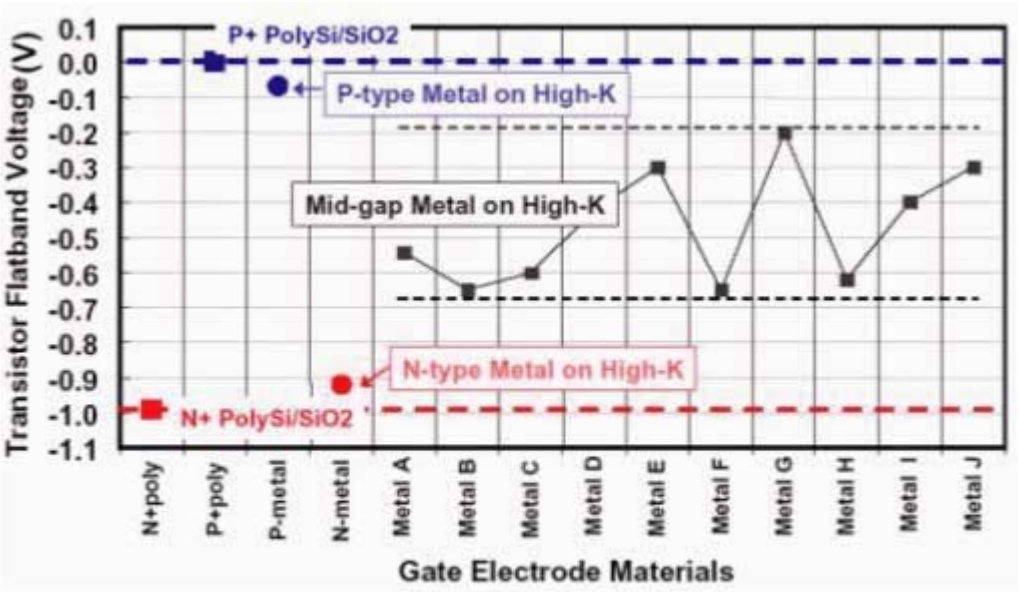

Figure 2. Intel has engineered N-type and P-type metal electrodes on high-K with the correct work functions (measured by flatband or threshold voltage) for NMOS and PMOS devices on bulk silicon.

Record Performance

Many months of persistent effort by the Intel Components Research (CR) team achieved a breakthrough in 2003. The Intel CR team has engineered and demonstrated NMOS and PMOS high-K/metal-gate stacks on bulk silicon with the correct work functions that exhibit channel mobility close to that of SiO_2 with significantly lower gate leakage. The transistors have a physical gate length (Lg) of 80 nm and electrical oxide thickness at inversion (Toxe) of 1.45 nm (**Figure 3**). These transistors exhibit record-setting drive current (Idsat) performance:

- The NMOS devices have a drive current of 1.66 mA/µm, with off-state leakage current of 37 nA/µm at 1.3V.
- The PMOS devices have a drive current of 0.69 mA/µm, with off-state leakage current of 25 nA/µm at 1.3V.

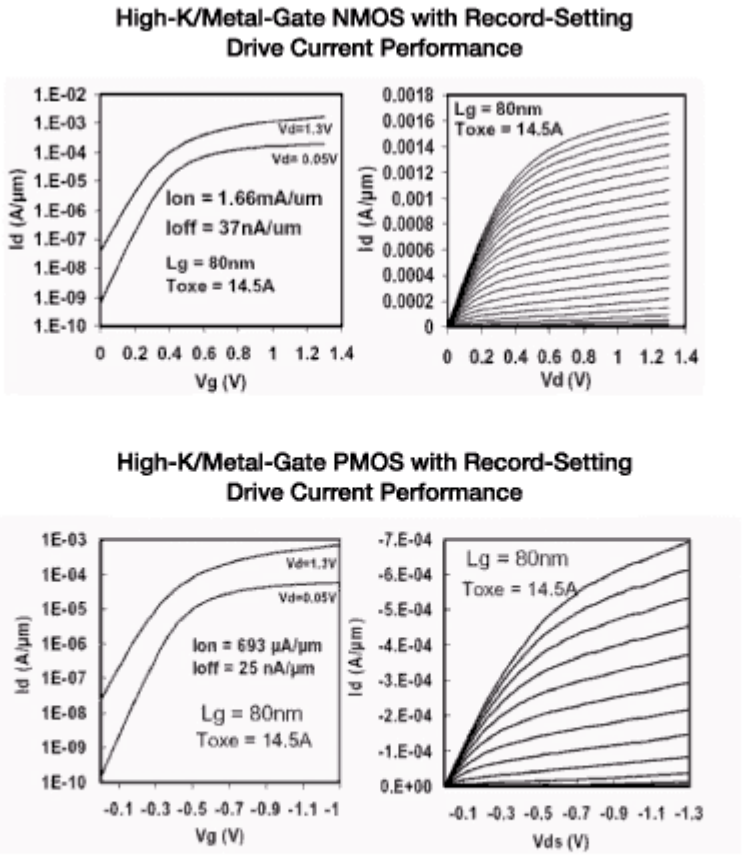

Figure 3. The Intel team fabricated high-K/metal-gate NMOS and PMOS transistors on bulk Si, with a physical gate length (Lg) of 80 nm and electrical oxide thickness at inversion (Toxe) of 1.45 nm. These transistors exhibit record-setting drive current (Idsat) performance and significantly lower gate leakage than SiO_2.

We believe high-K/metal-gate is one of the options for the 45 nm logic technology node, scheduled to be in production in 2007. Another option is the tri-gate transistor, which was described in the July 2003 issue of Technology@Intel Magazine.

Can-Do Spirit

The quest for alternative transistor gate materials was a mandatory effort for the semiconductor industry to drive Moore's Law into the future. Intel's program involved several years of intensive effort and good science, including both theoretical and laboratory work.

There is no way to adequately describe the "can-do" spirit and persistence of the research team, who were not afraid to fail. This effort and sense of teamwork ultimately paid off with breakthrough results.

This technology is now evolving from pure research to development work with Intel manufacturing engineers.

Summary

Moore's Law, which states that the number of transistors on integrated circuits doubles every processor generation (approximately every 24 months) is the foundation for the exponential growth of computing power and component integration at reduced cost. Current leakage and power dissipation issues associated with the traditional SiO_2 CMOS transistor gate dielectric impose practical limits on the extensibility of Moore's Law.

After several years of effort, the Intel technology team has made a major breakthrough that solves the chip power problem. Intel has identified a new material known as "high-K" to replace SiO_2 as the gate dielectric, in addition to new metals to replace the polysilicon gate electrode of NMOS and PMOS transistors.

These new materials, when implemented with the correct process recipe, reduce gate leakage by over 100-fold, while delivering record transistor performance. Intel is on track to implement this new technology in the 45 nm node in 2007. The breakthrough will drive Moore's Law into the next decade.

Feedback
Tell us what you think about this article.

More Info

Visit the Intel Web site for more information on Intel's High-K/Metal Gate breakthrough.

Gordon Moore's 1965 article, entitled *Cramming More Components Into Integrated Circuits*, is available on the Intel Web site.

Author Bio

Intel Fellow Robert S. Chau is responsible for directing research and development in advanced transistors and gate dielectrics for microprocessor applications. He is also responsible for leading research efforts in advanced nanotechnology for future device and process applications.

Chau joined Intel in 1989 and developed seven generations of Intel® gate oxides along with many transistor innovations used in various Intel® logic processes. He also introduced many new process modules and electrical test capabilities for Intel's future logic processes. He is a co-inventor and patent holder of the Intel's SiGe S/D, strained-Si PMOS transistor used in the 90 nm technology node. Chau was promoted in 2000 to the rank of Intel Fellow, the company's highest and most prestigious technical position.

He received his bachelor's, master's, and Ph.D. degrees in electrical engineering from Ohio State University. He holds 40 United States patents in device and process technologies. Chau received the 2003 Alumni Professional Achievement Award from The Ohio State University Alumni Association. He was recently selected in December 2003 by *Industry Week* magazine as one of the "top 16 R&D stars in U.S. who continue to push the boundaries of technical and scientific achievement."

—End of Technology@Intel Magazine Article—