

**PROCESS INTEGRATION ISSUES
OF LOW-PERMITTIVITY DIELECTRICS
WITH COPPER FOR HIGH-PERFORMANCE
INTERCONNECTS**

A DISSERTATION

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING

AND THE COMMITTEE ON GRADUATE STUDIES

OF STANFORD UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF Ph.D.

CHAPTER 2

Alvin Leng Sun Loke

March 1999

Chapter 2 Review of Interconnect Integration

The investigations to be presented in subsequent chapters assume a basic command of interconnect process technologies. This chapter provides an overview of interconnect integration, emphasizing key features in both conventional Al and Damascene Cu technologies. It is hoped that with this review, the less familiar reader will have acquired some relevant background information for comprehending the context of the work to follow.

In conventional silicon IC technologies, the interconnects are incorporated after front-end processing. Frontend processing refers to the sequence of fabrication steps, typically at very high temperatures (700–1100°C), that form the MOS transistors in the active regions, the pockets of thick isolation in the field regions that separate adjacent transistors, and the silicidation of the transistor terminals for low-resistance contacts. The reader is directed to [38]–[40] for a representative flavor of manufacturable advanced frontend technologies.

The backend, referring to the interconnection of transistors, is subsequently formed by contacting the transistor terminals and then vertically stacking alternating layers of metal wires and vias encased in dielectric. Backend process temperatures typically do not exceed 450°C to avoid melting of the metals and to control stress.

2.1 Conventional Technology

The state-of-the-art 0.25- μm backend, shown in Figure 2-1, is revisited to illustrate the integration of conventional Al metallization. The example consists of five levels of aluminum (Al) alloy wires and tungsten (W) vias (also called plugs or studs) embedded in oxide (SiO_2). Integration success is largely attributed to the processes that maintain excellent planarity after fabricating each and every via and wire level. The absence of topography helps to mitigate the fundamental depth-of-focus limitation of high-resolution lithography and avoid reliability problems such as metal line breaks over dielectric steps.

2.1.1 Fabrication of Tungsten Vias

The process sequence for forming tungsten vias is summarized in Figure 2-2 [40]. First, a thick blanket oxide film is deposited on a planar surface, typically by PECVD

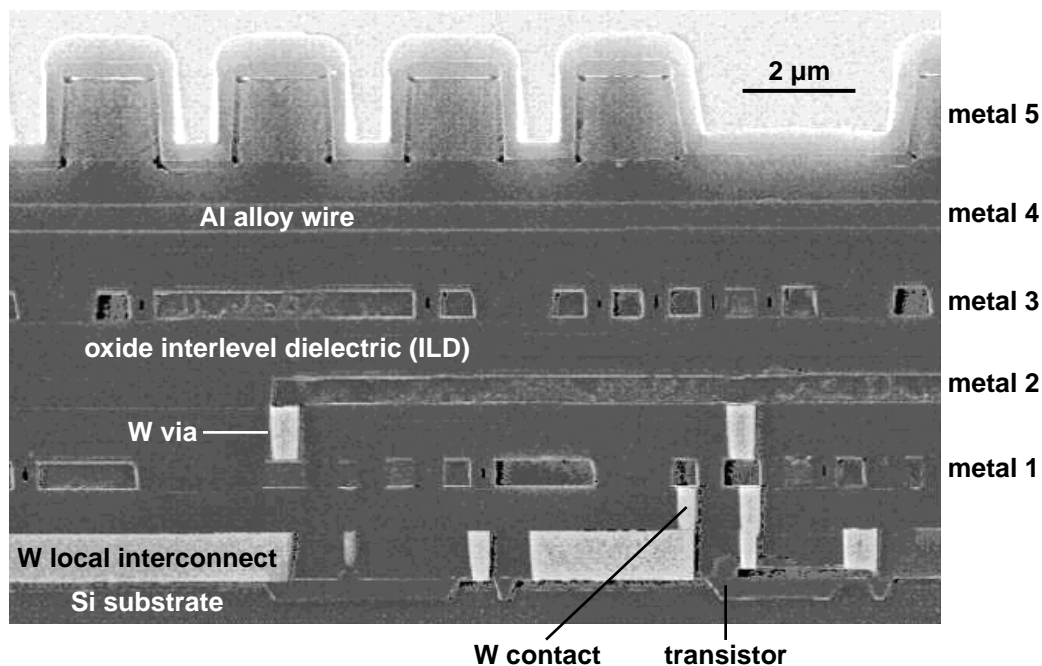


Figure 2-1 Cross-sectional scanning electron micrograph of state-of-the-art 0.25- μm CMOS multilevel interconnect technology for high-performance logic. Courtesy of Motorola.

(plasma-enhanced chemical vapor deposition) with a TEOS (tetraethyl orthosilicate) precursor at 350–400°C. The oxide ILD is patterned by photoresist and then etched to expose the underlying metal layer or contact level silicide. After the resist is stripped, the via opening is cleaned and then lined with a thin PVD titanium (Ti) layer. In modern CMOS technologies, PVD (physical vapor deposition) exclusively refers to sputtering. The Ti film serves as an adhesion layer and also decreases contact resistance to underlying conductors by reducing interfacial oxides. Titanium nitride (TiN) is subsequently deposited *in situ* either by sputtering or by CVD. Following that, the remaining part of the hole is conformally filled void-free with CVD tungsten at 425–450°C by SiH_4 reduction of WF_6 . Here, the TiN barrier layer protects the CVD by-products from attacking the underlying Ti adhesion layer and oxide. The excess W, TiN, and Ti in the field regions are finally removed by chemical-mechanical polishing (CMP), making the top of the W via thus formed coplanar with the flat oxide surface. This method of embedding metal structures in dielectrics is known as the *Damascene* process, paying tribute to an ancient art that originated in Damascus. Jewellers then would inlay soft metals, such as gold, in precious stones by boring into the gem, filling the opening with metal, and polishing away the excess metal.

Tungsten via technology has matured to the point where void-free and untapered vias with aggressive aspect ratios exceeding 3:1 are routinely formed, thus enabling increases in wiring density and reduction of capacitive parasitics to under- and overlying wires. Advances in lithography alignment have also enabled borderless vias to be formed, thereby permitting even further improvements in wiring density. In addition, Damascene tungsten has been adapted as planar local interconnects for strapping source/drain and gate contacts [41]. Although this process is more difficult to control, successful implementation of tungsten local interconnects can reduce the cell size of SRAM's used as microprocessor cache memories by 20–30%.

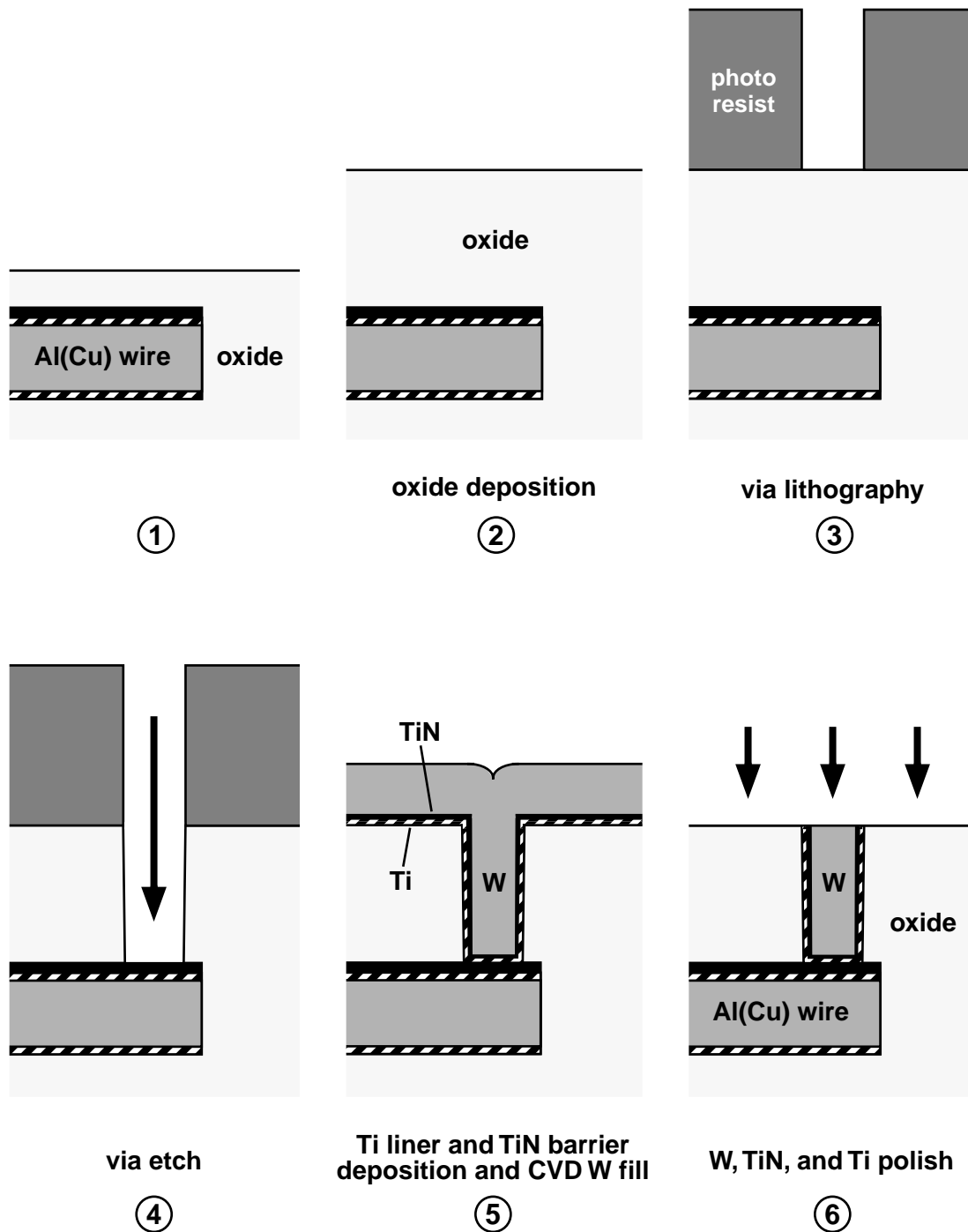


Figure 2-2 Process flow for fabrication of tungsten vias.

The chief drawback of tungsten via technology is cost. Furthermore, processing of tungsten, a brittle refractory metal, is notorious for introducing particles and defects on the wafer and compromising yield. Before CMP was employed, these problems were even more severe when the excess W was removed by etching. Cost alone continues to motivate the development of cheaper via technologies.

2.1.2 Fabrication of Aluminum Alloy Wires

The conventional process for forming Al alloy wires, also known as the *cloisonné* process, is summarized in Figure 2-3 [40]. After via or contact CMP, metal is sputtered over a planarized surface. The metal deposition typically consists of a sequence of Ti, Al(Cu), Ti, and TiN depositions without breaking vacuum. The Al layer is alloyed with 0.5% Cu which segregates to the Al grain boundaries for improved electromigration resistance [42]. This “Ti-over-and-under” wiring uses Ti as a base layer for good adhesion, low contact resistance to underlying vias, and a seed for (111)-textured Al(Cu) grains which have better electromigration resistance. The Al(Cu) layer is sandwiched by thin Ti layers because subsequent thermal treatment forms TiAl_3 , a hard refractory intermetallic that further improves electromigration reliability as well as mechanical stability against stress-induced void and hillock formation. Finally, the reactively sputtered TiN film caps the metal stack to minimize the reflectivity of the stack and thus facilitate photolithographic control of fine features. The process flow continues with the metal lithography and etch. The vertical reactive ion etch (RIE) of the metal stack is becoming increasingly difficult for very aggressive line geometries. After the metal is patterned, the photoresist is removed and the metal spaces are subsequently filled by a conformal oxide deposition. Void-free dielectric gapfill remains an integration challenge, but can be achieved with high-density plasma (HDP) CVD oxide processes for 0.18- μm technologies. The residual oxide topography is removed with oxide CMP, leaving a planar oxide surface as the starting point for fabricating the next level of vias.

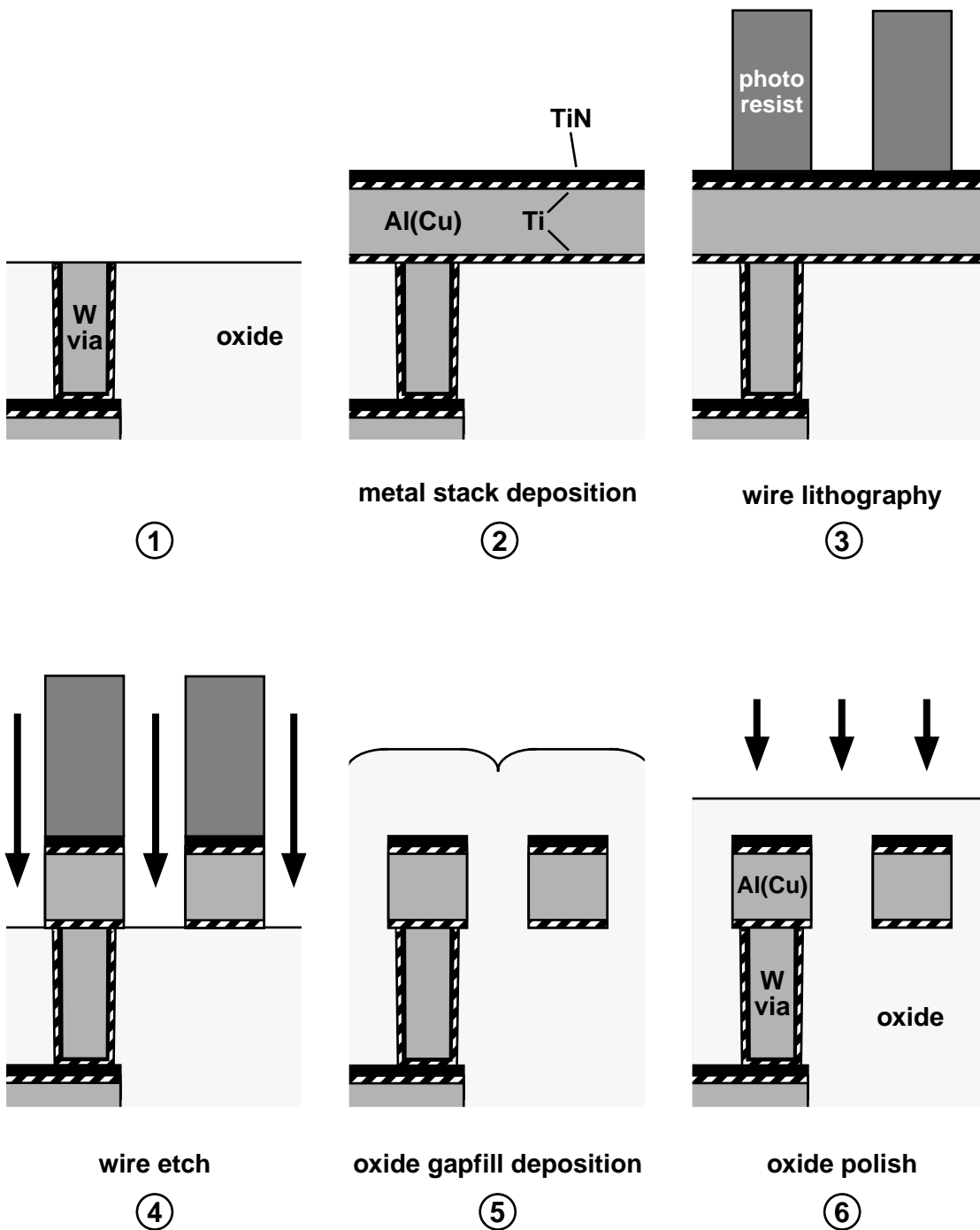


Figure 2-3 Process flow for fabrication of aluminum alloy wires.

2.2 Dual-Damascene Copper Technology

The interconnects in high-performance logic IC's typically obey a hierarchical wiring scheme. As seen in Table 2-1, the metal pitch (sum of line width and spacing) and thickness become progressively larger for interconnects further away from the transistors. The lower layers of interconnection close to the transistors are designed for maximum wiring density. On the other hand, the uppermost layer(s) of thick interconnects (also called *fat wires*) are generally reserved for long connections as well as power and ground distribution.

Table 2-1: Interconnect Design Rules for 0.25- μm Technology [18]

Layer	Minimum Pitch	Thickness	Wire Aspect Ratio
metal 1	0.48 μm	0.48 μm	1.5 : 1
metal 2	0.93 μm	0.90 μm	1.9 : 1
metal 3	0.93 μm	0.90 μm	1.9 : 1
metal 4	1.60 μm	1.33 μm	1.7 : 1
metal 5	2.56 μm	1.90 μm	1.5 : 1

2.2 Dual-Damascene Copper Technology

The cross-section of a manufacturable copper interconnect technology is shown in Figure 2-4. In this example, W local interconnects and contacts are fabricated first using the Damascene process described in Section 2.1.1. Then, six levels of Cu wiring are integrated with Cu vias between successive metal layers. Oxide is both the via- and wire-level dielectric. As mentioned in Chapter 1, the main technical issues with Cu integration are Cu line patterning and potential device contamination.

Deep submicron copper interconnects cannot be formed using the conventional cloisonné approach that is ubiquitous in Al metallization. Cu halide compounds, e.g., chlorides and fluorides, that form during plasma etching are hardly volatile at low temperatures [43], rendering the etch prohibitively slow. Unfortunately, photoresist can-

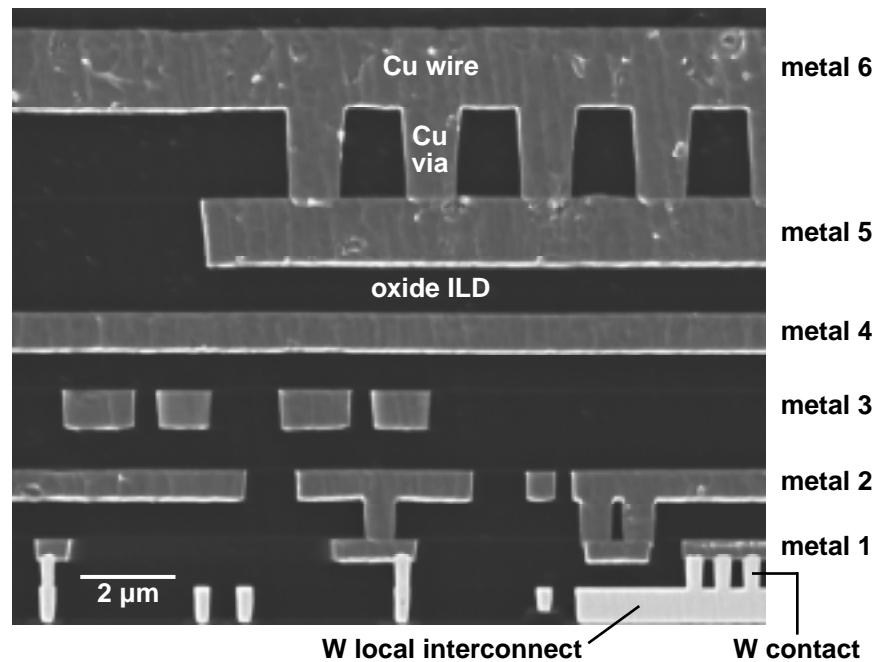


Figure 2-4 Scanning electron micrograph of manufacturable copper interconnect architecture demonstrated by IBM [27].

not withstand the temperatures required for practical Cu etch rates ($> 200^{\circ}\text{C}$). Dielectrics such as polyimide, oxide, and nitride have been explored as alternative masking materials but they complicate the lithography process. Wet etching and lift-off approaches have also been attempted [44]. However, line width control of deep submicron features is essentially impossible with these techniques.

Cu is known to be a fast diffuser in silicon where it can act as a deep level acceptor in the silicon bandgap [45]. Deep level states degrade minority carrier lifetimes, causing high junction leakage in transistors and short retention times in DRAM's. Cu also diffuses through silicon dioxide, especially under electrical bias [46]. These facts have raised serious concerns about device contamination should Cu be introduced into the backend. Successful implementation of Cu interconnects must consequently prevent any trace amounts of Cu from migrating to the Si substrate. This will not only involve added process complexity but also influence wafer handling and tool designs.

The preceding obstacles are overcome by the dual-Damascene process with diffusion barriers surrounding the Cu interconnects [47]. Illustrated in Figure 2-5, dual-Damascene is a modified single-Damascene process where incorporating a second lithography step defines both wire trenches and via holes before they are backfilled with Cu. Hence, Cu wires and vias are formed with only one metal fill and one CMP step. Otherwise, two complete single-Damascene flows will be required: one for the vias and the second for the overlying wires. This process simplification results in reduced cost and improved manufacturability. The Cu interconnects are isolated from the surrounding oxide by metal barrier materials on the interconnect side and bottom interfaces, and by a dielectric barrier

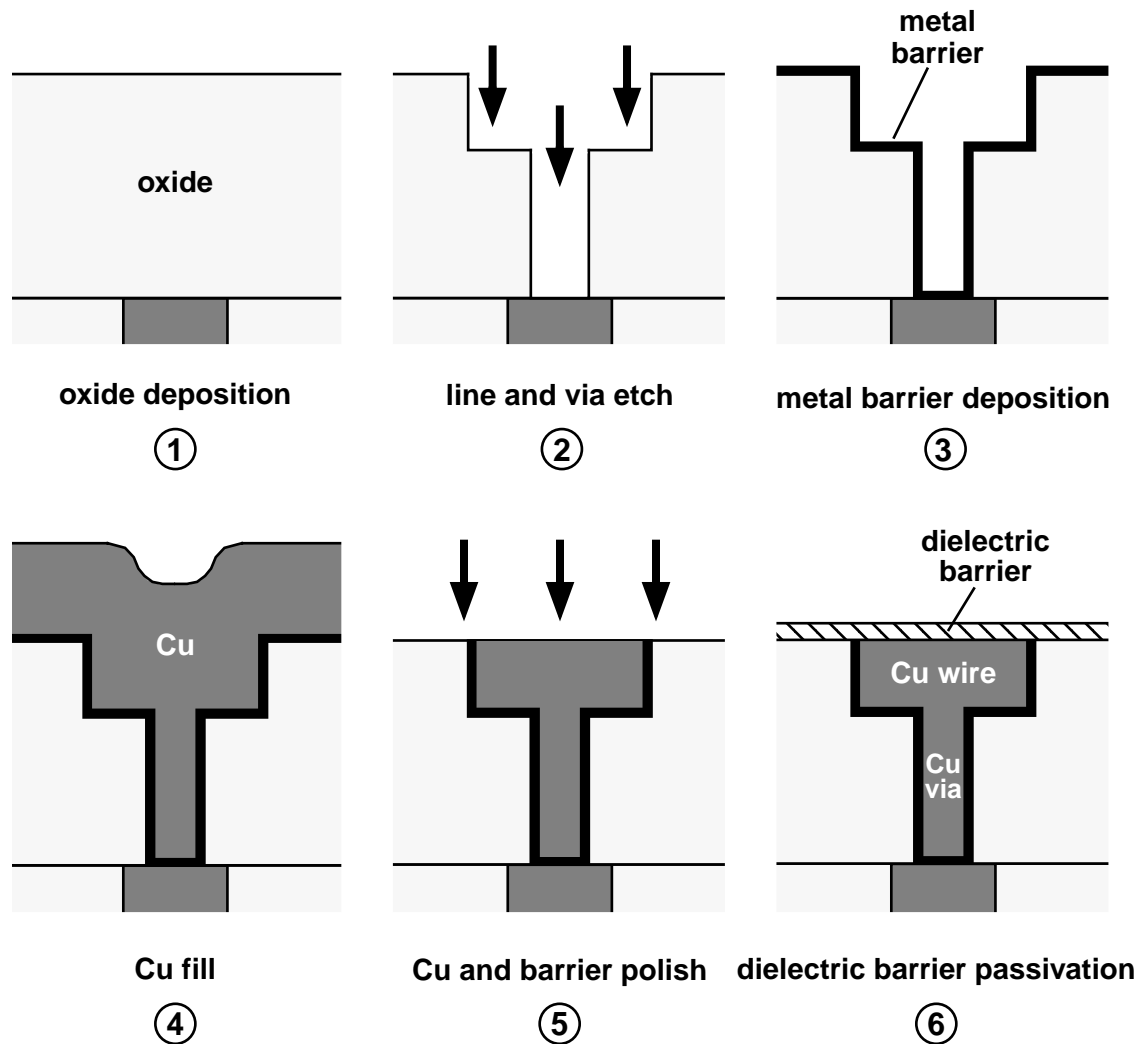


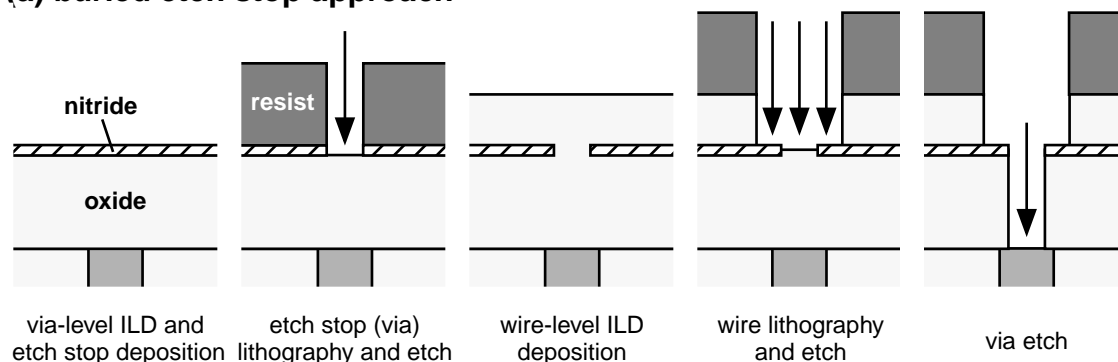
Figure 2-5 Simplified dual-Damascene process flow for fabricating Cu interconnects.

above the interconnect. The individual steps in the dual-Damascene flow and the complex considerations in choosing barrier materials are elaborated in the subsections to follow.

2.2.1 Dielectric Etch

In a dual-Damascene flow, there are various methods of forming wire trenches and via holes to the underlying conductor [48]. Five approaches are summarized in Figure 2-6 [49]–[53]. Their merits and issues are listed in Table 2-2. The specific flow that is ultimately implemented in manufacturing will vary from company to company and depends on the process strengths in lithography and etch within a corporation.

(a) buried etch stop approach



(b) clustered approach

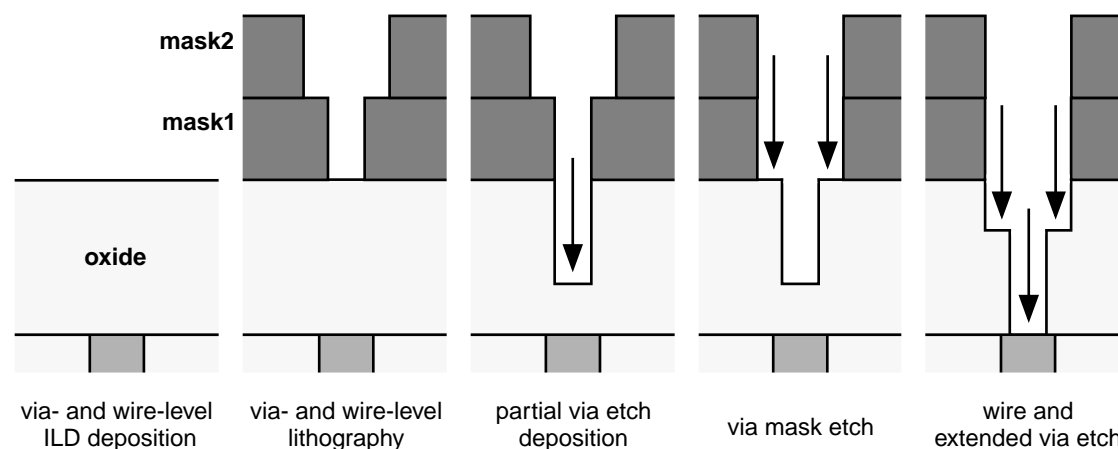
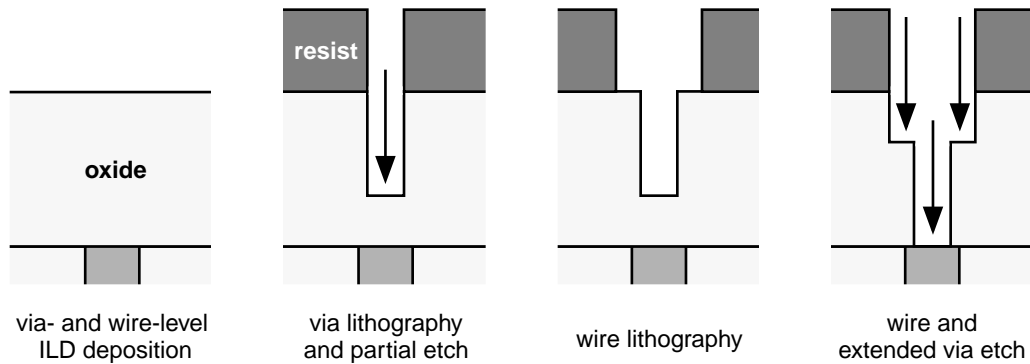
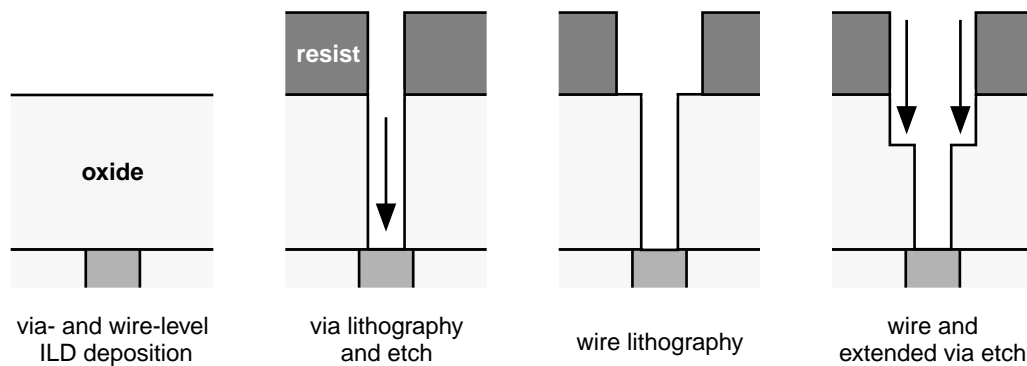


Figure 2-6 Dual-Damascene variations for defining wire trenches and via holes: (a) buried etch stop and (b) clustered approaches.

(c) partial via first approach



(d) full via first approach



(e) line first approach

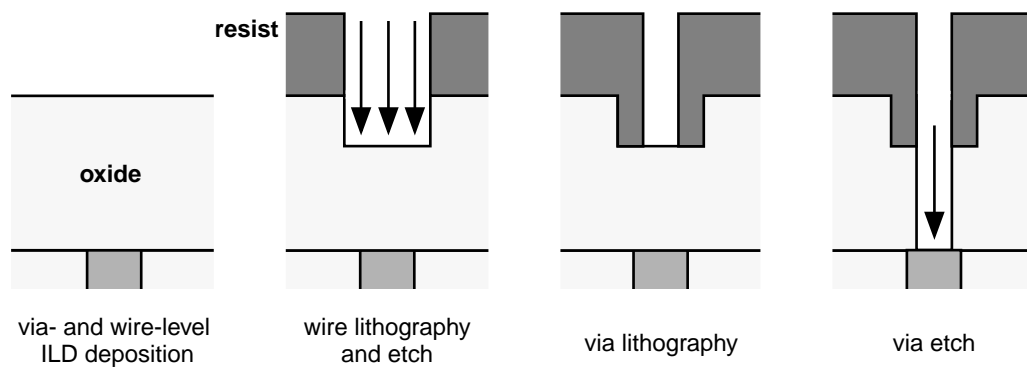


Figure 2-6 Dual-Damascene variations for defining wire trenches and via holes: (c) partial via first, (d) full via first, and (e) line first approaches.

Table 2-2: Comparison of Dual-Damascene Dielectric Etch Approaches [48]

Process Flow	Advantages	Disadvantages
buried etch stop [49]	topography minimized	etch process selectivity and control are critical
clustered [50]	process types grouped	resist adhesion, pattern transfer
partial via first [51]	cleaner structure, less critical etching	lithography process difficulty increased
full via first [52]	lithography and etch processes slightly easier; stacked via trivial	lithography rework and resist cleaning process difficult
line first [53]	easier etch process, less topography for lithography	resist cleaning process critical

2.2.2 Metal Barrier Deposition

Barrier encapsulation of Cu interconnects is required to ensure that even trace levels of Cu do not diffuse through the surrounding dielectrics into the Si substrate. As illustrated in Figure 2-5, both metal and dielectric barriers will be needed for dual-Damascene integration of Cu with oxide.

Following the dielectric etch, the wire trenches and via holes must be lined with a conductive barrier material to clad the side and bottom boundaries of the Cu interconnects. Since barrier materials are generally very resistive compared to Cu, barrier thickness must be kept to a minimum in order to preserve the effective conductivity advantage of Cu over Al alloys. Minimum barrier thicknesses in the 20–30 nm range are expected for 0.18- μm technologies [24]. Besides possessing superior barrier property, metal barriers should additionally exhibit low contact resistance to Cu. This requires an effective clean of the via holes following the dielectric etch. Since the via etch will expose underlying Cu wires, the clean must not redeposit any Cu onto the via hole sidewalls [54]. The barrier layers should also have low stress and good adhesion to oxide. In addition, barriers play an

important role in determining the microstructure of Cu films that are subsequently deposited. Similar to that of Al alloys, the electromigration reliability of Cu interconnects depends on Cu film texture [55]. The texture and roughness of the barrier layer are only two factors affecting the texture that develops in Cu films [56]. Finally, for integration feasibility, it is critical that metal barriers be deposited conformally into high aspect-ratio holes with low particle counts and be easy to planarize [57].

The above requirements have generated much interest to evaluate the barrier properties of refractory metals, primarily Ti, W, tantalum (Ta), and their nitrides [58]. With the wealth of experience gained from W via technology, the industry would ideally like to extend the use of Ti/TiN liners in Damascene Cu integration. However, it appears that TiN may be inadequate as a barrier against Cu diffusion. Ta and TaN have shown great promise. Amorphous materials are also being considered. Ternary films of TaSiN as thin as 5 nm have been shown to exhibit excellent barrier properties, presumably by removing fast Cu diffusion paths along the grain boundaries present in polycrystalline films [57]. These advanced barrier materials will draw more attention as barrier thickness scales with interconnect dimension.

There exists a strong concurrent effort to develop deposition technologies capable of providing conformal coverage of barrier materials in very high aspect-ratio holes. Conformal coverage of the dielectric openings is essential because failure is expected to occur where the barrier is thinnest, usually at the lower corners and sidewalls of a via. Conventional dc magnetron sputtering cannot meet the stringent conformality requirements because the large angular distribution of sputtered atomic flux will result in more deposition along the top corners of the trenches before there is adequate barrier coverage along the via bottom and sidewalls. This cusping will also increase the difficulty of the subsequent Cu fill. See Figure 2-7. Sputtering technology has thus been modified to improve vertical flux directionality. Long-throw, collimated, and ionized metal plasma (IMP) sputtering technologies provide better but not completely conformal step coverage. Inherently a conformal process, CVD also has been actively investigated but is an expensive technol-

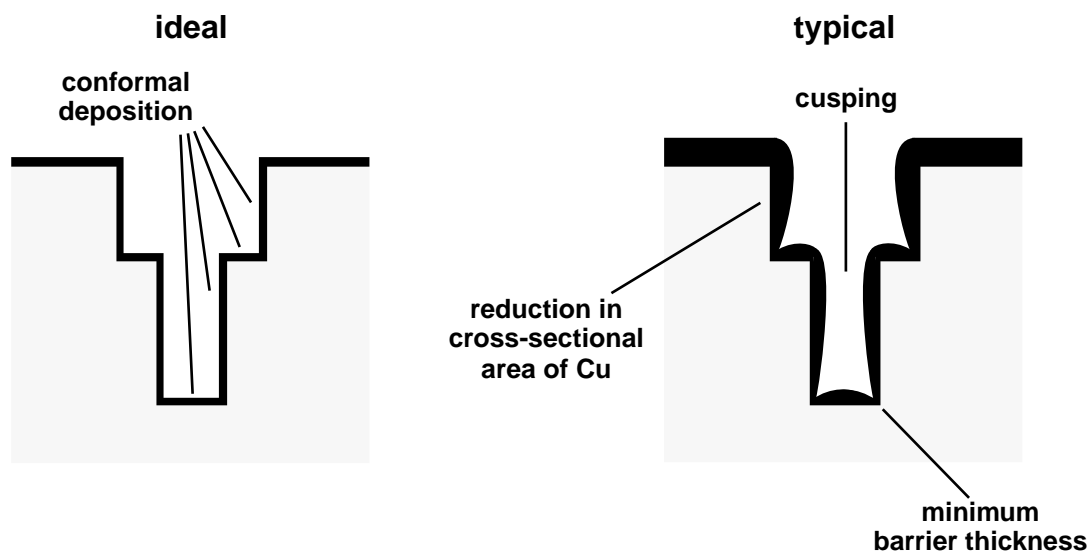


Figure 2-7 Comparison of ideal and typical step coverages of a metal barrier deposited by PVD [57].

ogy. The potential of CVD will depend on the extendability of cheaper sputtering technologies for more aggressive geometries [54].

The development of a metal barrier technology is key to successful integration of Cu with oxide. Although many implementation details remain undisclosed by companies involved, there is growing consensus in the industry to employ Ta liners and TaN barriers deposited by IMP sputtering.

2.2.3 Copper Deposition

After metal barrier deposition, the trenches and vias are filled with Cu. Many technologies have been explored to identify a cost-effective solution capable of high aspect-ratio and void-free Cu fill. Four are described in this discussion: PVD, CVD, electroless plating, and electroplating.

PVD techniques, even with improved flux directionality, are incapable of achieving void-free Cu fill. Revisiting Figure 2-7, the cusping that develops during sputtering will eventually pinch off the Cu film near the top of the trench and form a keyhole. However,

good trench filling has been demonstrated through reflow after sputtering [59]–[60]. First, the trench is partially filled by sputtering. In a subsequent *in situ* heat treatment, typically at 450°C for 30 minutes, the metal atoms redistribute from the field region into the trench, thereby completing the fill. The reflow process is thermodynamically driven by surface diffusion which minimizes the surface energy of the Cu film. It is very sensitive to the purity of the ambient gas during anneal, microstructural inhomogeneities in the Cu film, the wettability of the barrier underlayers, and the density of trench features. Moreover, the relatively high thermal budget incurred by the reflow anneal may unnecessarily impose stricter barrier requirements. The limited process latitude renders sputter reflow inadequate for manufacturing.

Due to its superior step coverage over PVD, CVD has naturally received much attention. CVD Cu films are deposited by thermal decomposition of organometallic (OMCVD) precursors at 150 to 200°C [61]. The most extensively investigated precursor is Cu(hfac)(tmvs), abbreviated for copper (I) hexafluoroacetylacetonate trimethylvinylsilane. Although excellent trench fill in aggressive geometries have been demonstrated, the main bottleneck preventing widespread use of CVD Cu is cost. The price of the Cu precursor will remain prohibitively high until cheaper alternative fill technologies can no longer accommodate the fill requirements as interconnects continue to scale.

Electroless plating, a cheap and simple means of selectively depositing thin Cu films, was also considered [62]. Wafers are immersed in a heated bath of aqueous Cu ions. Cu atoms are then supplied to the wafer surface by catalytic reduction of the Cu ions, but only at exposed conductive surfaces of the wafer. Electroless plating was a serious contender during the early stages of Cu process development. Unfortunately, its primary drawback is lack of process control during deposition. Deposition will proceed spontaneously and depend primarily on the plating solution chemistry and the seed layer. Moreover, the microstructure of electroless Cu films generally consists of very fine grains, implying poor electromigration reliability. For these reasons, electroless Cu is not considered feasible for production.

Recently, electroplating has emerged as the most promising and cost-effective Cu deposition technology [63], having already been demonstrated for manufacturability [27]. In electrochemical deposition of copper, the wafer is coated with a thin seed layer of Cu, typically by sputtering, and immersed in a solution containing Cu^{2+} ions. Although the wafer will have already been lined with a conductive barrier and a thin Cu seed layer, the Cu seed layer is needed because electroplating may not occur on some barriers. Electrical contact is made to the seed layer which serves as the cathode. An electrical current is supplied to the cathode to reduce Cu ions at the wafer, thereby depositing atomic Cu on the Cu seed. As Cu ions are plated out of the solution onto the wafer, the Cu anode simultaneously undergoes oxidation to replenish the supply of Cu ions in the solution. See Figure 2-8.

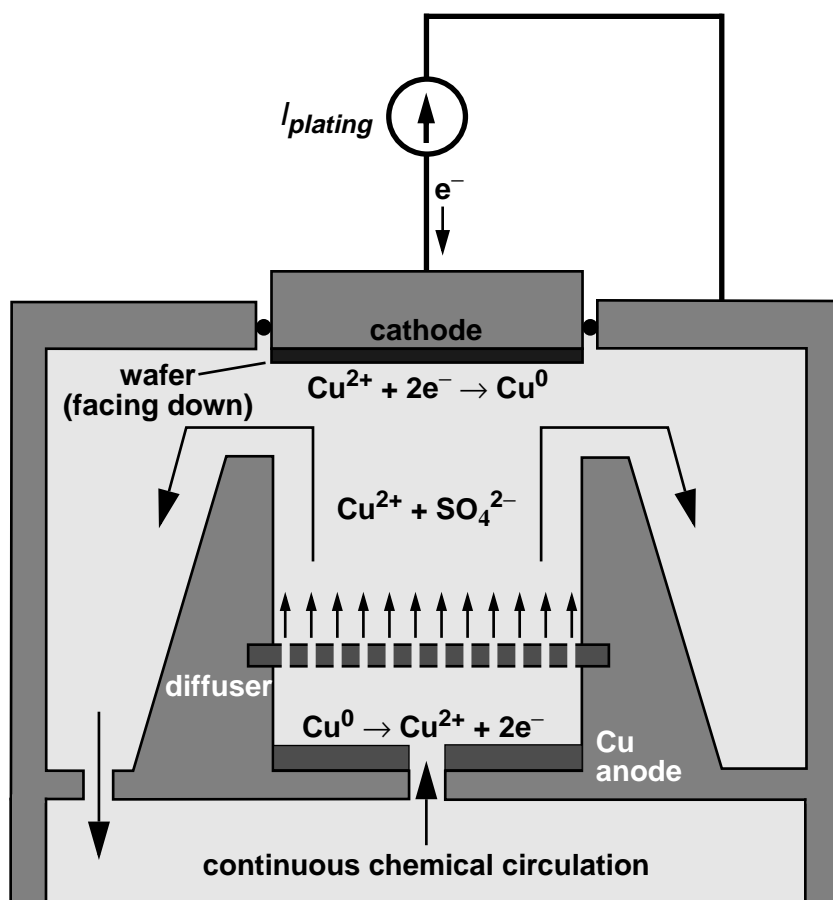


Figure 2-8 Schematic of a Cu electroplating system.

In principle a relatively simple technology, Cu electroplating in practice is fairly complex. A manufacturable process must demonstrate good fill capability, step coverage, film morphology, across-wafer and wafer-to-wafer uniformities, and practical deposition rates. To achieve void-free fill, the contents of the electroplating solution and the way in which the electrical current is applied must be optimized. Otherwise, keyholes may form in the trench since the plating rate is higher at the trench shoulders, where the current density is highest, than at the trench bottom. The plating bath primarily consists of aqueous copper sulfate (CuSO_4) and sulfuric acid (H_2SO_4) but also contains trace quantities of organic additives (e.g., thiourea, disulfides, and polyamines). These additives improve the quality of the deposited Cu film by, for example, enhancing deposition at the bottom of trenches, serving as wetting agents for good film nucleation, and relieving deposited film stress [64]. The trench and via filling capability of electroplating is also improved by modulating the magnitude and direction of the electrical current. Reversing the polarity of the applied current causes oxidation or etching of Cu to occur at the wafer surface. Since the etching rate is also a direct function of current density, a deposition/etch sequence is employed to remove copper from the trench shoulder more quickly than from the trench bottom during the etch cycle, resulting in more conformal coverage.

With both *pulsed* plating waveform and bath chemistry optimized, high aspect-ratio trenches and vias can be successfully filled [65]. Given the appropriate barrier and Cu seed layers and microstructures, plated Cu films with large grain sizes and a near-bamboo microstructure can be obtained. These factors are believed to be responsible for the good electromigration resistance of plated Cu [66].

2.2.4 Chemical-Mechanical Polishing

After the trenches and vias are filled with Cu, the excess Cu in the field region is removed by chemical-mechanical polishing (CMP). Pioneered by IBM, CMP is unquestionably the key enabling technology in Damascene integration [67]. Figure 2-9 illustrates a typical CMP system. Both chemical reactivity and mechanical abrasion play important roles in the selective removal of a film from the wafer surface. Chemicals in the slurry

Chapter 2: Review of Interconnect Integration

react with the film surface, typically forming a thin oxidized layer. This layer is subsequently removed by mechanical abrasion due to fine particles in the slurry under the pressure of the polishing pad. The wafer surface becomes progressively planar with polishing time since the removal or polishing rate increases with local pad pressure.

In metal CMP, a good balance must exist between chemical and mechanical components to achieve optimum planarization. If the mechanical component is too dominant, surface scratches and nonuniform polishing may result. On the other hand, if the chemical component is too dominant, overpolishing can result in severe surface topography due to the selectivity of the slurry chemistry against dielectric removal. Mechanical abrasion depends on the size and concentration of slurry particles, hardness and surface roughness of the pad, pad pressure, and the rotational speeds of the pad and wafer. The chemical component is controlled by the chemistry, concentration, and pH of the slurry. The CMP process must also minimize pattern density and feature size effects in order to avoid dielectric erosion and metal dishing.

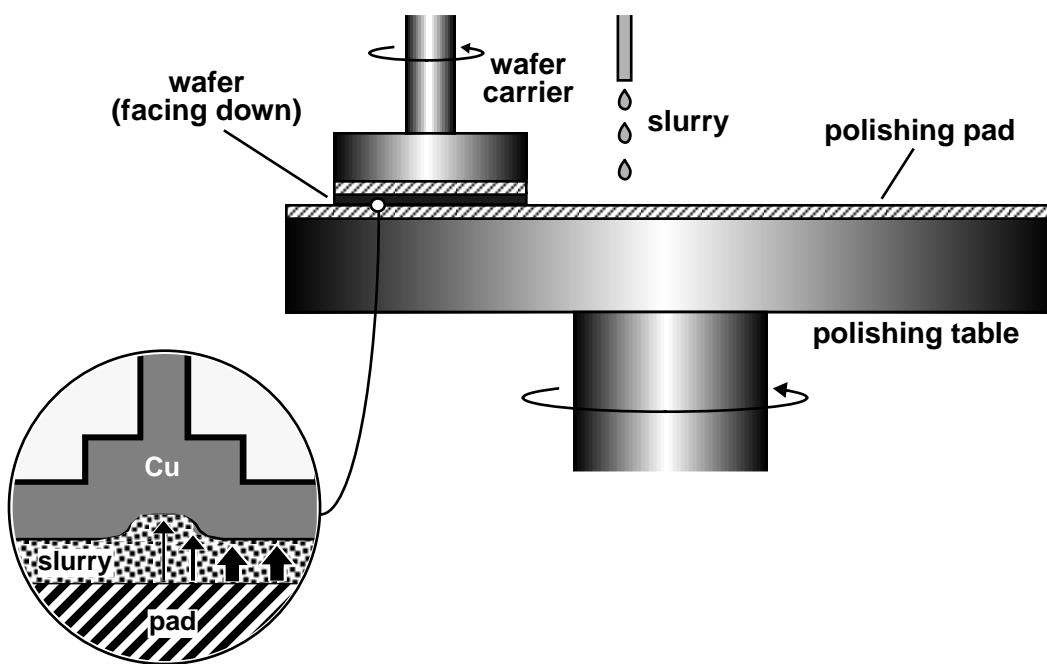


Figure 2-9 Schematic of a typical chemical-mechanical polishing system.

Compared to W CMP, there are several additional challenges unique to Cu CMP [63]. Unlike W, Cu is a relatively soft metal which is easily corroded and is prone to scratches and embedded particles. In addition, Cu CMP is complicated by the underlying conductive barrier layers which must also be removed. Like any CMP process, the post-CMP clean is critical in removing traces of slurry from the polished surface. However, since Cu CMP is inherently a wet process that will liberate Cu^{2+} by-products, the post-CMP clean has the additional burden of removing these ions from the wafer surface in order to minimize the potential of device contamination.

The development of a manufacturable Cu CMP process is arguably the most challenging aspect of Cu integration. Cu CMP process recipes will largely remain proprietary for the few years to come while they provide successful companies with a competitive technology edge.

2.2.5 Dielectric Barrier Passivation

Following Cu CMP, the Cu interconnects must be capped by a dielectric barrier such as PECVD silicon nitride. The nitride is typically deposited at 350–400°C using SiH_4 and NH_3 precursors. Since copper readily oxidizes at these temperatures, certain procedures must be followed to protect the exposed Cu surfaces. For example, in cluster tools, a wafer is loaded into the nitride deposition chamber after being evacuated in the common buffer chamber. The nitride passivation completes the fabrication of one level of Cu wires and vias.

2.3 Summary

This chapter reviewed the process integration of conventional Al and dual-Damascene Cu interconnects. First, Al metallization technology was described with an outline of Al alloy wire and W via fabrication. Next, the dual-Damascene Cu technology was presented. Key technical issues in the various aspects of both integration schemes were highlighted as they pertain to manufacturing. This background information establishes the

Chapter 2: Review of Interconnect Integration

context for understanding Damascene Cu integration with low- κ dielectrics. Low- κ polymer materials are the subject of the following chapter.