Lecture 27

ANNOUNCEMENTS

- **Regular office hours will end on Monday 12/10**
  - Special office hours will be posted on the EE105 website
- **Final Exam Review Session:** Friday 12/14, 3PM, HP Auditorium
  - Video will be posted online by Monday 12/17
- **Final Exam:**
  - Thursday 12/20, 12:30PM-3:30PM, 277 Cory
  - Closed book; 6 pages of notes only
  - Comprehensive in coverage:
    - Material of MT#1 and MT#2, plus MOSFET amplifiers, MOSFET current sources, BJT and MOSFET differential amplifiers, feedback.
    - Qualitative questions on state-of-the-art device technology

Outline

- **IC technology advancement**

  Q: How did we get here?

- **Modern BJT technology**

  Q: What is an HBT?

- **Modern MOSFET technology**

  Q: What are the challenges (and potential solutions) for continued MOSFET scaling?

The IC Market

- The semiconductor industry is approaching $300B/yr in sales

Military
2%

Computers
42%

Communications
24%

Industrial
8%

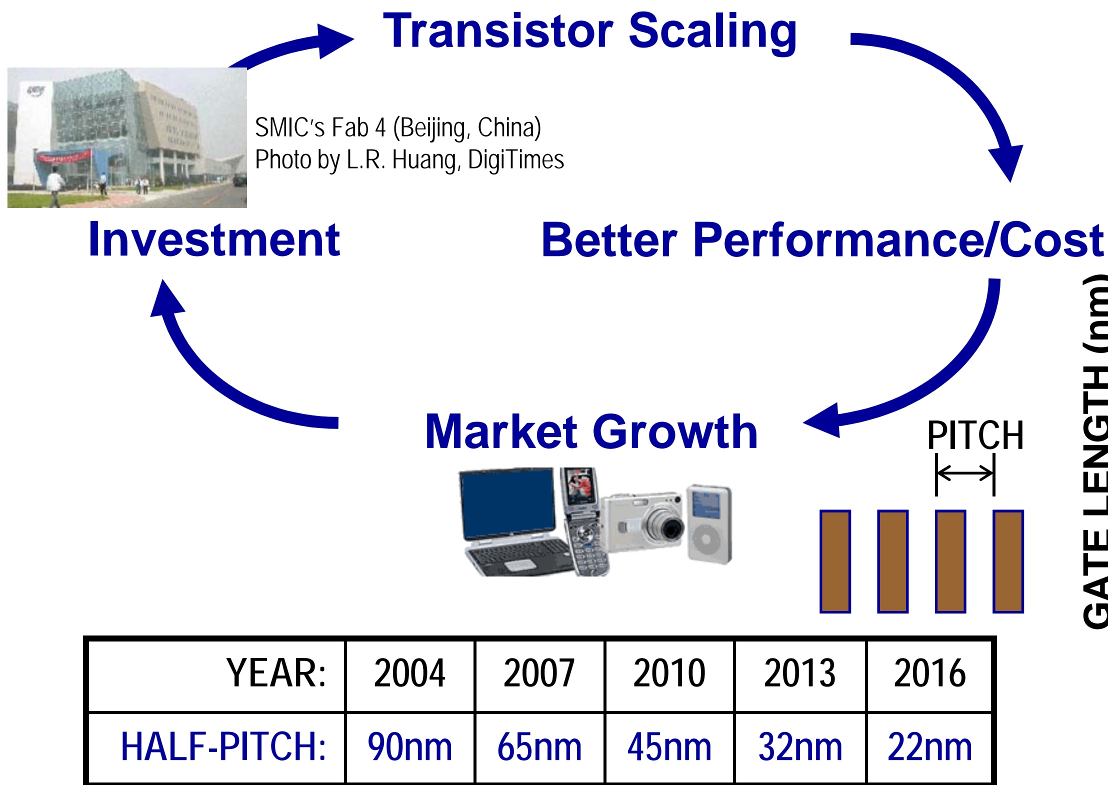
Transportation
8%

Consumer Electronics
16%

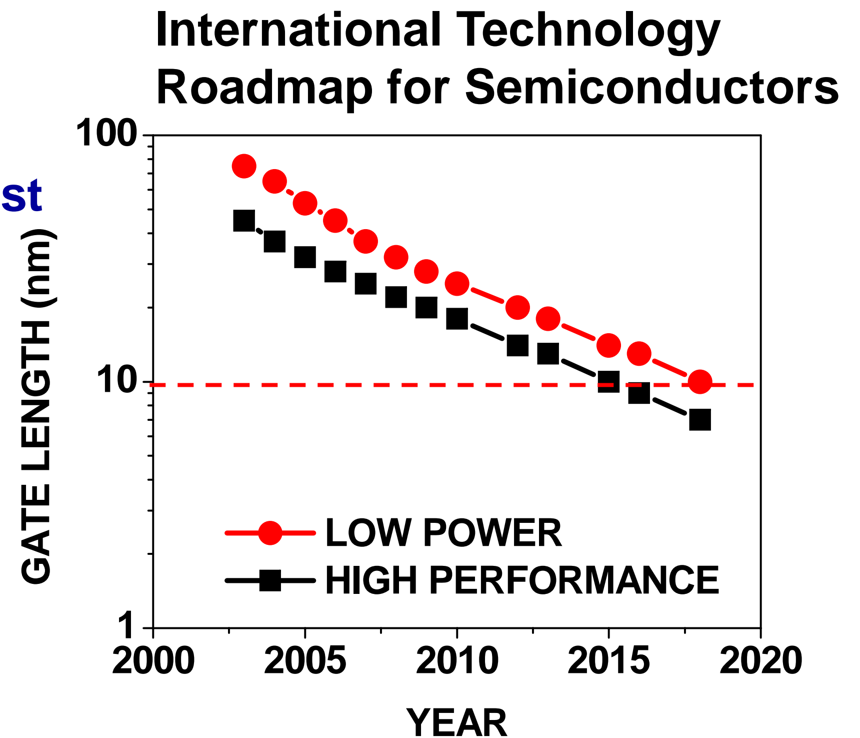
Courtesy of Dr. Bill Flounders, UC Berkeley Microlab

IC Technology Advancement

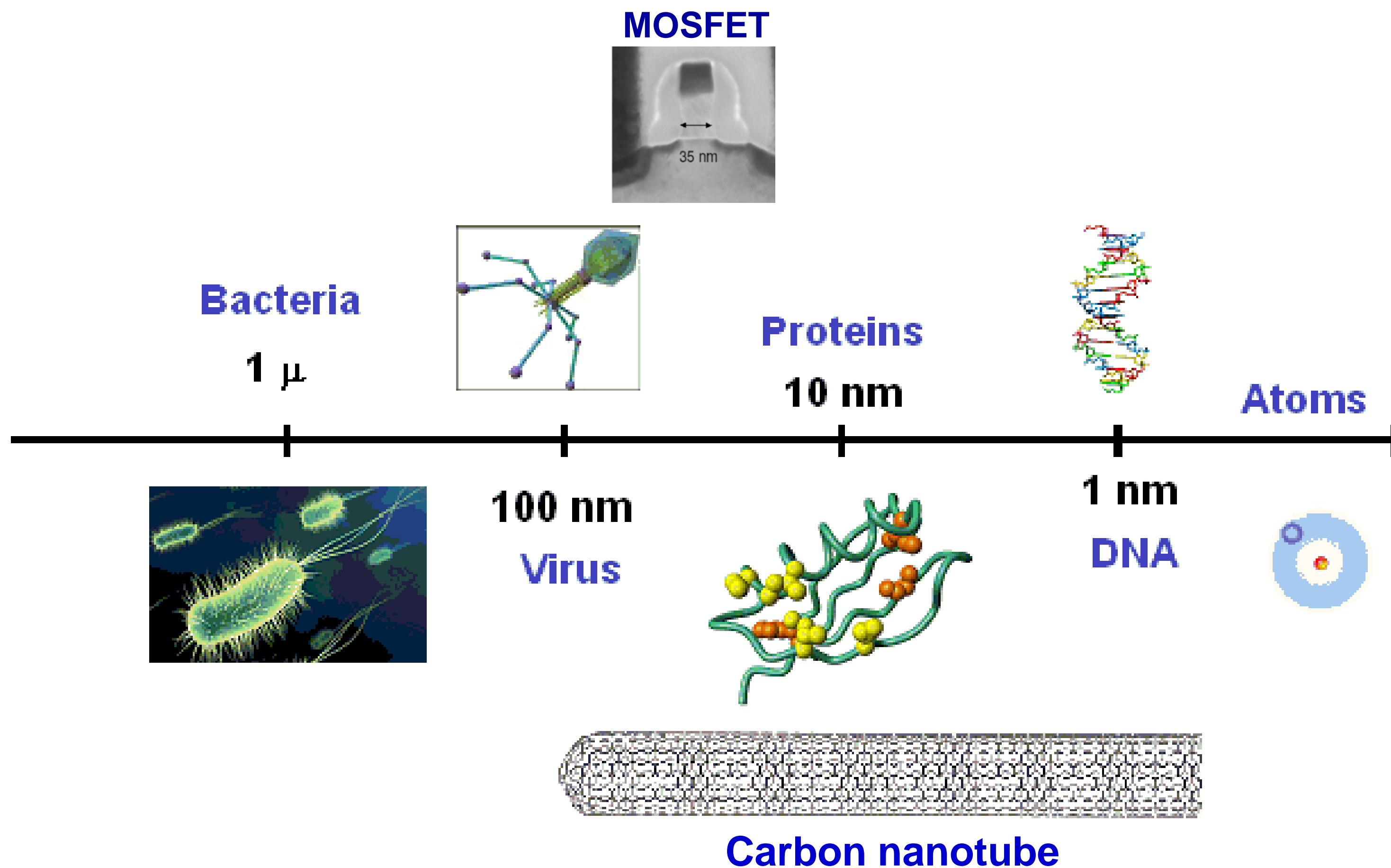
Improvements in IC performance and cost have been enabled by the steady miniaturization of the transistor



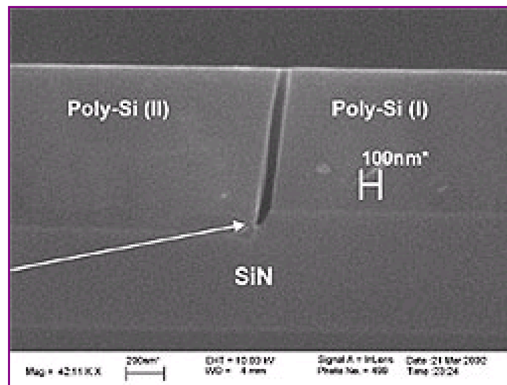
YEAR:	2004	2007	2010	2013	2016
HALF-PITCH:	90nm	65nm	45nm	32nm	22nm



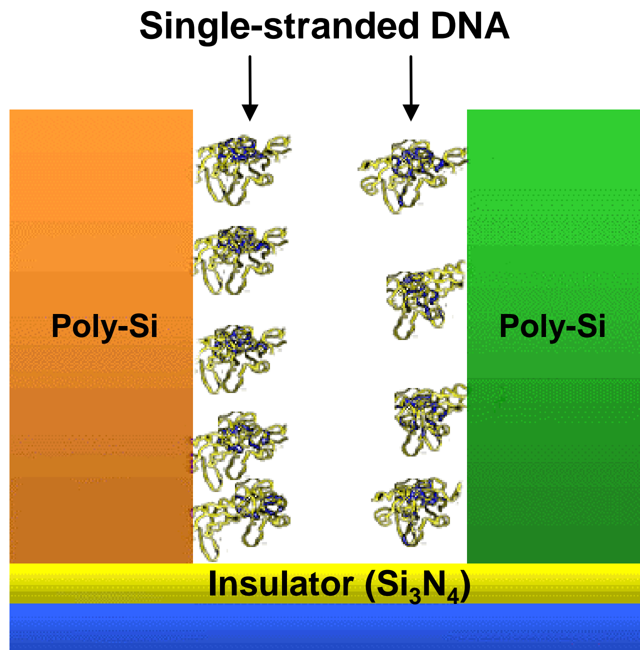
The Nanometer Size Scale

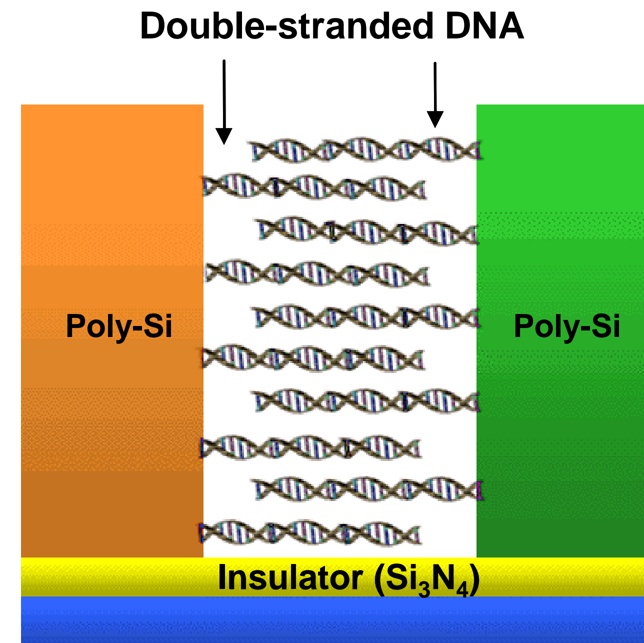


Nanogap DNA Detector



Prof. Luke Lee, BioEngineering Dept.
http://www-biopoems.berkeley.edu/





IC Fabrication

- **Goal:** Mass fabrication (*i.e.* simultaneous fabrication) of many IC "chips" on each wafer, each containing millions or billions of transistors
- **Approach:** Form thin films of semiconductors, metals, and insulators over an entire wafer, and pattern each layer with a process much like printing (lithography).

Planar processing consists of a sequence of additive and subtractive steps with lateral patterning

additive ↓ oxidation, deposition, ion implantation

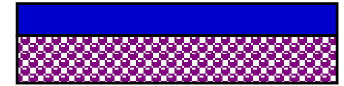
subtractive ↓ etching

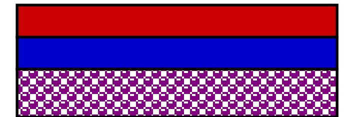
lateral patterning ↓ lithography

Planar Processing

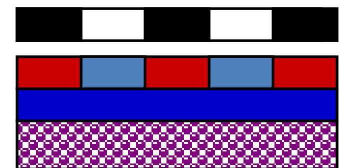
(patented by Fairchild Semiconductor in 1959: J. A. Hoerni, US Patent 3,064,167)

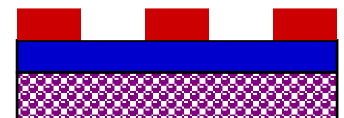
- DEPOSITION of a thin film



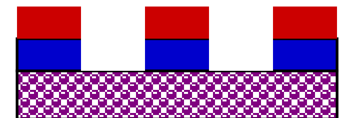


- LITHOGRAPHY
  - Coat with a protective layer
  - Selectively expose the protective layer
  - Develop the protective layer

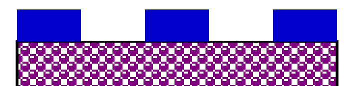




- ETCH to selectively remove the thin film

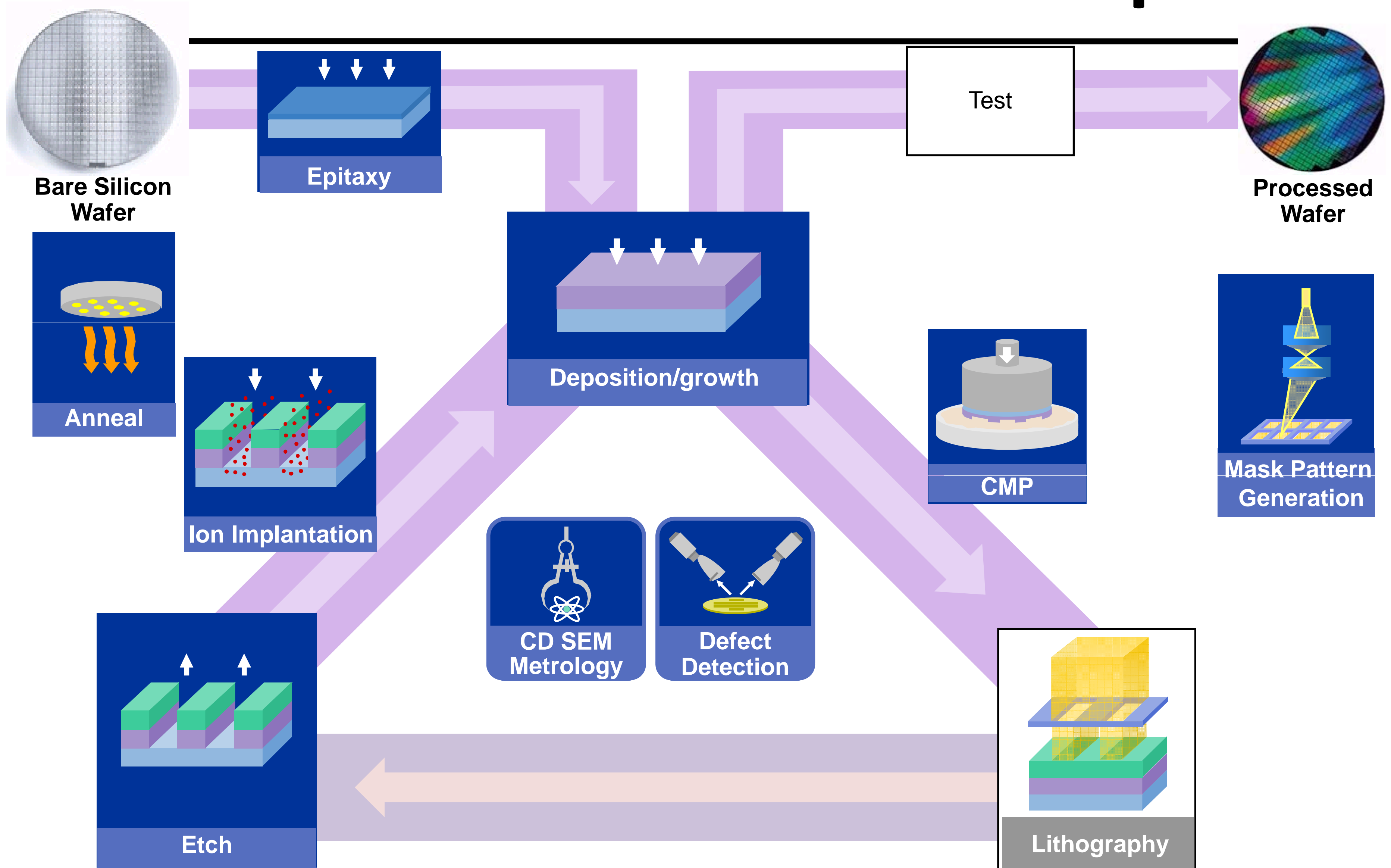


- Strip (etch) the protective layer



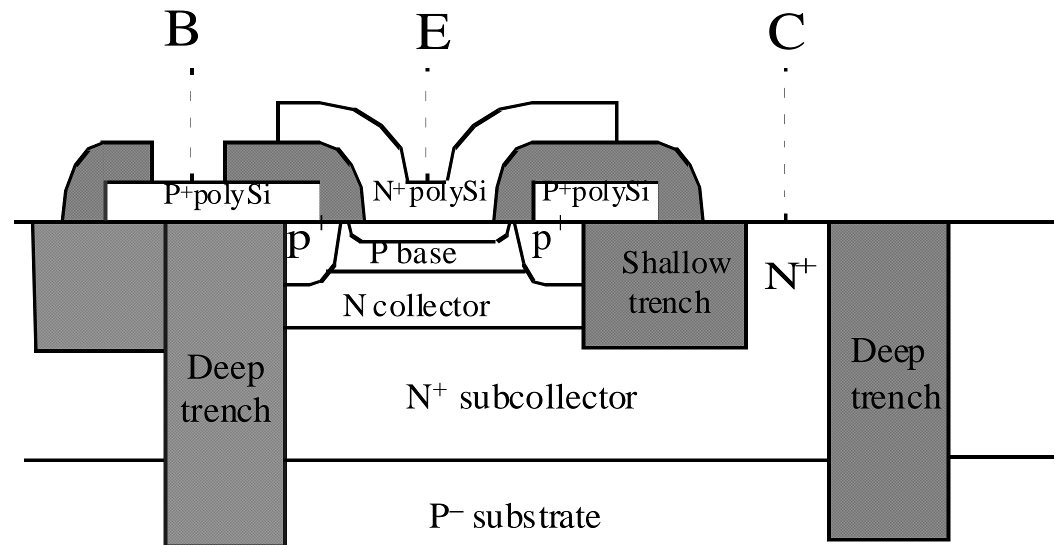
Courtesy of Dr. Bill Flounders, UC Berkeley Microlab

Overview of IC Process Steps



Courtesy of Dr. Bill Flounders, UC Berkeley Microlab

Modern BJT Structure



Features:

- Narrow base
- n+ poly-Si emitter
- Self-aligned p+ poly-Si base contacts
- Lightly-doped collector
- Heavily-doped epitaxial subcollector
- Shallow trenches and deep trenches filled with SiO_2 for electrical isolation

BJT Performance Parameters

- Common emitter current gain, β:

$$\beta \equiv \frac{I_C}{I_B} = \frac{\left(\dfrac{qA_E D_B n_{iB}^2}{N_B W_B}\right)}{\left(\dfrac{qA_E D_E n_{iE}^2}{N_E W_E}\right)} = \frac{D_B n_{iB}^2 N_E W_E}{D_E n_{iE}^2 N_B W_B}$$

- The cutoff frequency, f_T, is the frequency at which β falls to 1. It is correlated with the **maximum frequency of oscillation, f_{max}.**

- Intrinsic gain $g_m r_o \approx \frac{I_C}{V_T} \cdot \frac{V_A}{I_C} = \frac{V_A}{V_T}$

Heterojunction Bipolar Transistor (HBT)

- **To improve β, we can increase n_{iB} by using a base material ($Si_{1-x}Ge_x$) that has a smaller band gap energy**
  - for $x = 0.2$, E_g of $Si_{1-x}Ge_x$ is 0.1eV smaller than for Si

$$n_i^2 \propto \exp\left(\frac{-E_g}{kT}\right)$$

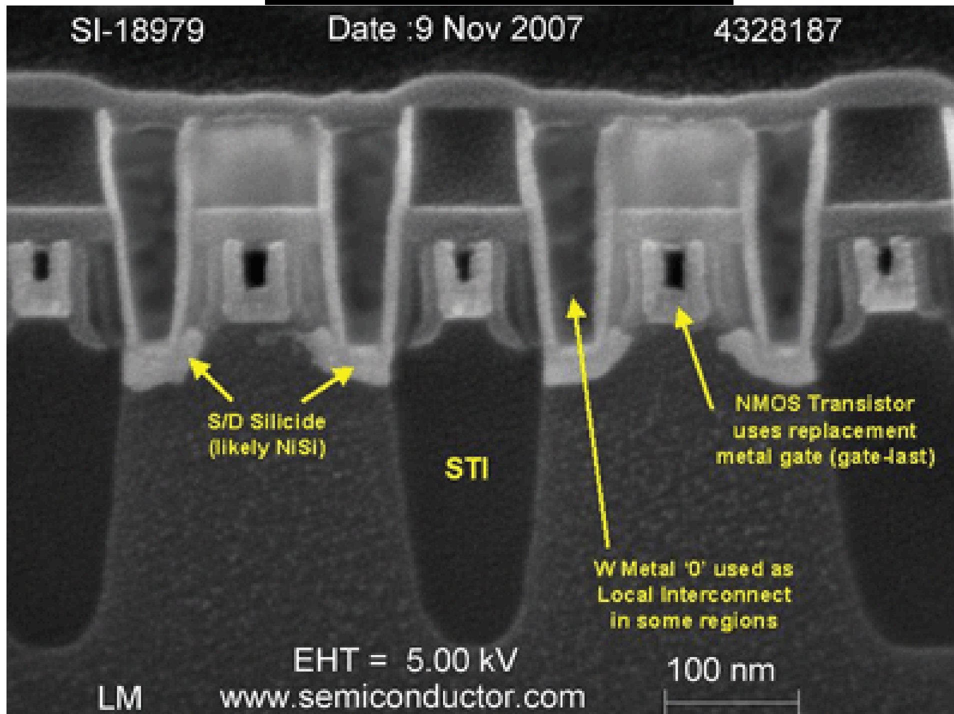
$$\beta = \frac{D_B n_{iB}^2 N_E W_E}{D_E n_{iE}^2 N_B W_B}$$

- **Note that this allows a large β to be achieved with large N_B (even $>N_E$), which is advantageous for**
  - increasing Early voltage (V_A)
  - reducing base resistance

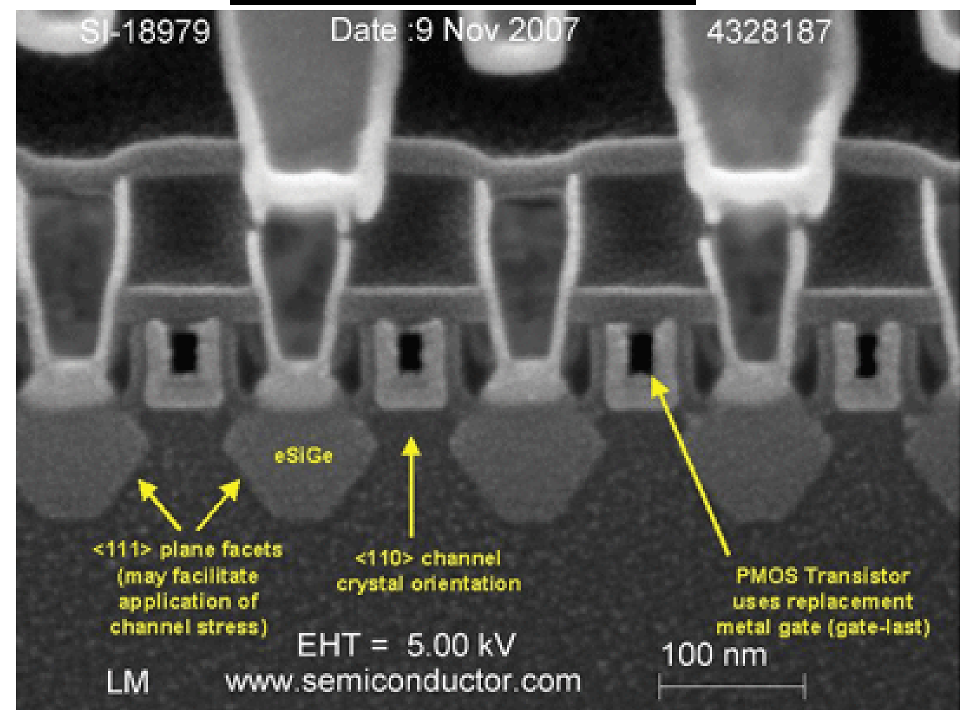
Modern MOSFET Structures

(Intel Penryn©, from www.semiconductor.com)

N-channel MOSFETs



P-channel MOSFETs



- **45nm CMOS technology features:**
  - High-permittivity gate dielectric and metal gate electrodes
  - strained channel regions
  - shallow trench isolation

MOSFET Performance Parameters

- Transconductance (short-channel MOSFET):

$$g_m = vWC_{ox} = \frac{I_D}{V_{GS} - V_{TH}}$$

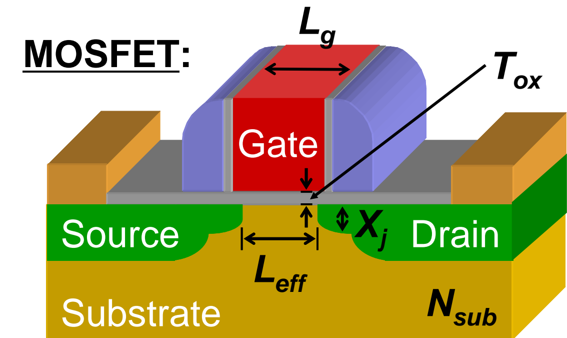
  – The average carrier velocity *v* is dependent on the velocity at which carriers are "injected" from the source into the channel, which is dependent on the carrier mobility

- The cutoff frequency of a MOSFET is given by $2\pi f_T = \frac{g_m}{C_{GS}}$

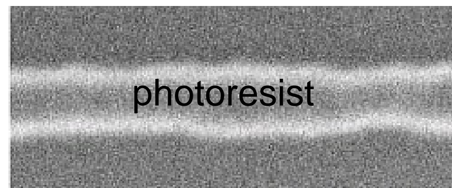
- Intrinsic gain: $g_m r_o = \frac{I_D}{V_{GS} - V_{TH}} \cdot \frac{1}{\lambda I_D} = \frac{1}{\lambda (V_{GS} - V_{TH})}$

MOSFET Scaling Challenges

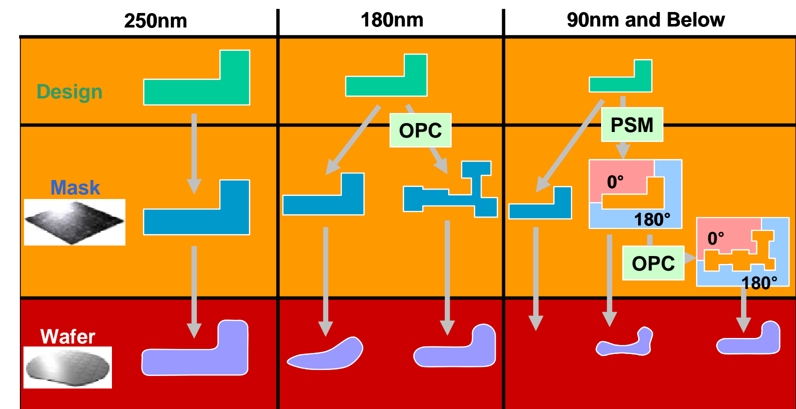
- **Suppression of short-channel effects**
  - Gain in I_{ON} is incommensurate with L_g scaling

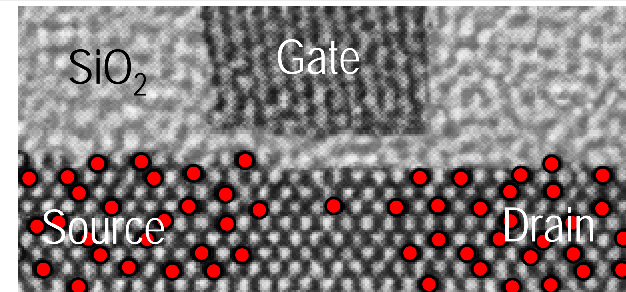


- **Variability in performance**
  - **Sub-wavelength lithography:**
    (Costly resolution-enhancement techniques are needed)
  - **Random variations:**
    - Photoresist line-edge roughness



    - Statistical dopant fluctuations

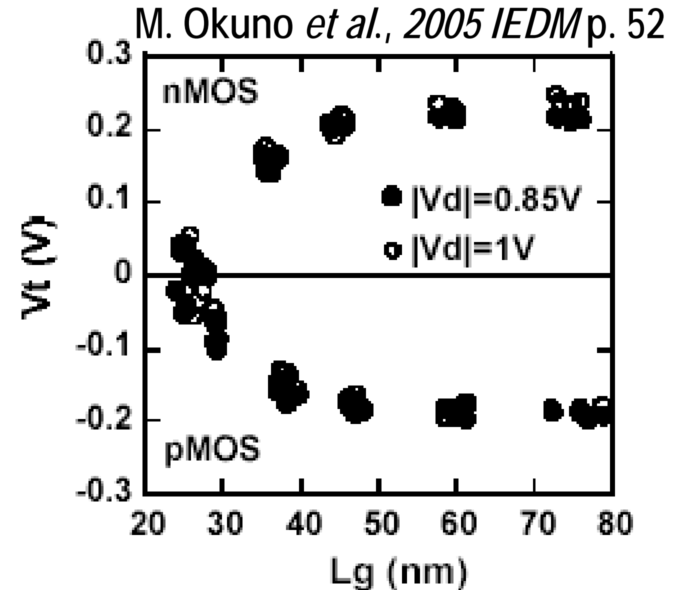




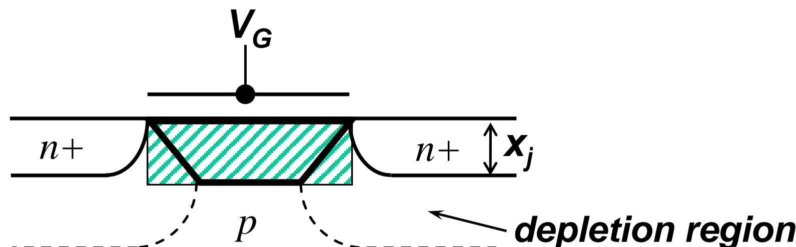
A. Brown *et al.*, *IEEE Trans. Nanotechnology*, p. 195, 2002

"V_{TH} Roll-Off"

- $|V_{TH}|$ decreases with L_g
  - Effect is exacerbated by high values of $|V_{DS}|$



- Qualitative explanation:
  - The source & drain p-n junctions assist in depleting the Si underneath the gate. The smaller the L_g, the greater the percentage of charge balanced by the S/D p-n junctions:

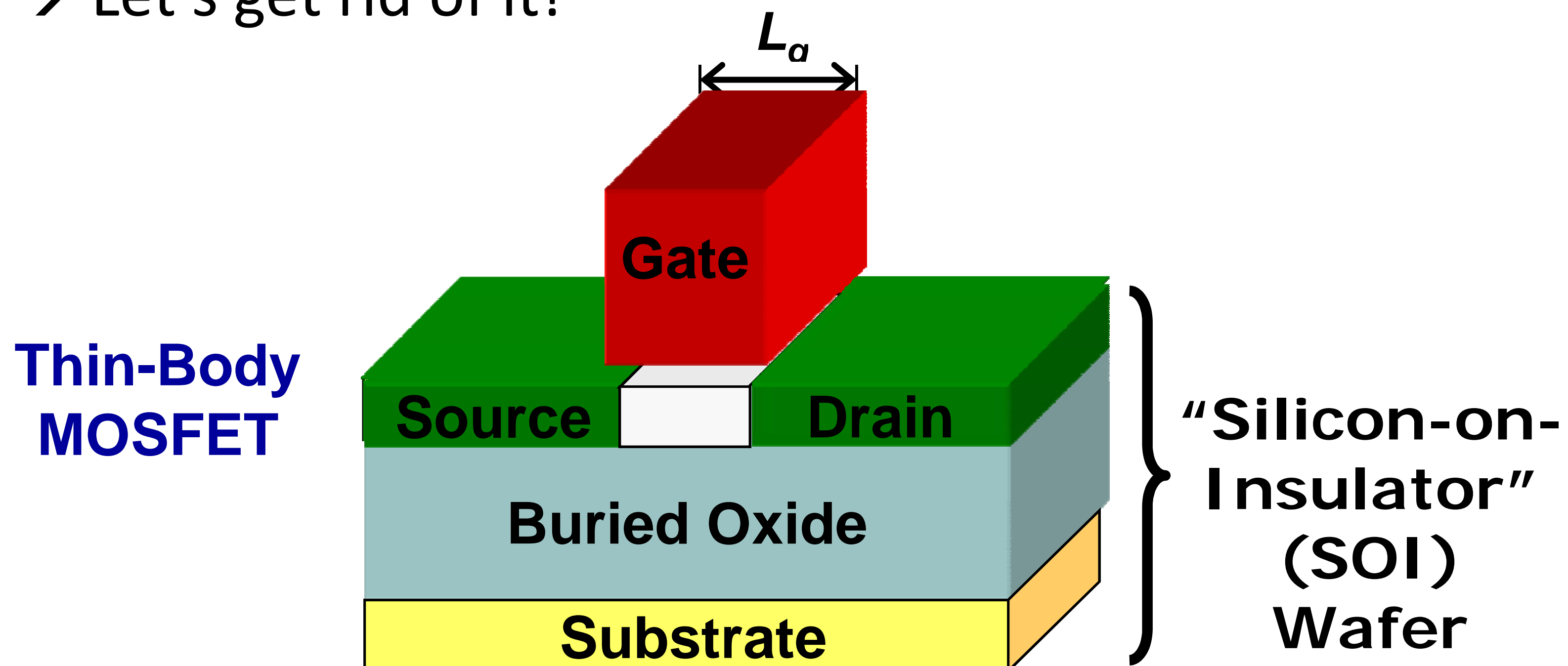


Large L_g: S D

Small L_g: S D

Why New Transistor Structures?

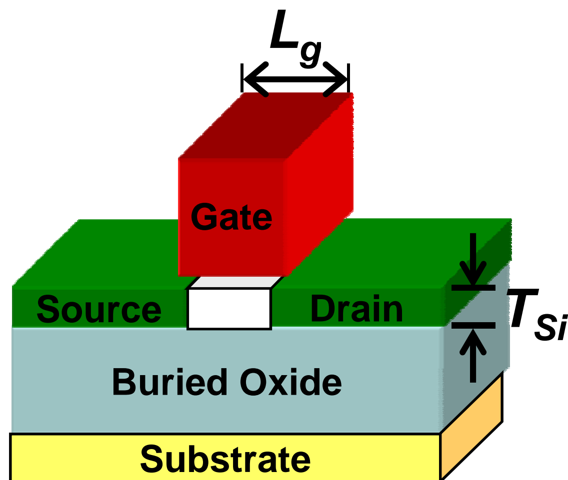
- DIBL must be suppressed to scale down L_g
- Leakage occurs in region far from channel surface
  - → Let's get rid of it!



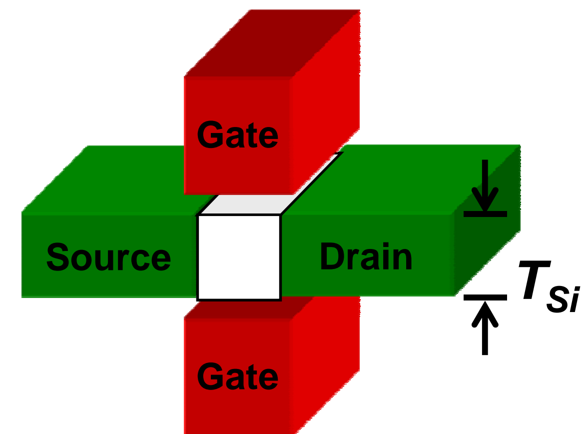
Thin-Body MOSFETs

- Leakage is suppressed by using a thin body **(T_{Si} < L_g)**
  - Channel doping is not needed → higher carrier mobility
- Double-gate structure is more scalable **(to L_g<10nm)**

Ultra-Thin Body (UTB)

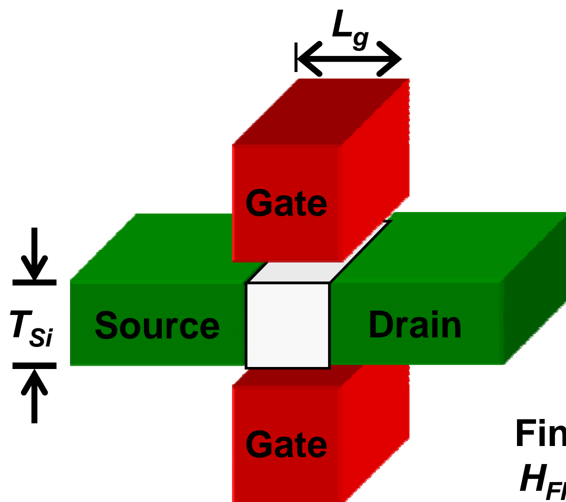


Double-Gate (DG)

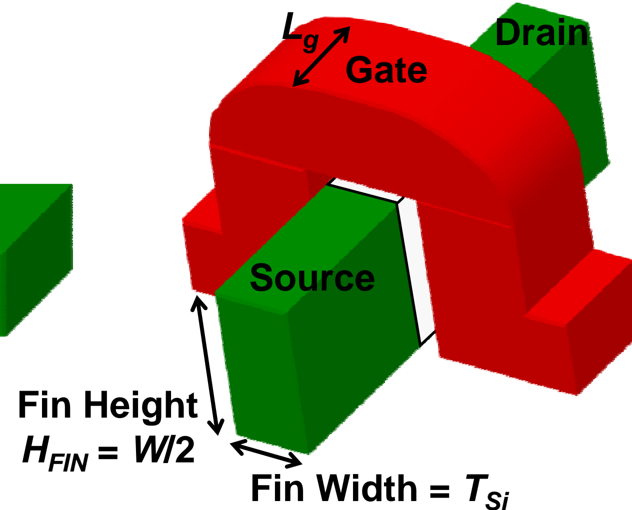


Double-Gate "FinFET"

Planar DG-FET



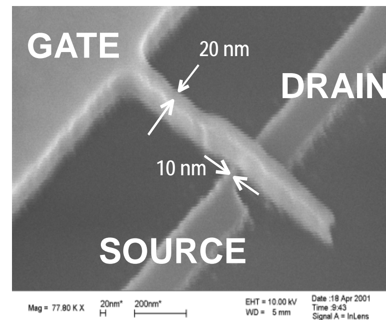
FinFET



D. Hisamoto *et al.* (UC Berkeley), *IEDM Technical Digest*, pp. 1032-1034, 1998

N. Lindert *et al.* (UC Berkeley), *IEEE Electron Device Letters*, pp. 487-489, 2001

15nm L_g FinFET:



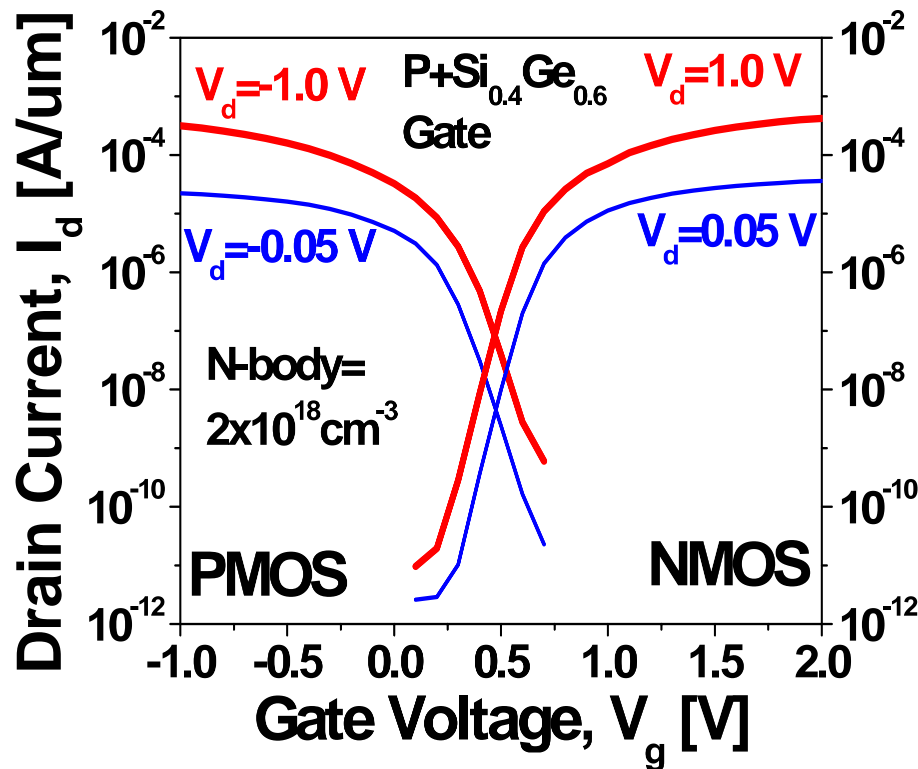
Y.-K. Choi *et al.* (UC Berkeley), *IEDM Technical Digest, pp. 421-424*, 2001

15 nm L_g FinFETs

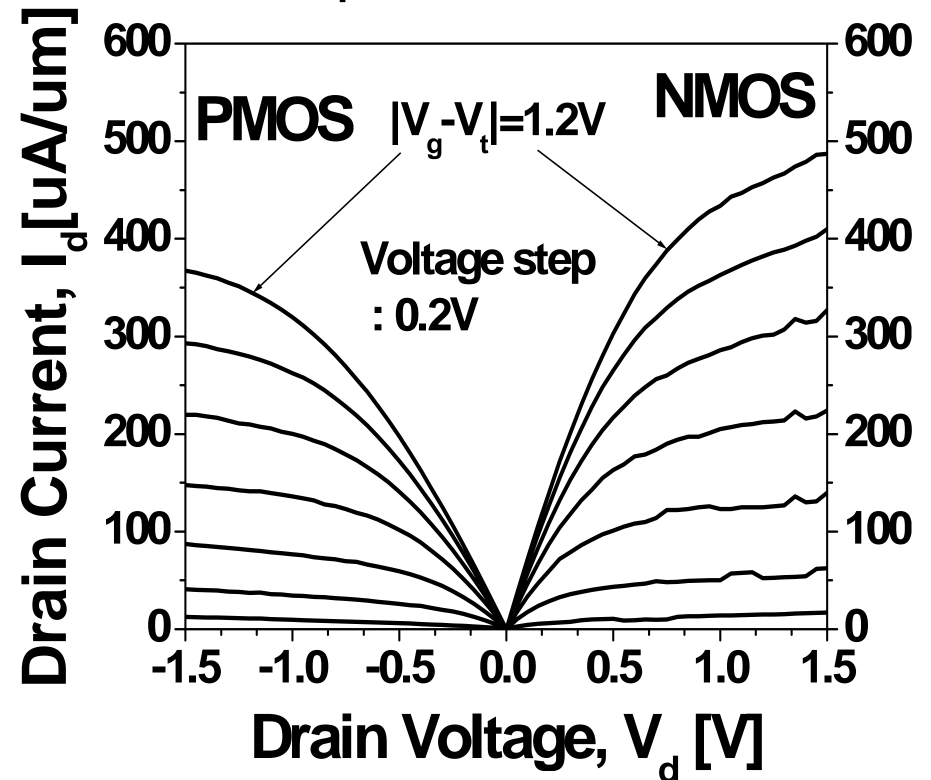
Y.-K. Choi *et al.* (UC Berkeley), *IEDM Technical Digest*, pp. 421-424, 2001

T_{Si} = 10 nm; T_{ox} = 2.1 nm

Transfer Characteristics

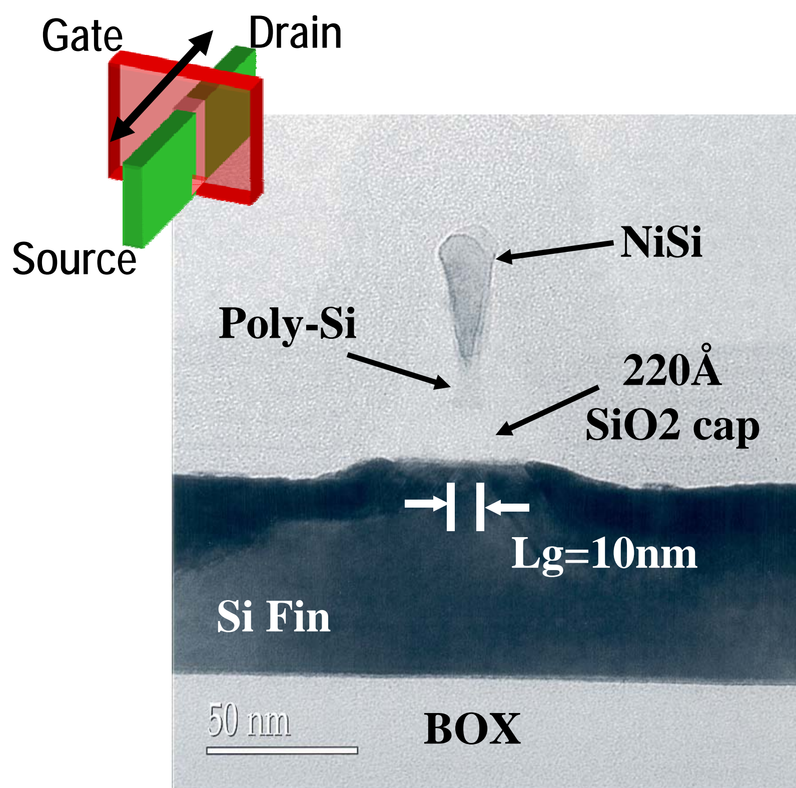


Output Characteristics



10 nm L_g FinFETs

B. Yu *et al.* (AMD & UC Berkeley), *IEDM Technical Digest*, pp. 251-254, 2002



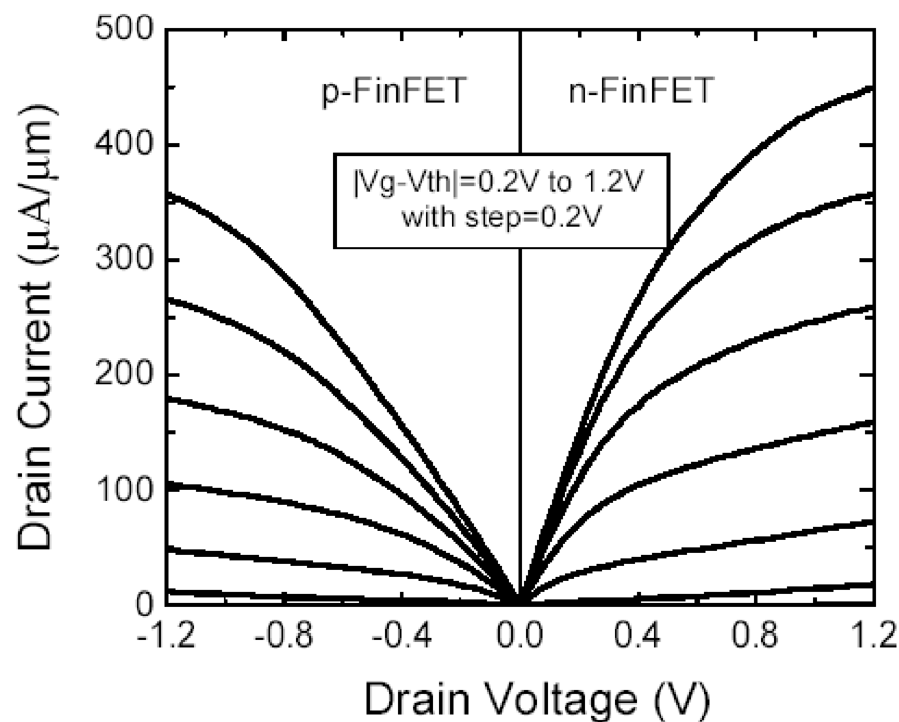
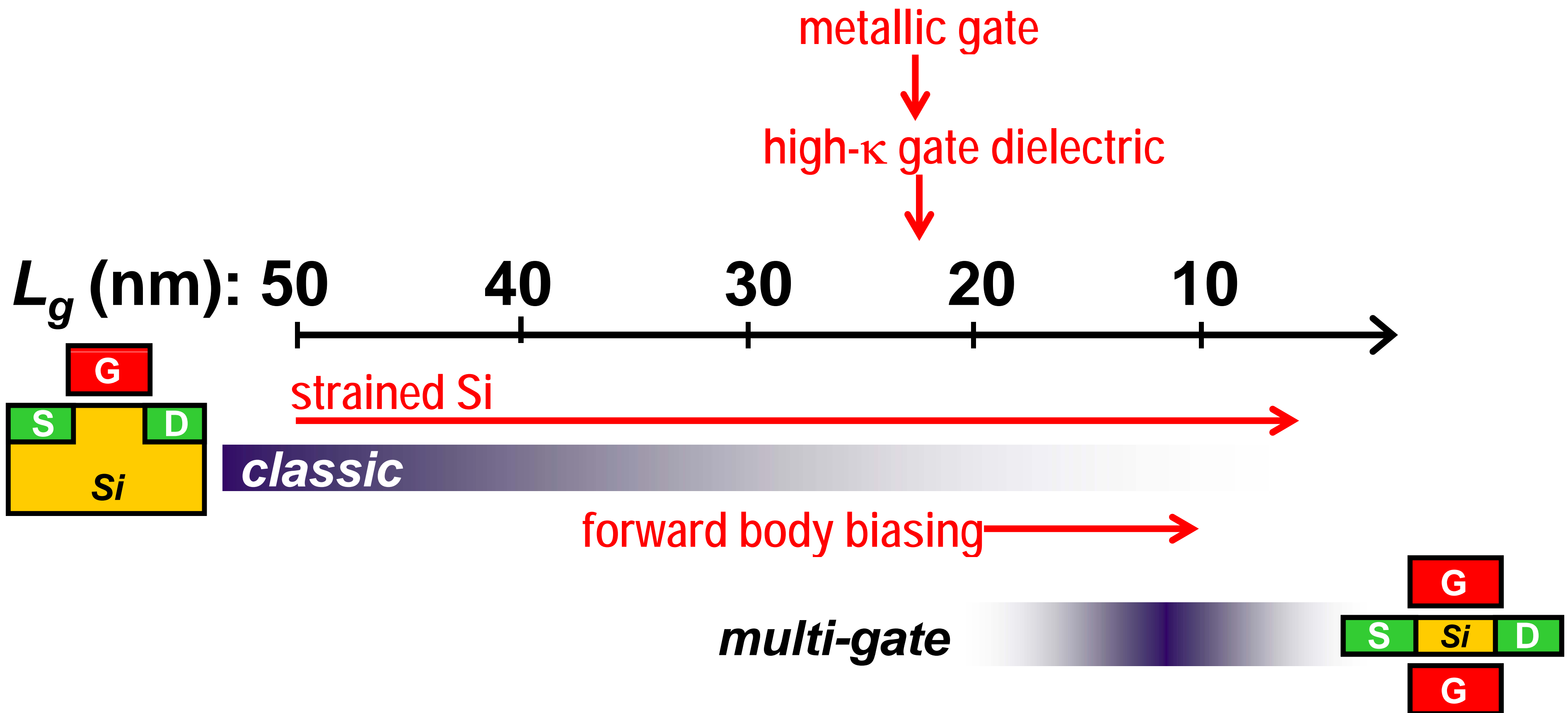


Fig.5 Id-Vd characteristics of 10nm gate length CMOS FinFET transistors.

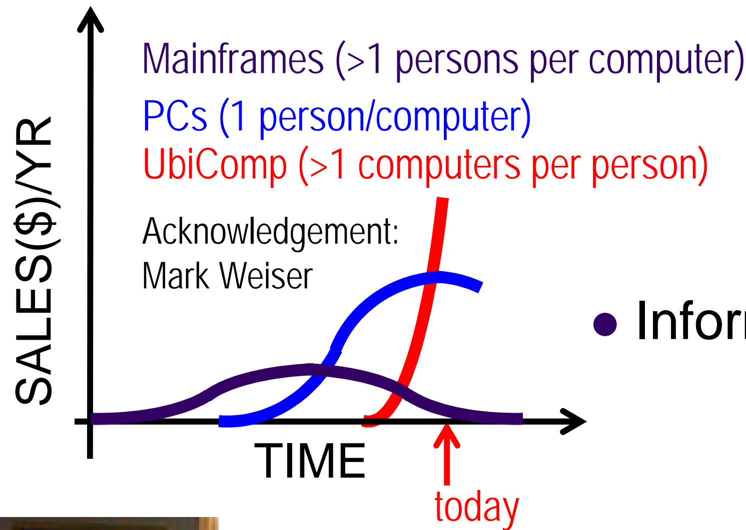
MOSFET Scaling Scenario

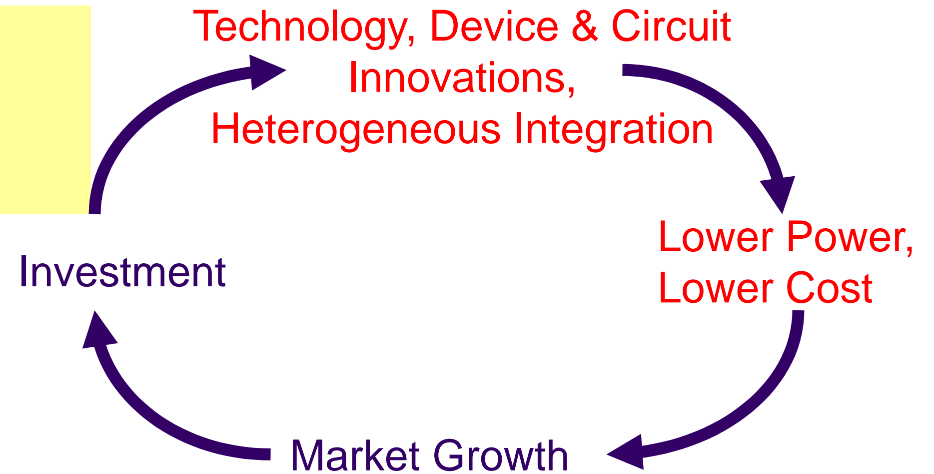
- **Advanced structures will enable Si MOSFET scaling to L_g <10 nm**



The End is Not the Limit !

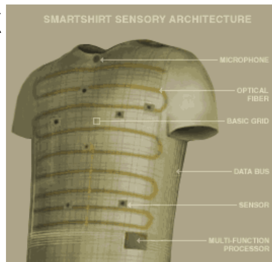
- Innovations in process technology, materials, and device design will sustain the Si revolution





- Information technology for better quality-of-life
  - pervasive
  - embedded
  - human-centered
  - solving societal-scale problems

Philips



Sensatex

Environment

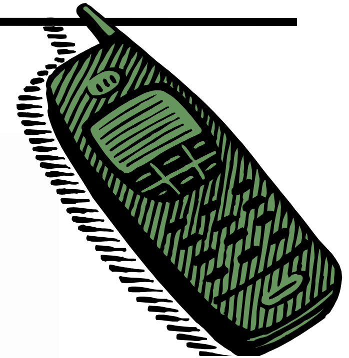
Transportation

Energy

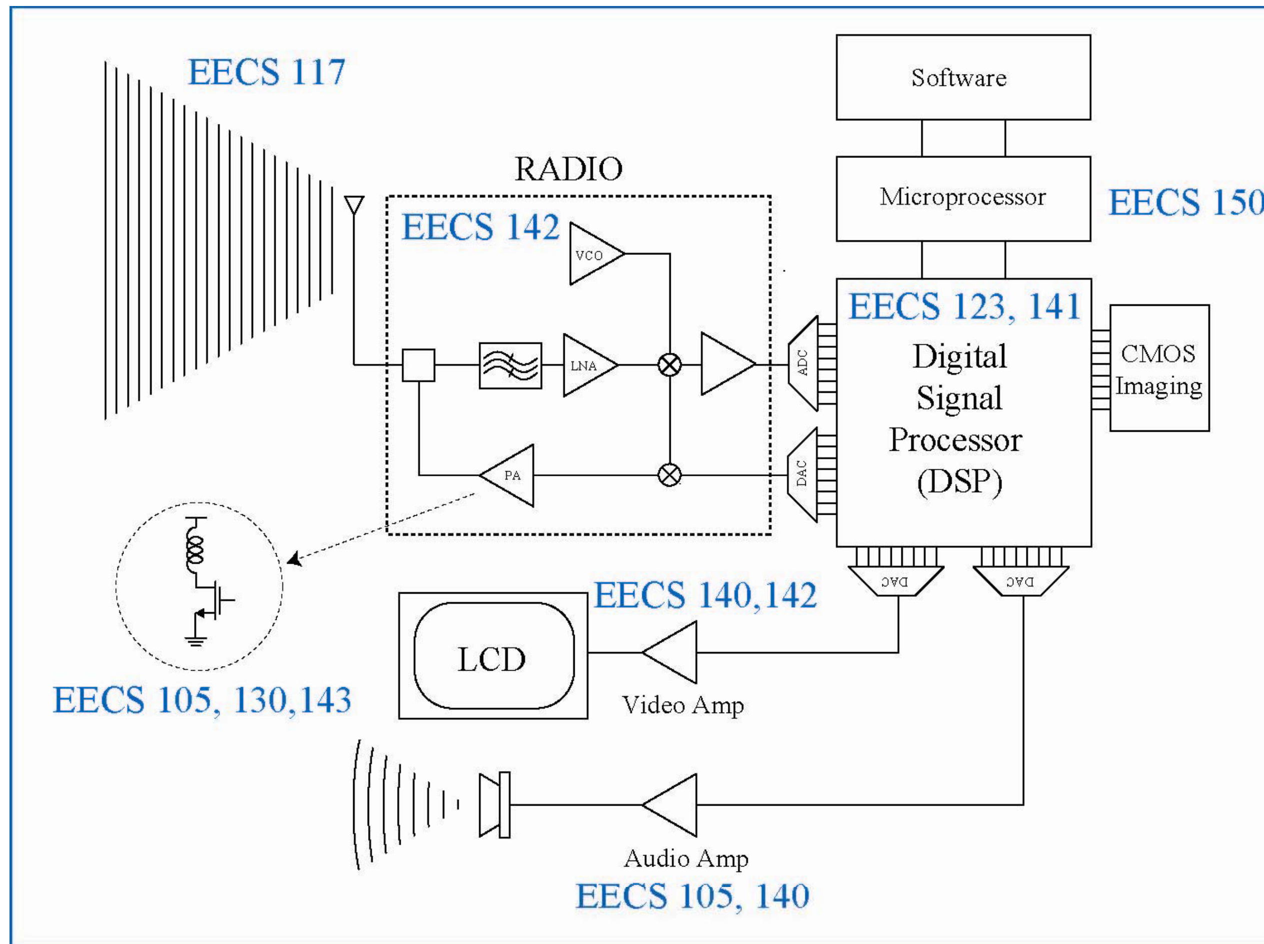
Health care

Disaster response

EECS 105 in the Grand Scheme



- Example electronic system: cell phone



ENTIRE SYSTEM: EECS 120, 126, 121