Performance of

70nm Strained-Silicon CMOS Devices

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UMC

Outline

- Introduction
- Mobility and drive current performance
- Id-sat and Id-lin enhancement
- Self-heating & temperature effect
- Gate oxide & junction leakage
- Unit channel resistance vs. lateral-field
- Ring oscillator power delay
- Summary

Introduction

- *Strained-Si improves mobility by the tensile stress induced energy band split and reduced electron scattering rate.*
- *Band split also causes a narrow bandgap and Vt shift.*

- *Vt shift was compensated to obtain fair comparisons of mobility, drive current, and speed.*
- *Junction leakage due to both defects and $Si_{0.2}Ge_{0.8}$ virtual substrate are investigated.*
- *Both vertical and lateral field dependency of mobility on gate and drain biases are explored by detail comparison of Id-lin and Id-sat gain.*

Strained Silicon Device Structure

- **Optimized strained-Si structure on standard 0.13um foundry process with a heavily nitrided 16A gate oxide.**

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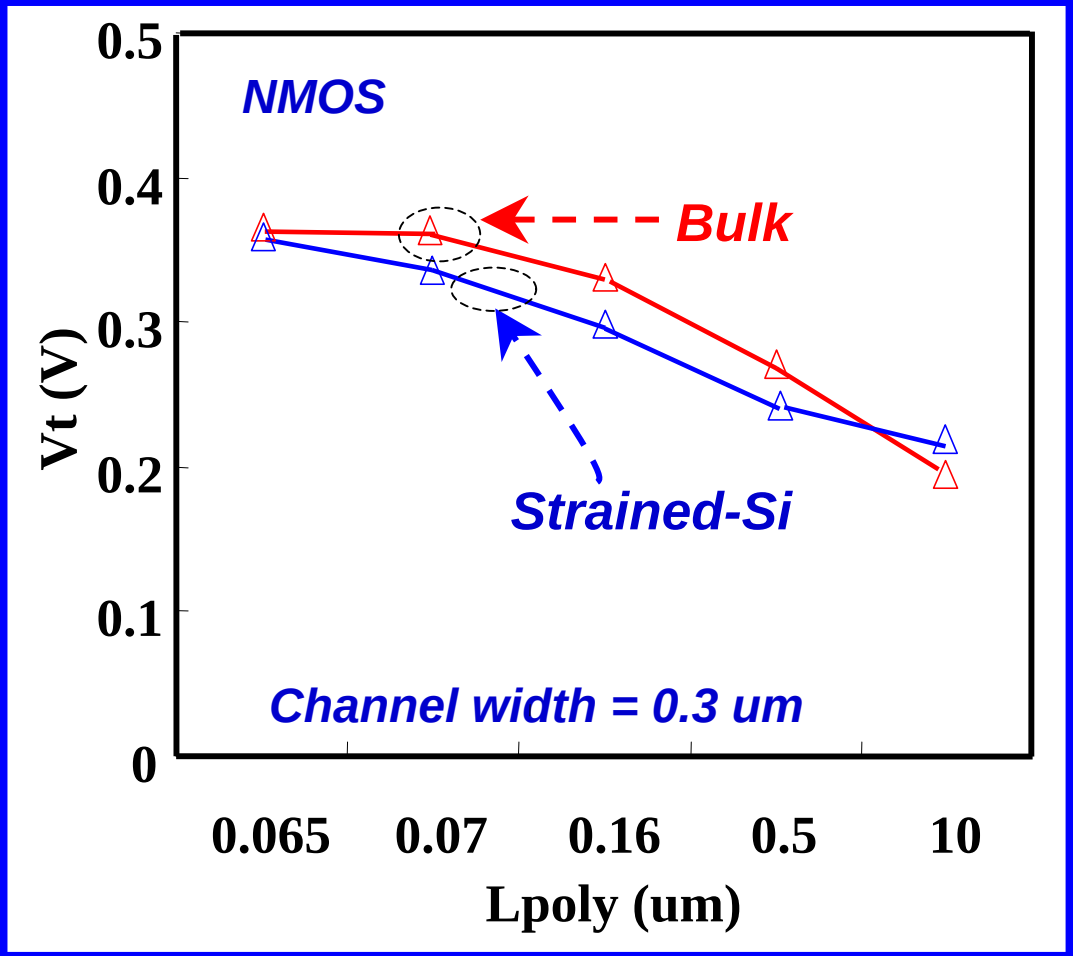
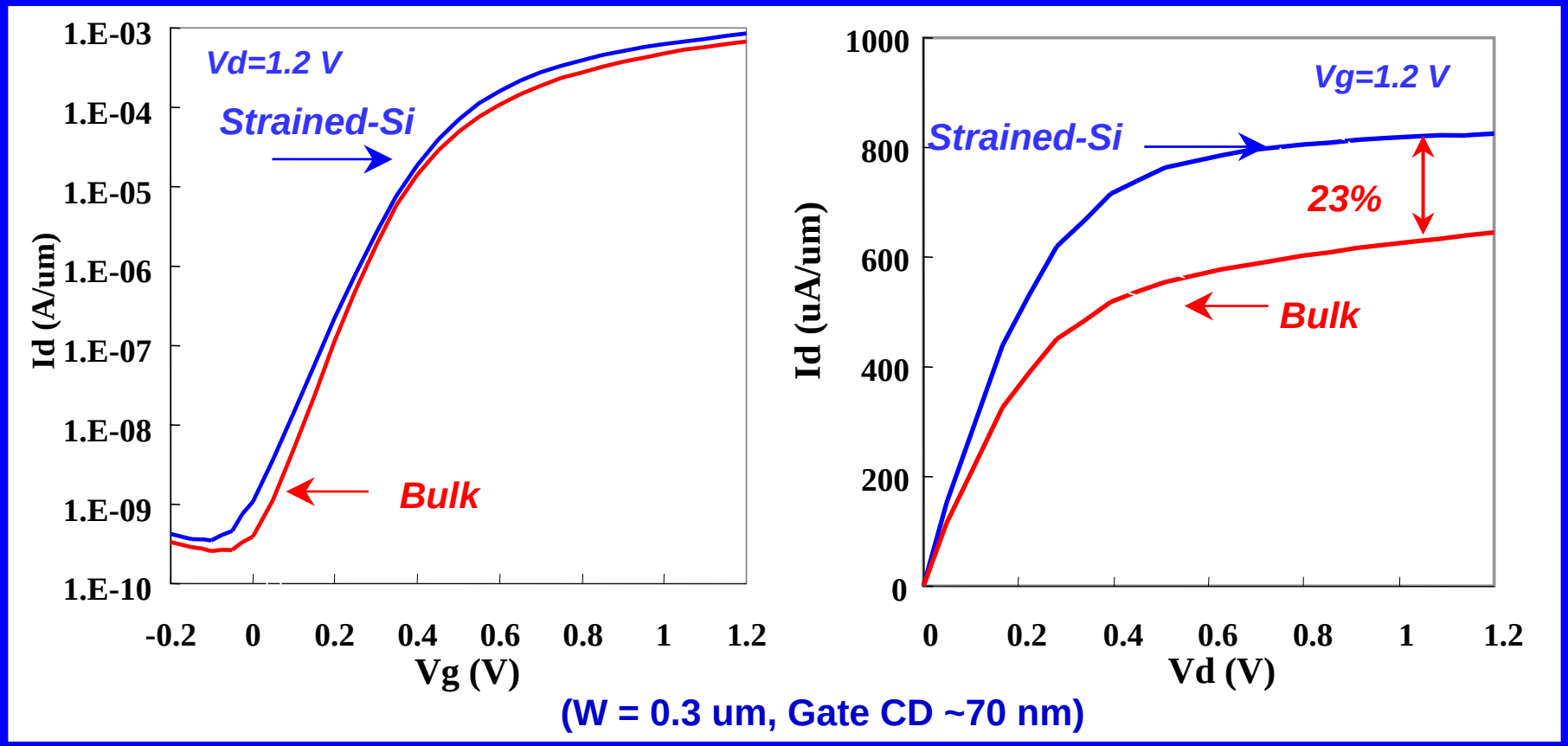
NMOS Vt Roll-off Characteristics



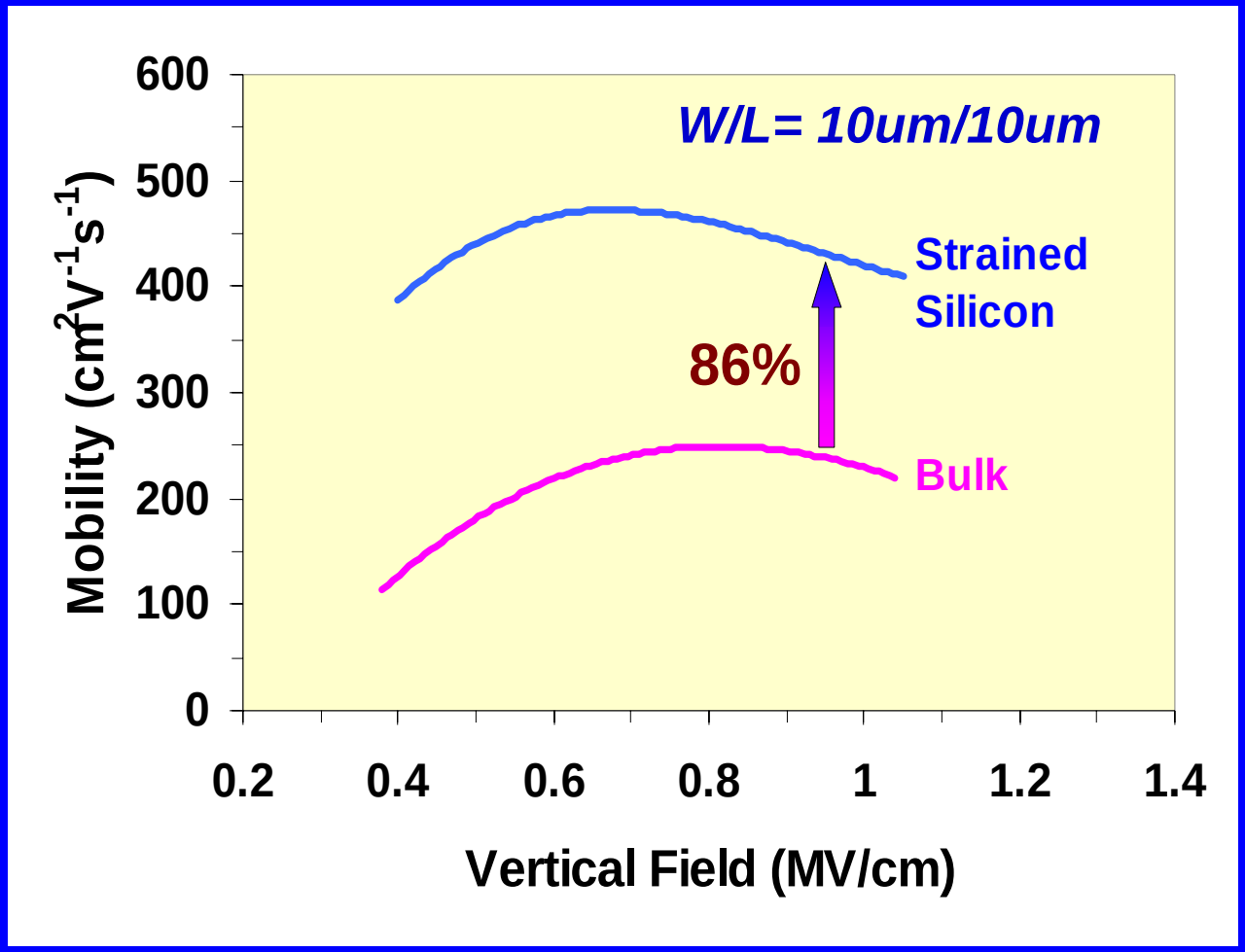
- *The Vt of strained-Si NMOS devices are well matched with bulk-Si devices within 30 mV for gate length from 65 nm to 10 um.*

Short-channel NMOS Performance



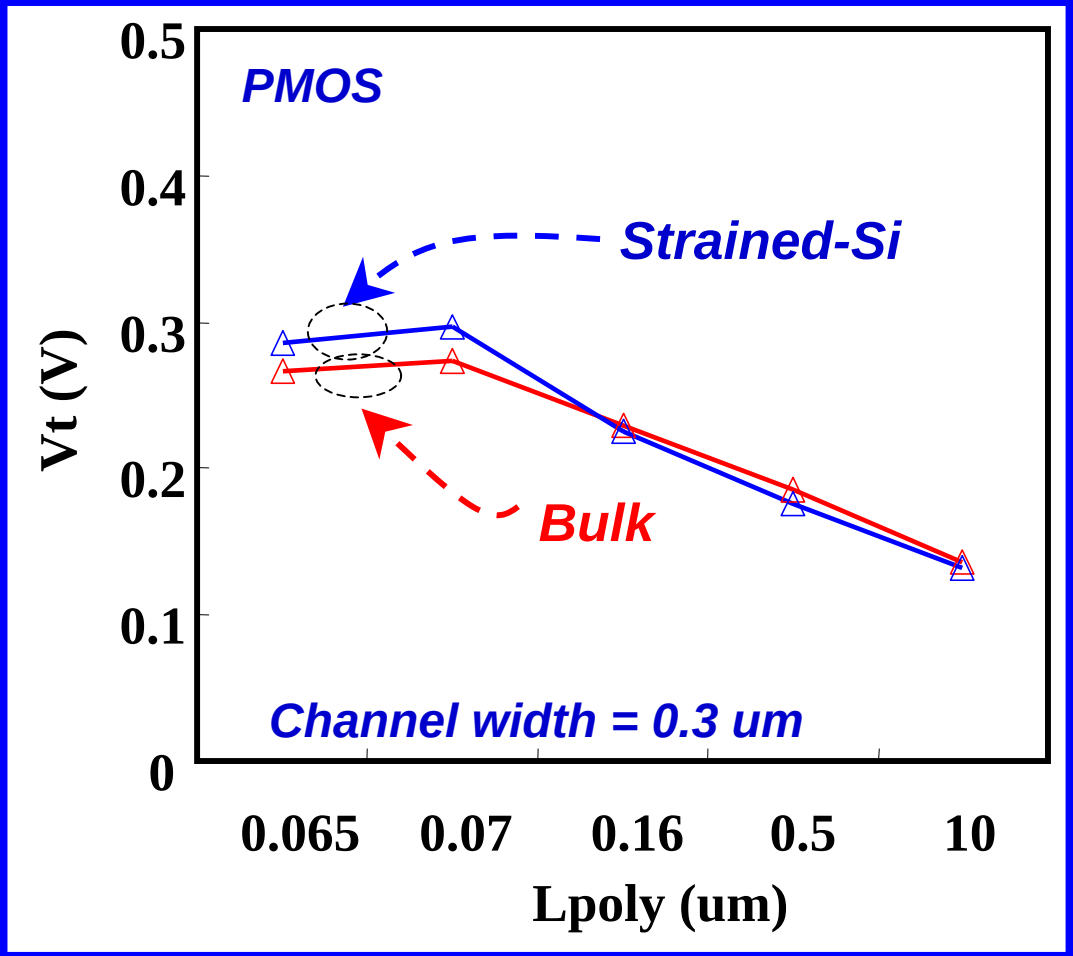
- *Vt of strained-Si device well matched with bulk's (<20 mV).*
- *Ioff of strained-Si device about 3 times larger than bulk's.*
- *Short channel drive current increases 23%.*

Electron Mobility Enhancement



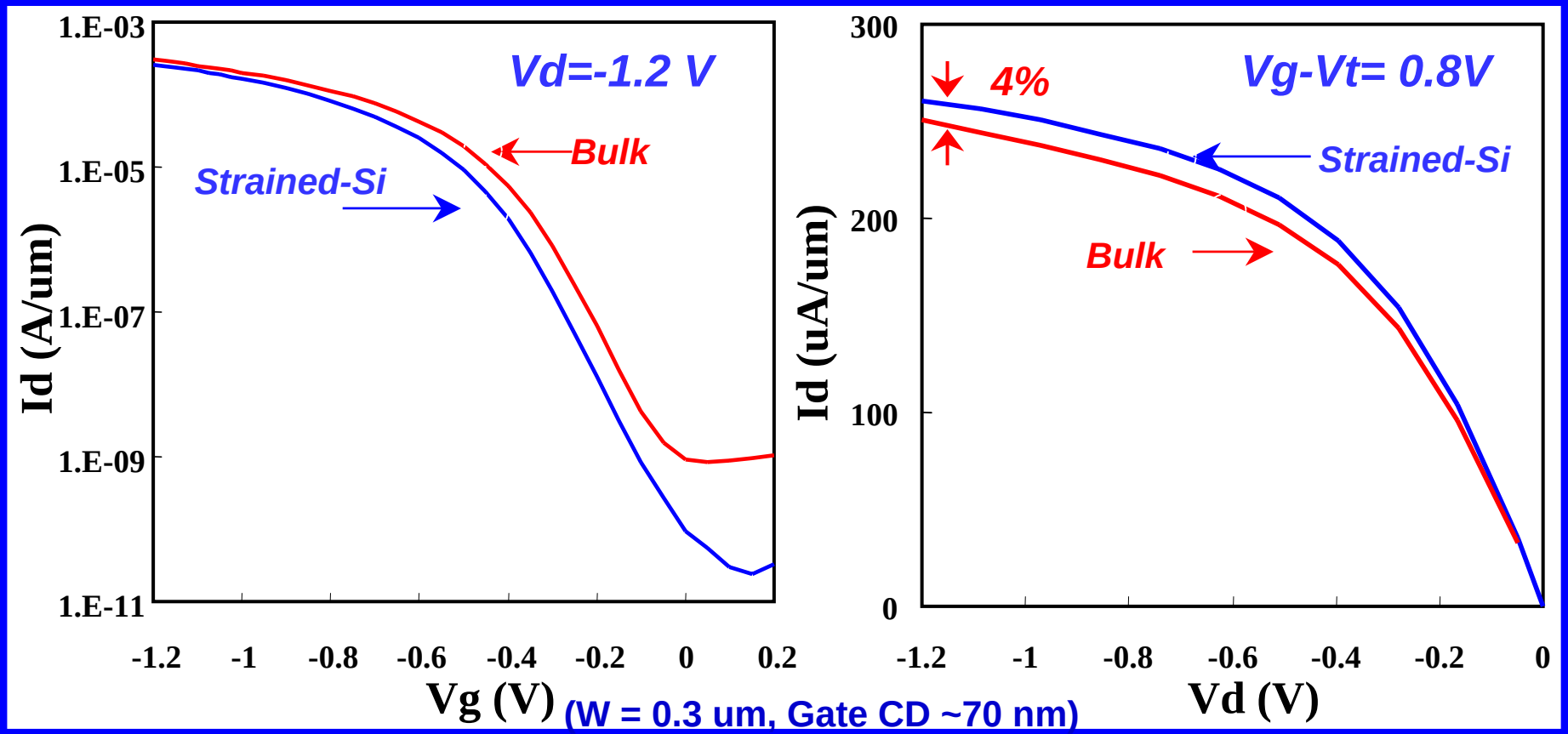
- *Long channel electron mobility of strained silicon devices increased by 86% over bulk devices with matched Vt at high field.*

PMOS Vt Roll-off Characteristics



- *The Vt of strained-Si PMOS devices are matched with bulk-Si devices within 50 mV for gate length from 65 nm to 10 um.*

Short-channel PMOS Performance



- *Short channel PMOS drive current increases 4% for samples with the same Vg -Vt.*

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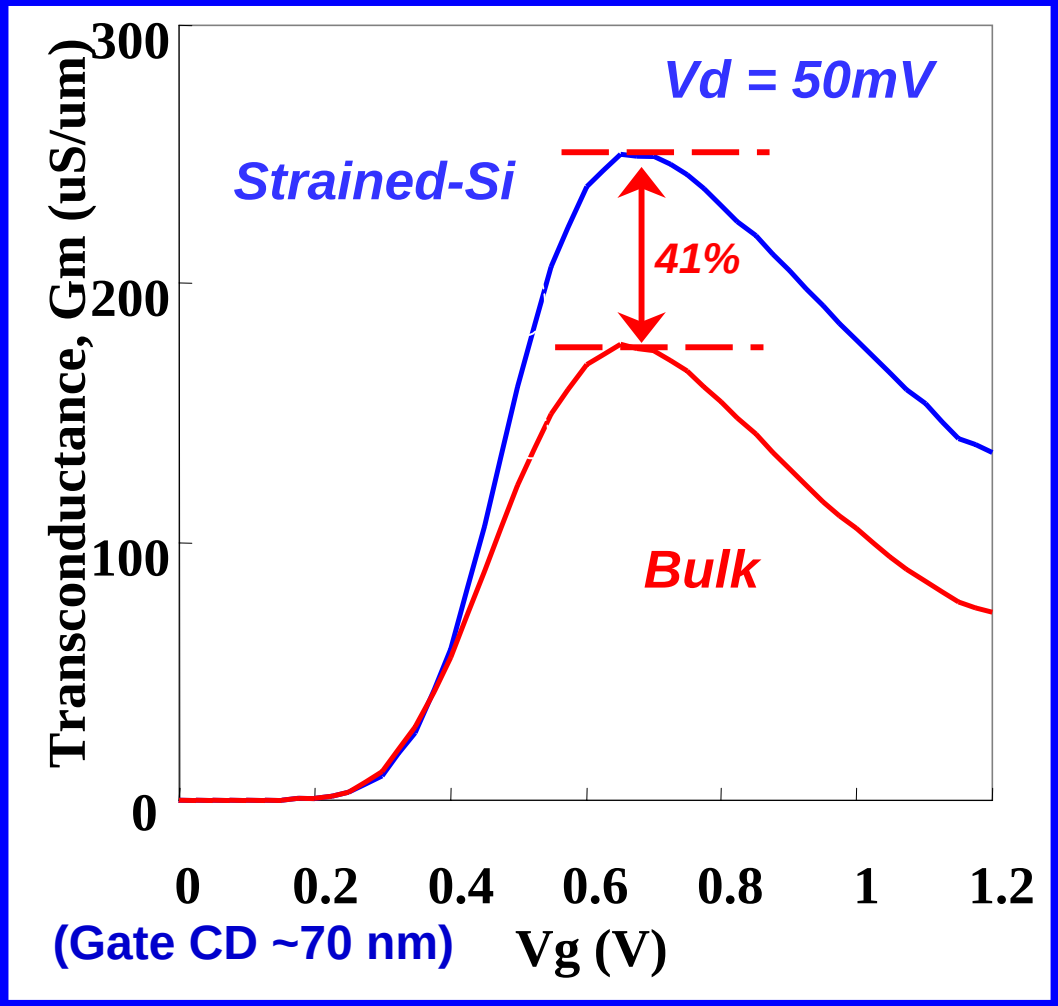
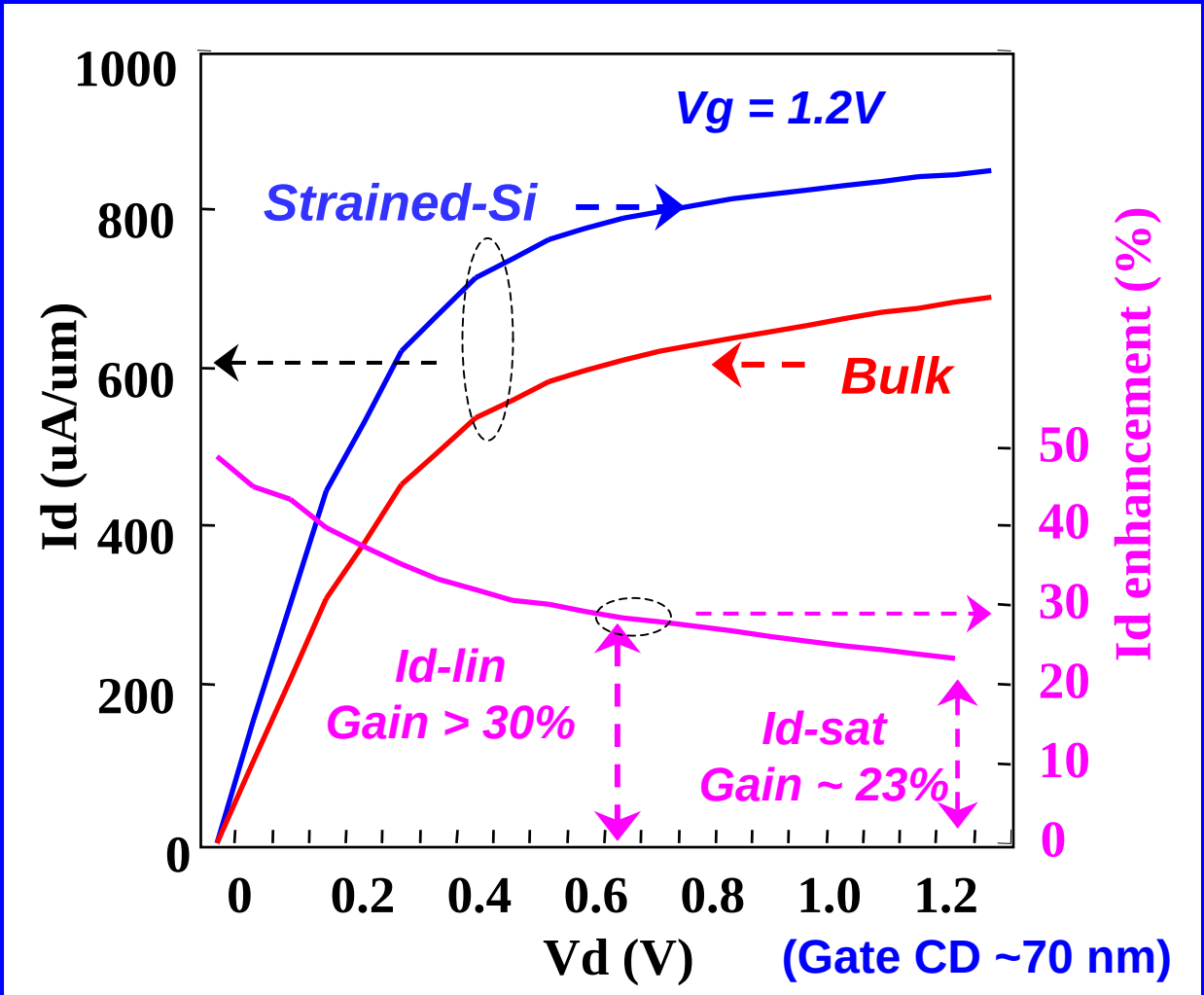
NMOS Transconductance
@ linear region



- *Short Channel Gm-max increases 41% at linear region for Vd = 50 mV.*

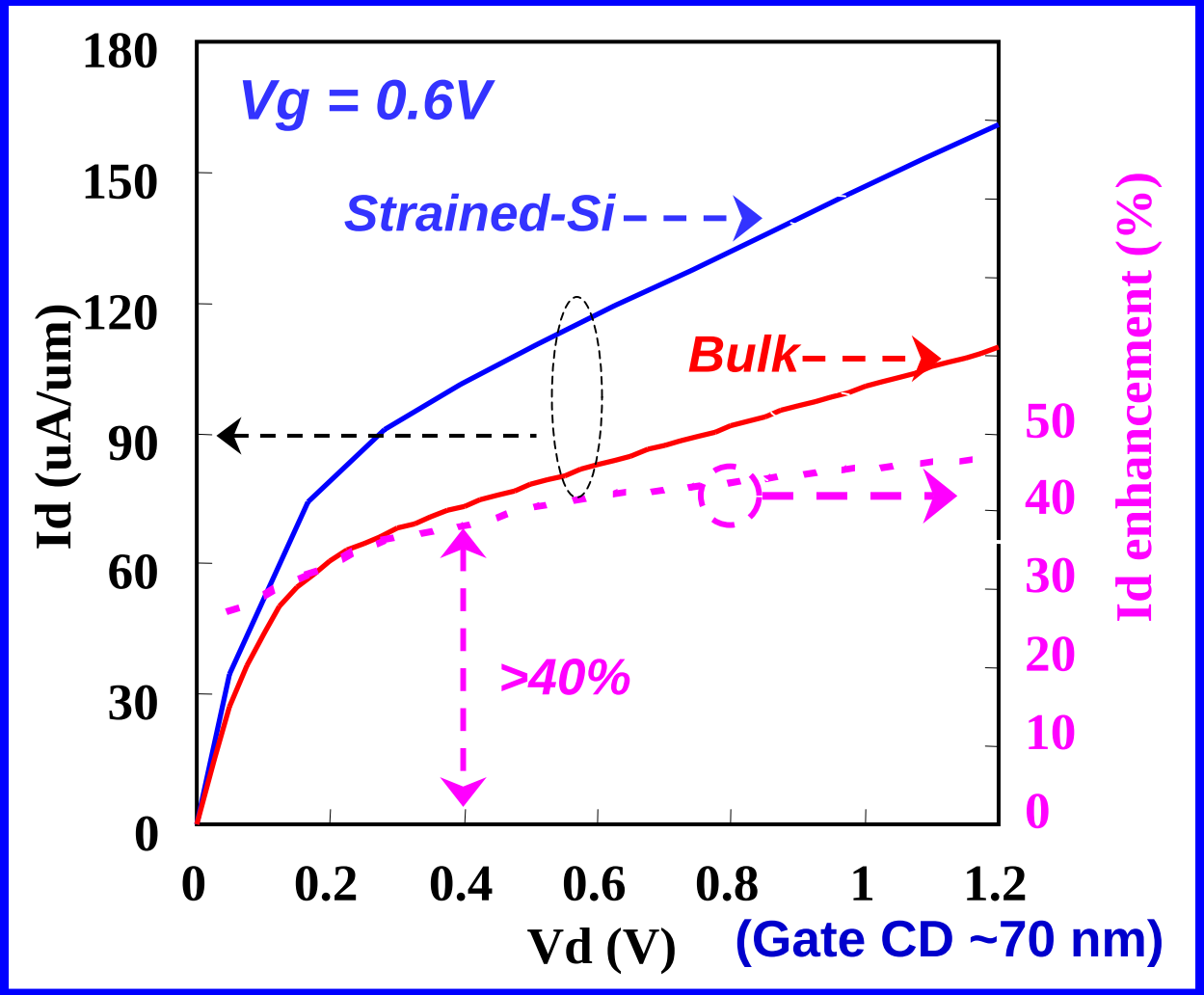
NMOS Id-lin Performance



- *Larger Id-lin gain (>30% for Vd < 0.6V) than Id-sat gain (23%).*

→ *better driving capability for the switching cycle.*

NMOS Drive Current @ Medium Gate Field



- *Larger Id gain (>40%) for medium gate field (i.e. Vg=0.6V).*

→ *better driving capability for the switch cycle.*

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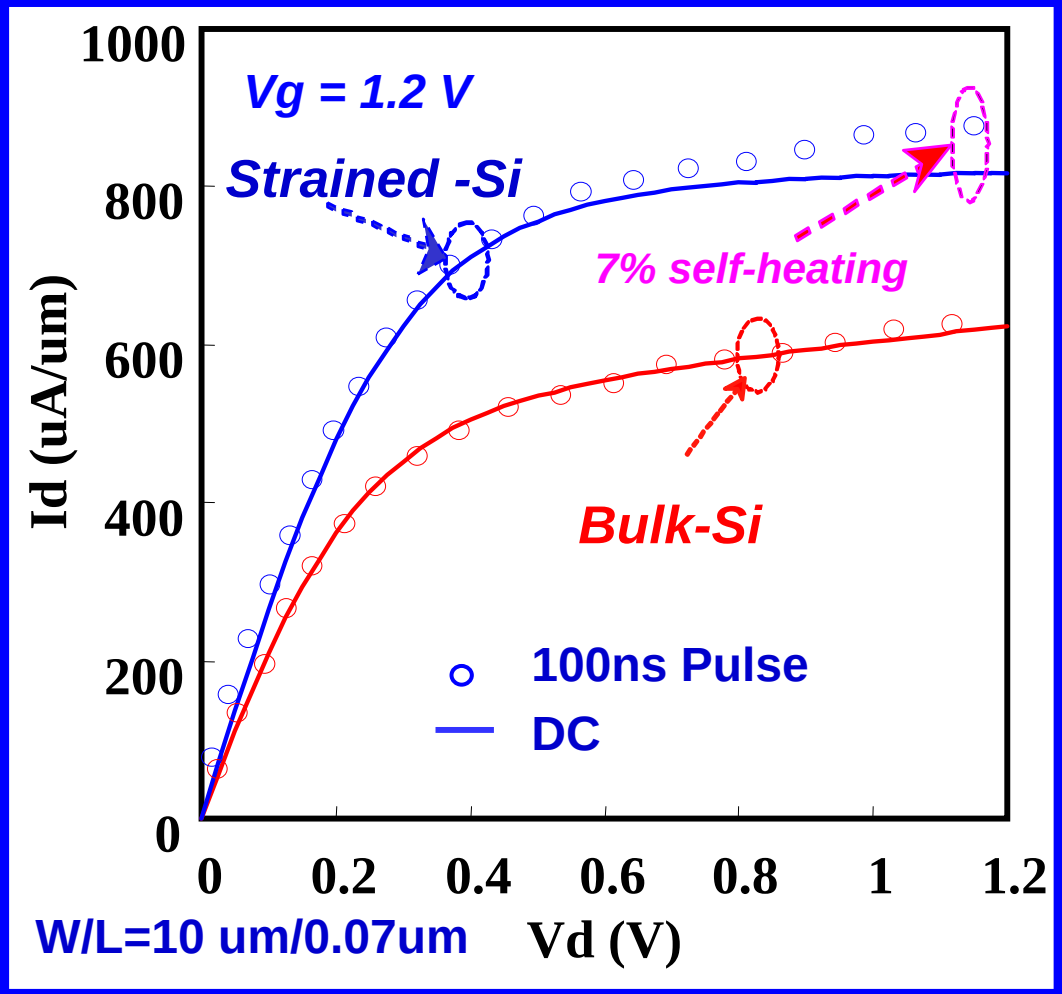
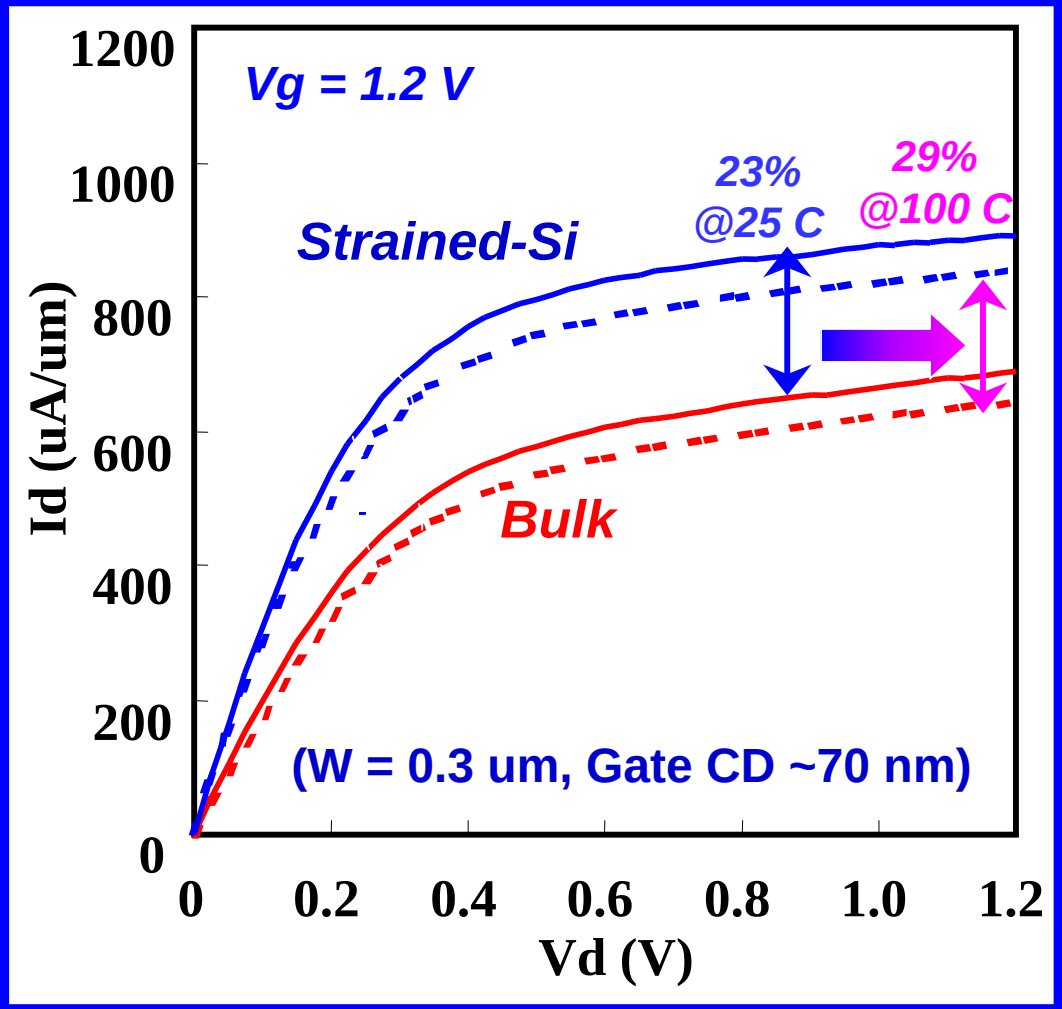
Self-heating Effect

- Pulsed vs. DC measurements



- *Pulsed strained-Si NMOS Id-sat increases 7% than DC results while bulk devices exhibit no self-heating effect.*

Temperature Effect on Drive Current



- *Strained NMOS Id-sat gain over bulk increases from 23% to 29% as temperature rises from 25C to 100C due to less degradation of strained-Si mobility at high temperature.*

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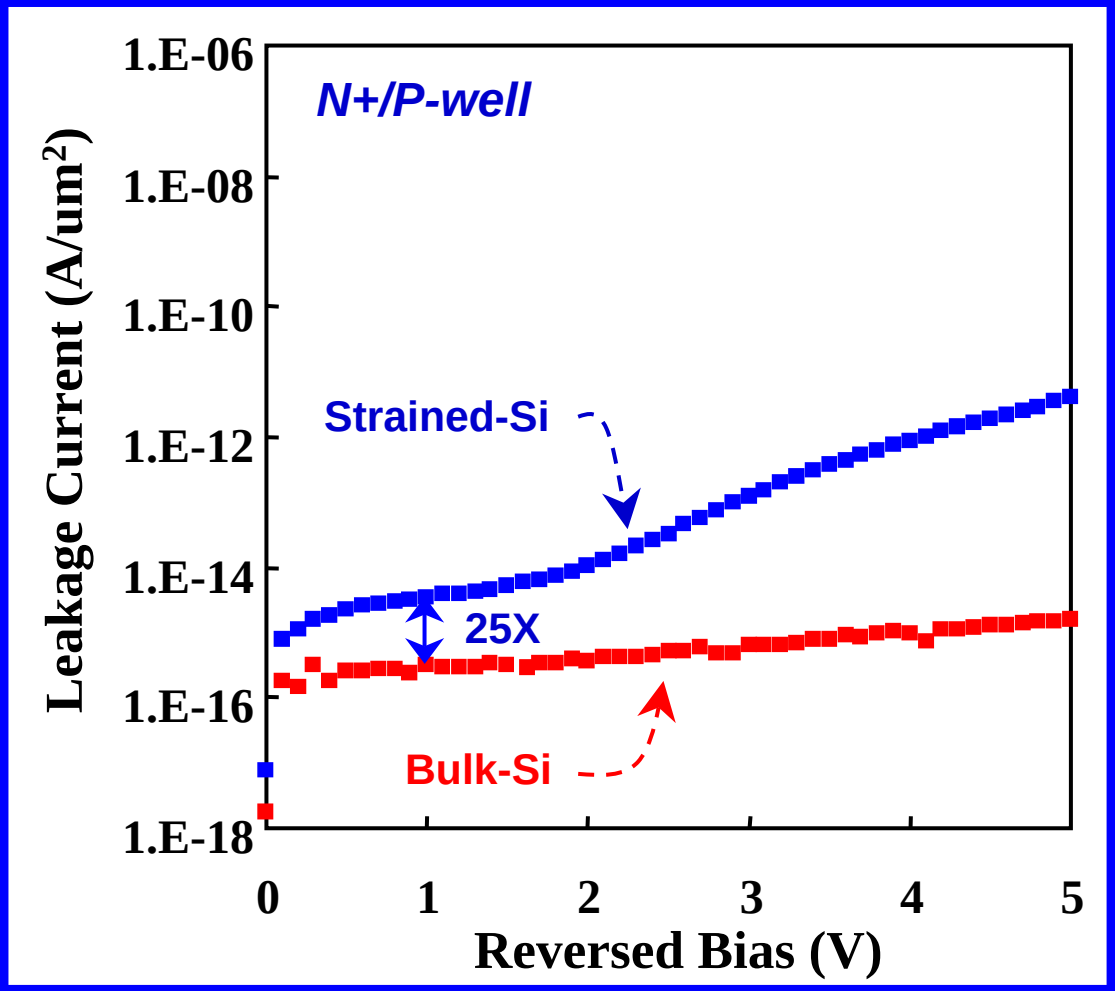
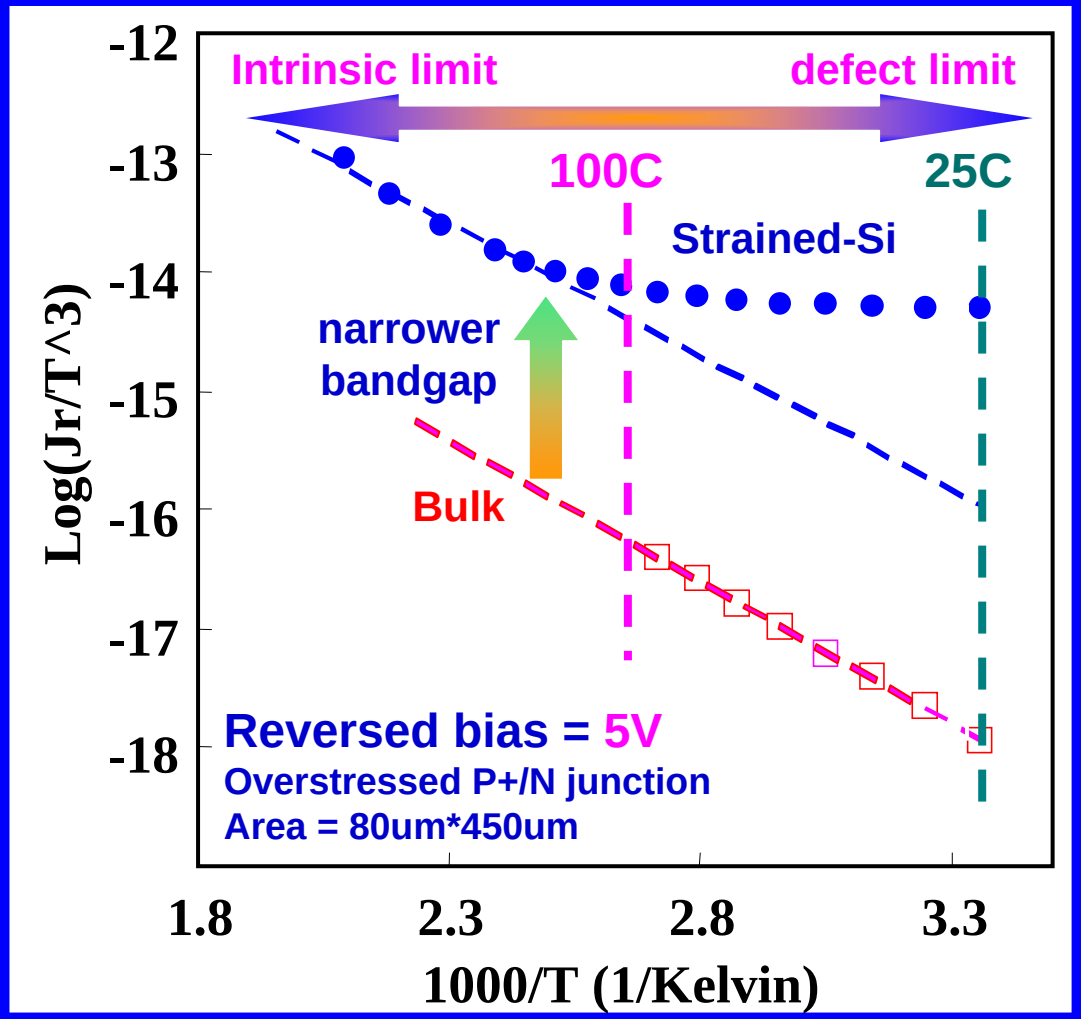
Junction Leakage Comparison



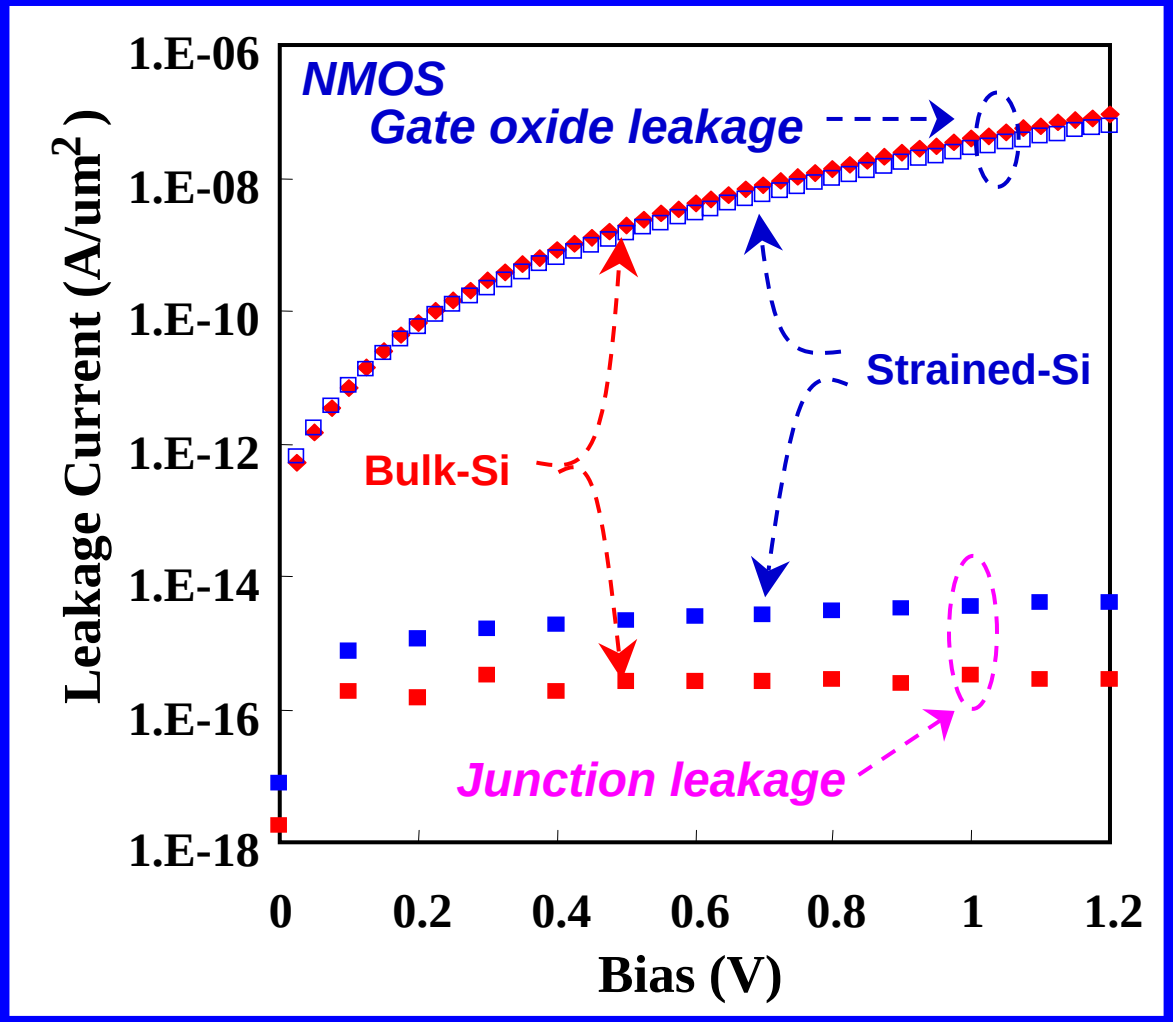
- *Strained-Si shows a 25 X junction leakage increase under normal circuit operation condition @1.2V.*
- *A large junction leakage was observed for reversed bias greater than 2.5V.*

Temperature Effect on Junction Leakage



- *Threading defect reduction is required to reach minimal junction leakage set by strained-Si narrower bandgap.*

Gate and Junction Leakage Comparison



- *Strained-Si demonstrated comparable gate leakage as bulk-Si.*
- *Junction leakage of strained-Si remains much smaller than gate oxide leakage under normal circuit operation condition.*

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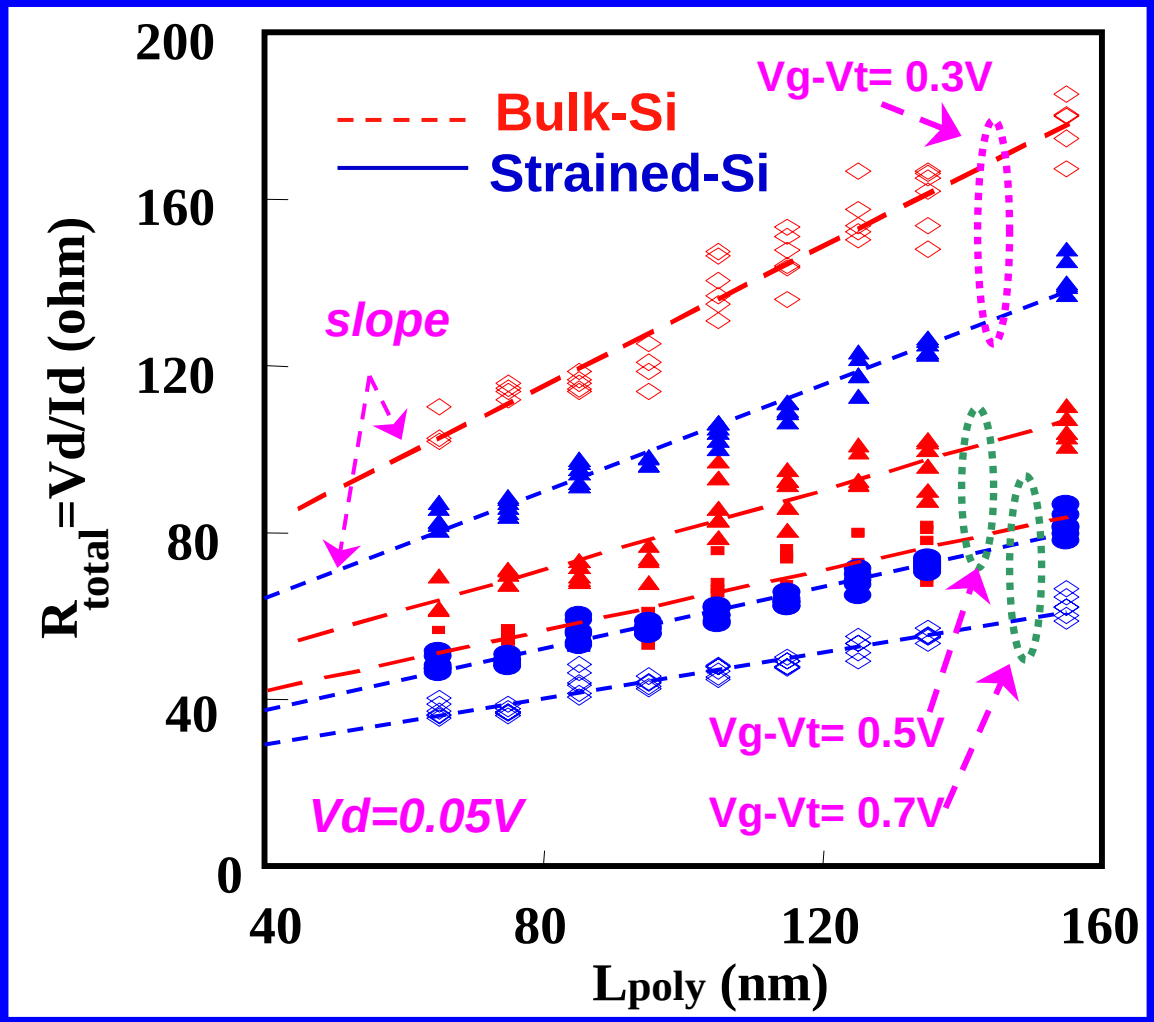
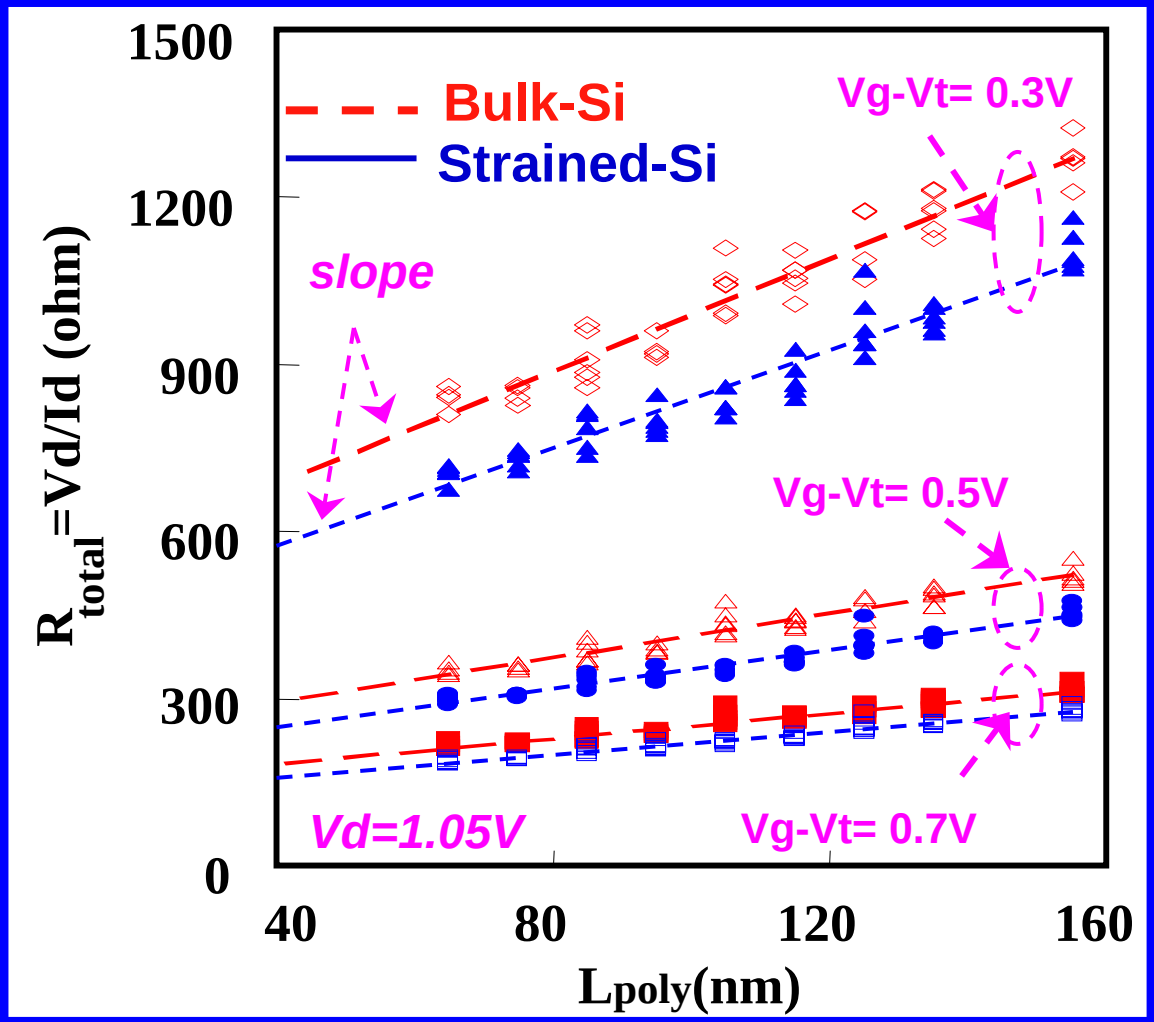
Unit Channel Resistance - Linear Region



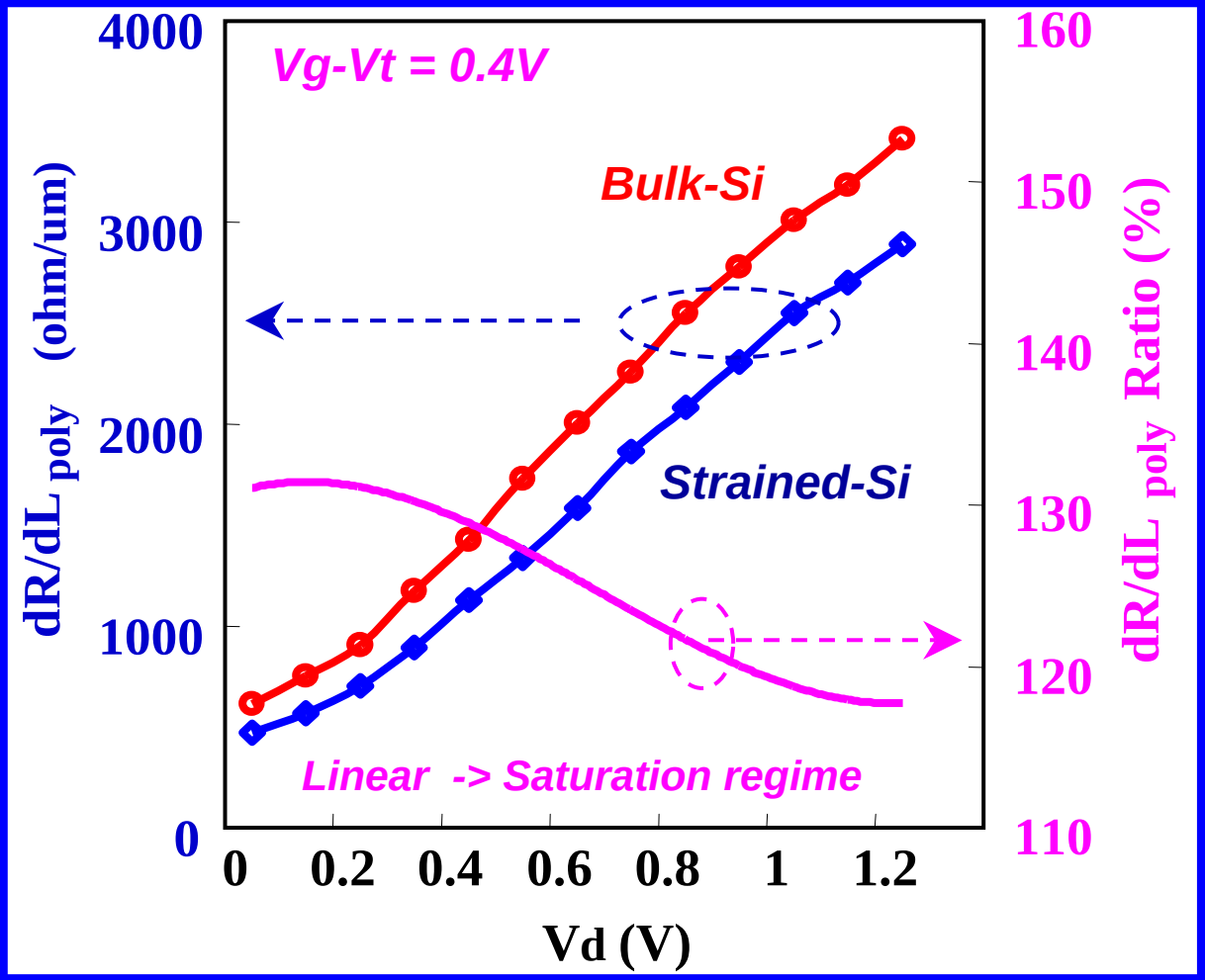
- *By shift-and-ratio method, resistance slope dR_{total}/dL_{poly} is extracted and defined as unit channel resistance without Leff and parasitic resistance uncertainties.*

Unit Channel Resistance - Saturation Region



- *Unit channel resistance can be extracted for various Vg and Vd.*
- *At saturation region, unit channel resistance increases due to pinch-off.*

Unit Channel Resistance
- Linear vs. Saturation



- *Strained-Si short channel devices show a 32% smaller unit channel resistance at linear region.*
- *The improvement decreases to 18% at saturation.*

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- Comparison of Id-sat and Id-lin enhancement
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- Gate oxide & junction leakage
- Unit channel resistance vs. lateral-field
- ❖ **Ring oscillator power delay**
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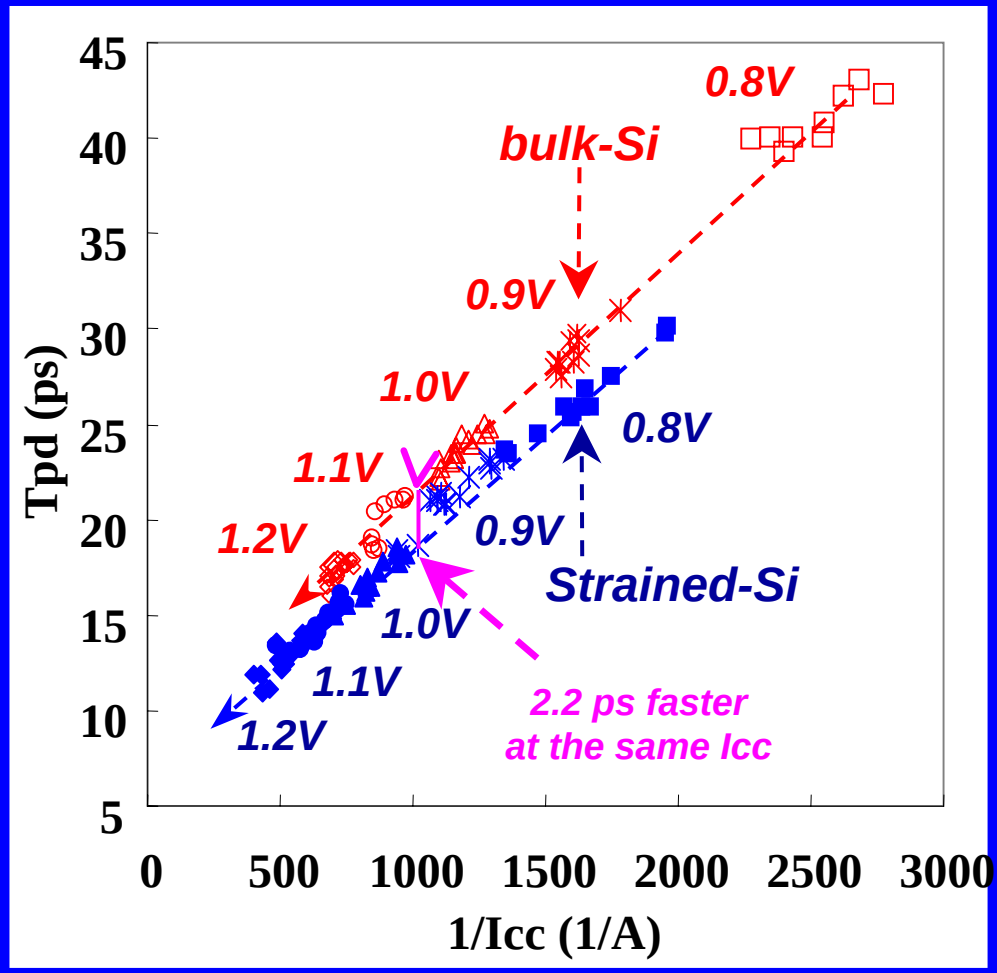
Strained-Si Ring-Oscillator
Gate Delay vs. Drive Current



151 stages
Wp/Wn=3.25um/2.5um
Gate Length ~70nm

- Gate delay of ring oscillator for the same Icc current is improved over 2.2 ps due to better Id-lin gain of strained-Si.

Summary

- ***Short channel strained-Si devices demonstrated including self-heating/temperature effect.***
- ***Strained-Si has a 25X larger Junction leakage due to defect which is still much smaller than gate oxide leakage.***
- ***Larger Id-lin gain than Id-sat gain gives strained-Si device better driving capability over bulk-Si devices for circuit operation.***
- ***Ring oscillator power-delay performance of strained-Si shows its great potential on high-performance low-power applications.***