CSE 577 Spring 2011

Device Physics, Modeling, and Fabrication

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  - Device Reliability (TDDB, HCE)

Device Characterization

Model Parameter

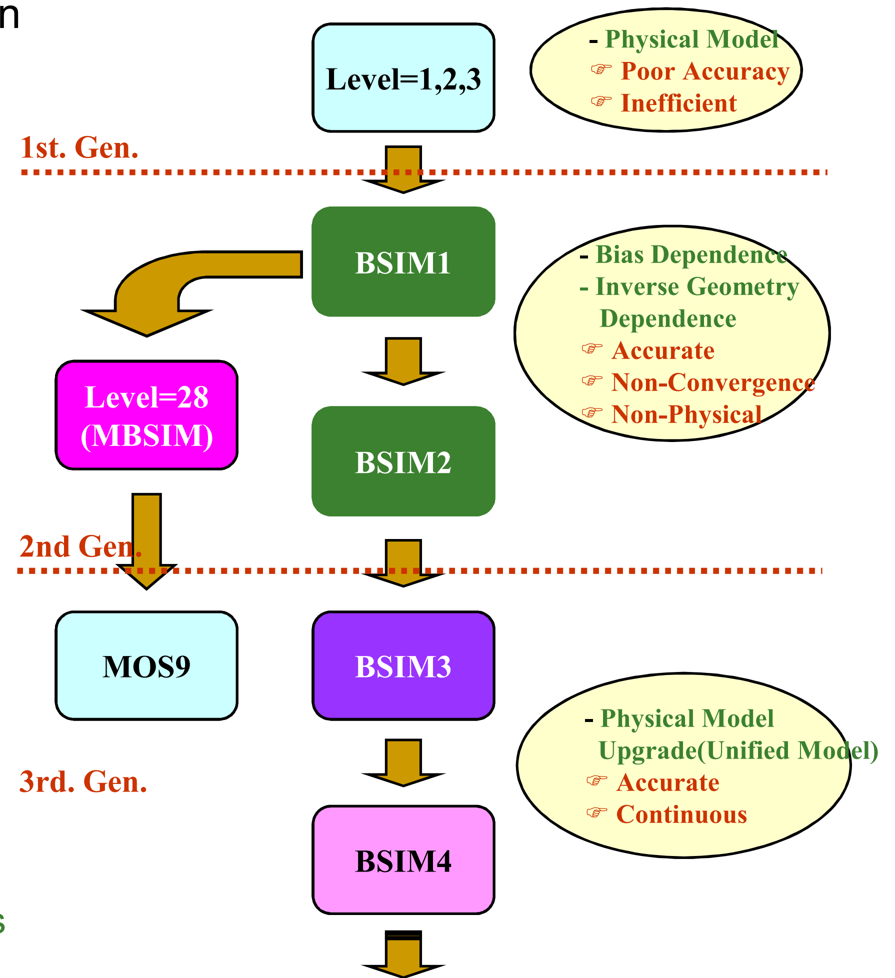
MOSFET I-V Relationship

I-V, Vth Simulation

Ring Oscillator Simulation

Model Parameter

- SPICE Model Parameter
  - Device Model for SPICE Circuits Simulation
  - Originally developed at Univ. of Berkeley
- Model Parameter History
  - 1st Generation Models(Level 1, 2, 3)
    - Simple and Physically Based Model
    - Inefficient for Circuit Simulations
  - 2nd Generation Models(BSIM1, BSIM2, Level 28(MBSIM))
    - Complex and Empirical M/P based Model
    - Mathematically Conditioned for Efficient Circuit Sim.
    - Polynomial Functions
  - 3rd Generation Models(BSIM3, MOS9, BSIM4)
    - Physically Based Model (Reduction of Number of M/P)
    - Well -behaved Smoothing Function(Continuous and Single Unified Eq.)



(cont'd) Model Parameter

- An example of Model Parameter

♣ Operation Bias Condition 및 Geometry Parameter

- VGG	: Maximun Gate Supply Voltage	:V
- VDD	: Maximun Drain Supply Voltage	:V
- VBB	: Maximun Substrate Supply Voltage	:V
- WMIN	: Minimum Width	:um
- LMIN	: Minimum Length	:um
- TMAX	: High Temerature	:℃
- TLOW	: Low Temperature	:℃
- HDIF	: Length from Center of Contact to Gate edge	:um
- LDIF	: Length of LDD adjacent to Gate	:um
- NPEAK	: Substrate doping rigth under Gate	:/cm^3
- NSUB	: Substrate doping	:/cm^3
- XJ	: Junction depth	:um

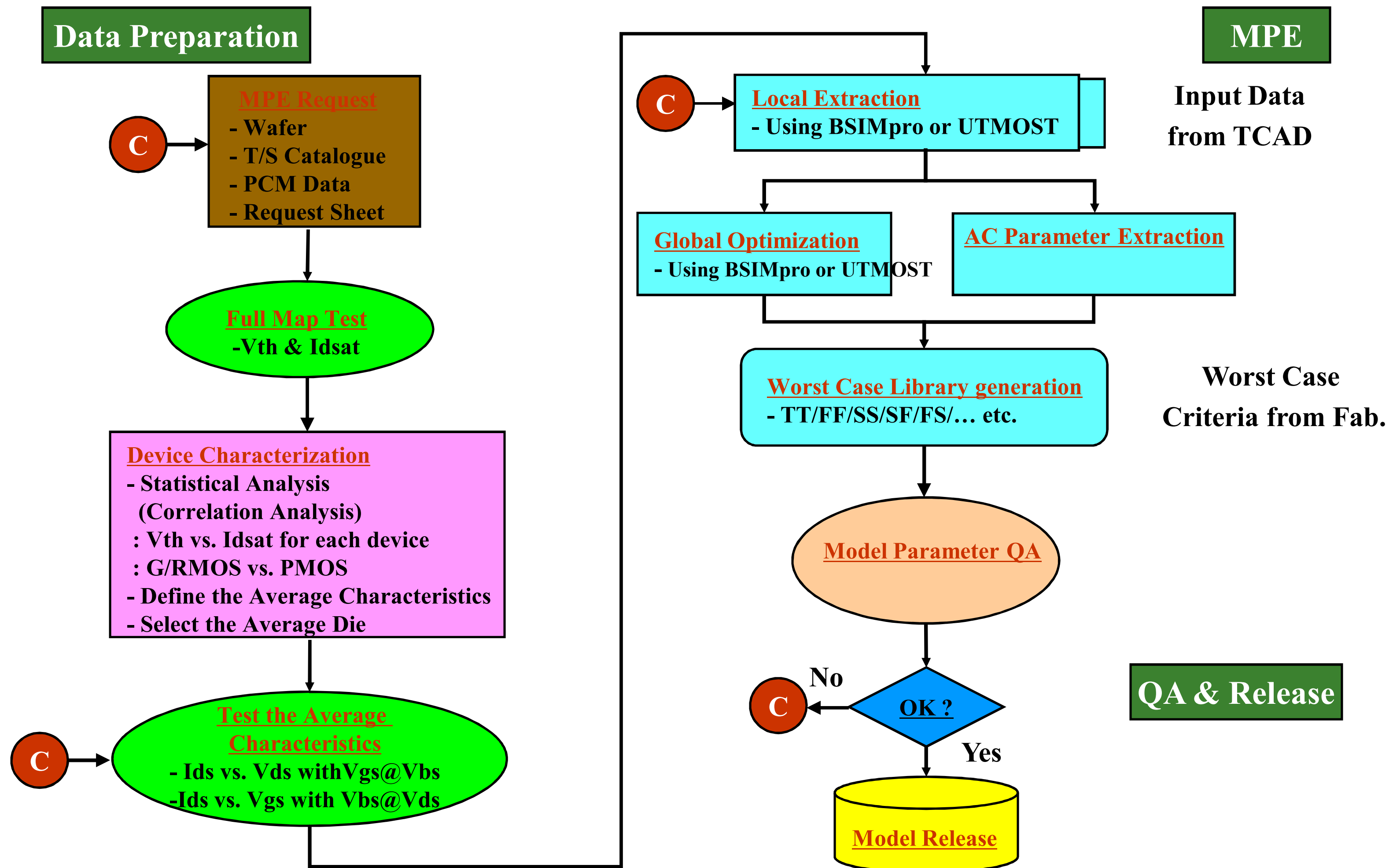
♣ Fab Tracking Parameter

- VTO	: Threshold Voltage	:V
- TOX	: Gate Oxide Thickness	:Å
- RSH	: S/D Sheet Resistence	:Ω/sqr
- WD	: Channel Width shortening	:um
- LD	:Channel Length shortening	:um
- XW	: Accounts for masking & etching effects	:um
- XL	: Accounts for masking & etching effects	:um

Leff=L+XL-2×LD
Weff=W+XW-2×WD

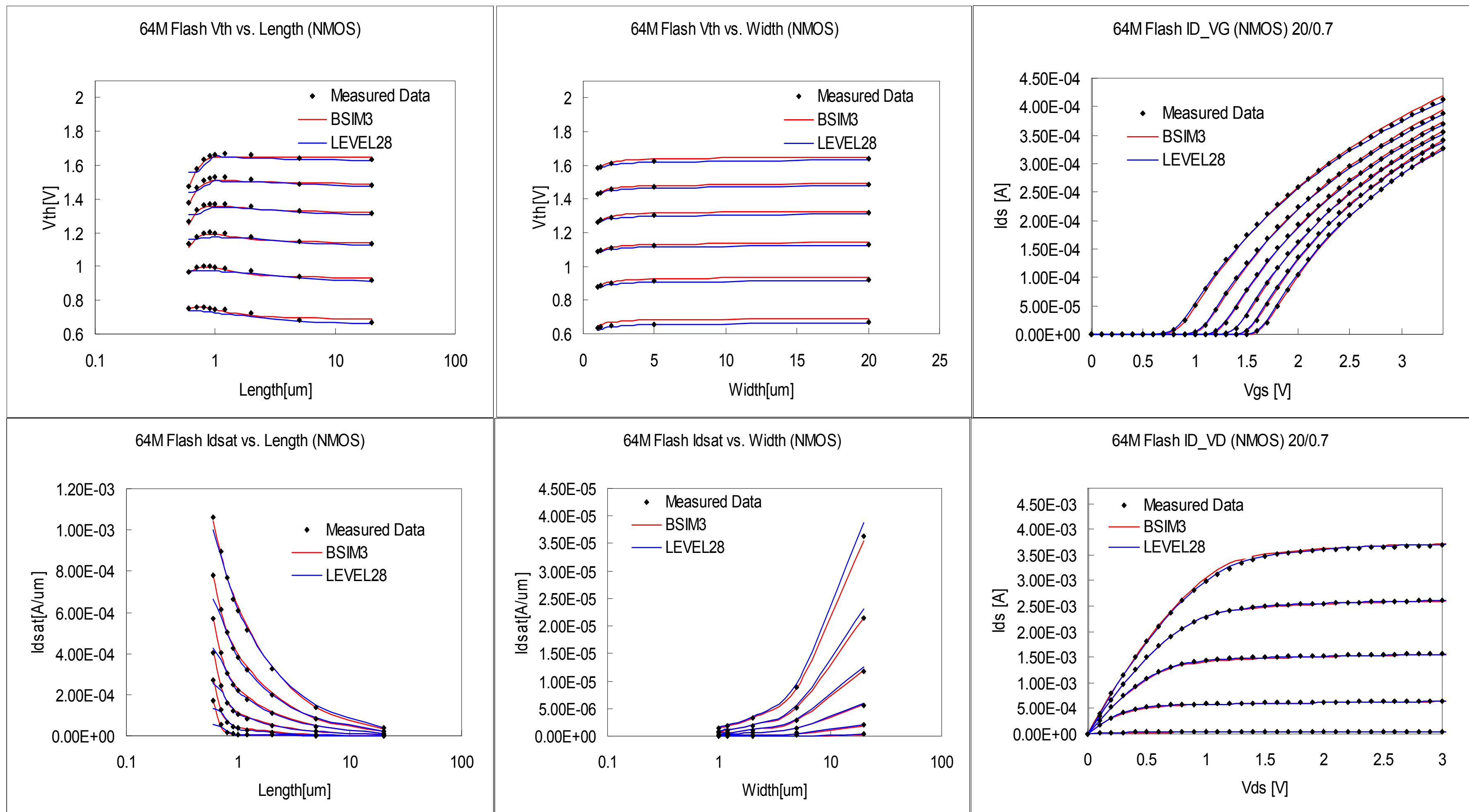
(cont'd) Model Parameter

- Model Parameter Extraction Process



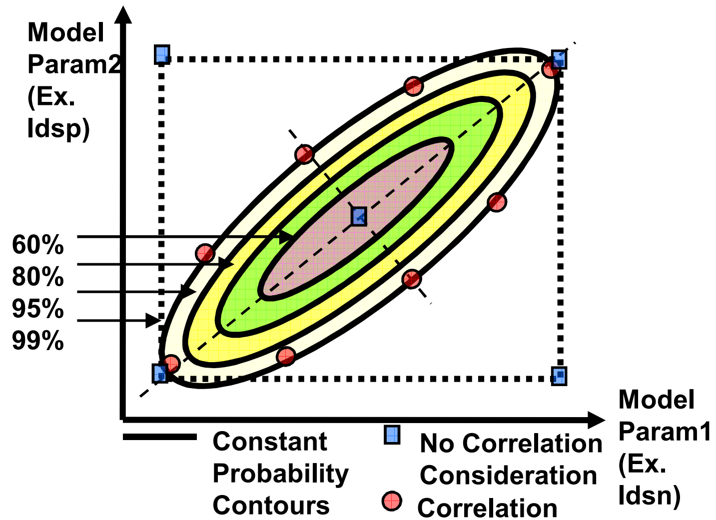
(cont'd) Model Parameter

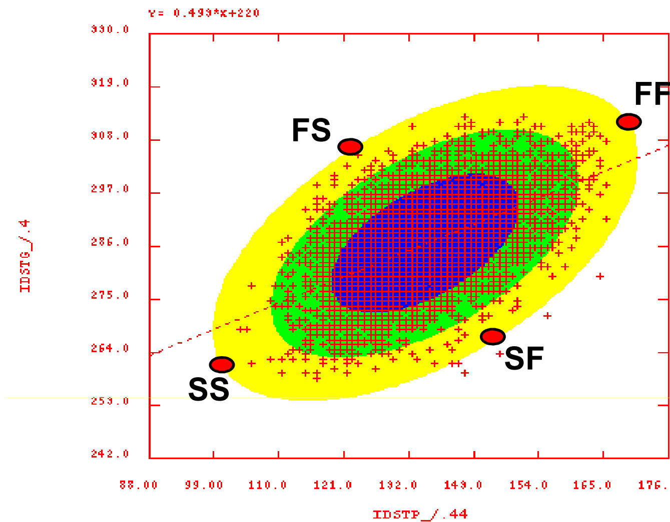
- MPE example



(cont'd) Model Parameter

- Worst-Case Simulation Methodology
  - Extreme Corner Method



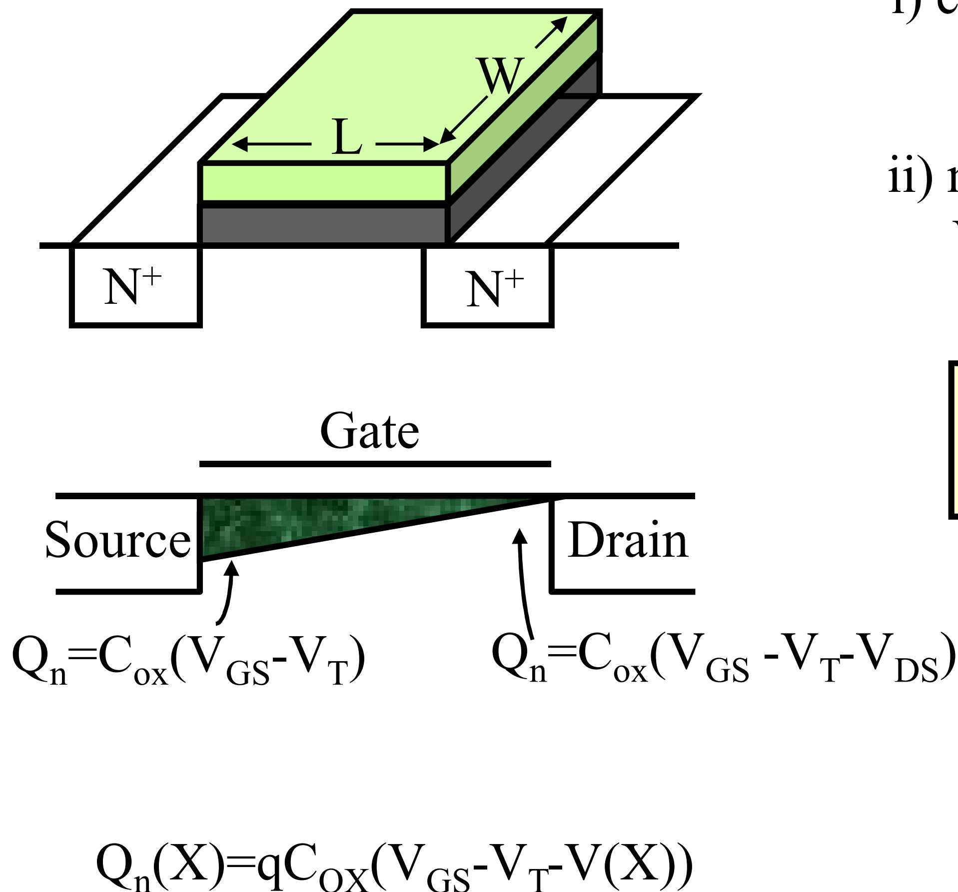


- Skew Parameters (Corner Model: +/- 3s model)
  - Tox, RSH, DelVto, XL, XW (process parameters)
  - TT,FF,SS,FS,SF

* How do the parameters contribute the Corner model?

* Why should we consider the skew parameter?

MOSFET I-V Relationship



i) cutoff region ; $V_{GS} < V_T$

$I_D = 0$

ii) nonsaturation(or triode) region ;

$V_{GS} \geq V_T$, $0 < V_{DS} \leq V_{GS} - V_T$

$$I_{DS} = W\mu_n Q_n(x) \frac{dV(x)}{dx}$$

- $Q_n(x)$: #of electrons per unit surface area
- μ_n : electron mobility
- $V(x)$: surface potential at x

(cont'd) MOSFET I-V Relationship

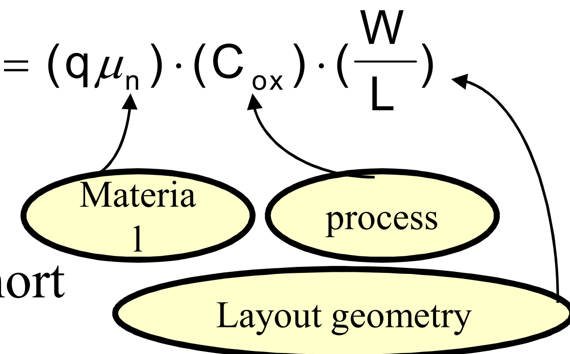
Integrating both sides of $I_{DS}=W\mu_n Q_n(x)\dfrac{dV(x)}{dx}$

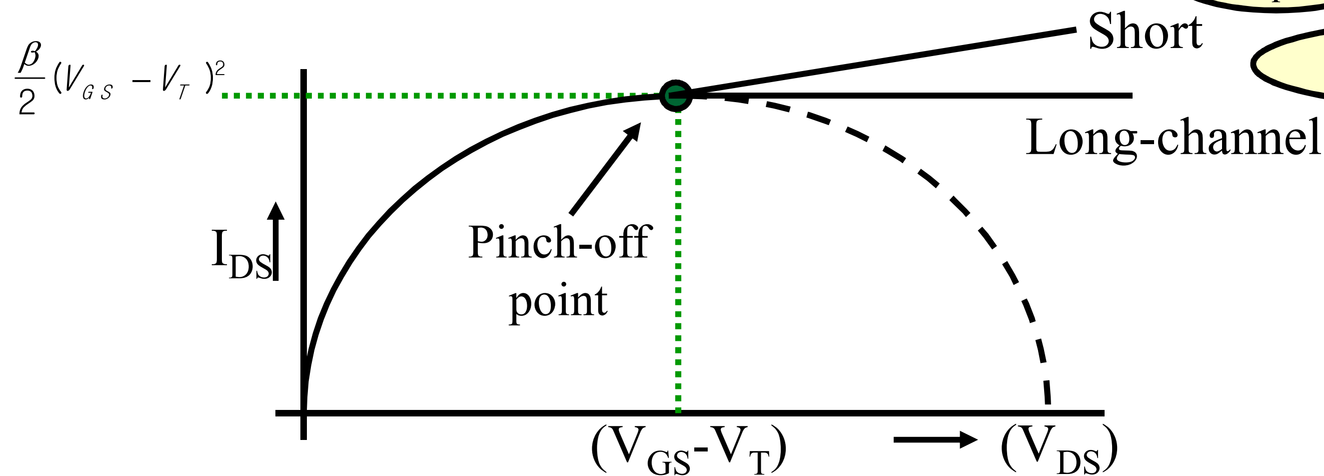
$$\int_0^L I_{DS}\cdot dx = \int_0^{V_{DS}} qW\mu_n C_{ox}[V_{GS}-V_T-V(x)]dV(x)$$

$$\Rightarrow I_{DS} = q\mu_n C_{ox}\frac{W}{L}[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}]$$

$$= \beta[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}], \quad \text{where} \quad \beta=(q\mu_n)\cdot(C_{ox})\cdot(\frac{W}{L})$$

$$= -\frac{\beta}{2}[V_{DS}-(V_{GS}-V_T)]^2+\frac{\beta}{2}(V_{GS}-V_T)^2$$



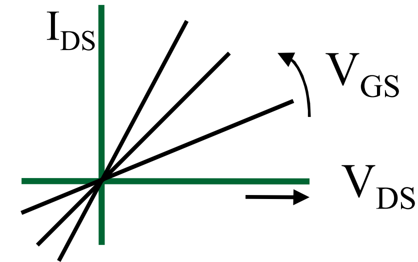


(cont'd) MOSFET I-V Relationship

ii) Linear Region, VDS ≤ δ(0.1V)

IDS=β(VGS-VT)VDS : analog multiplier

iii) Saturation Region

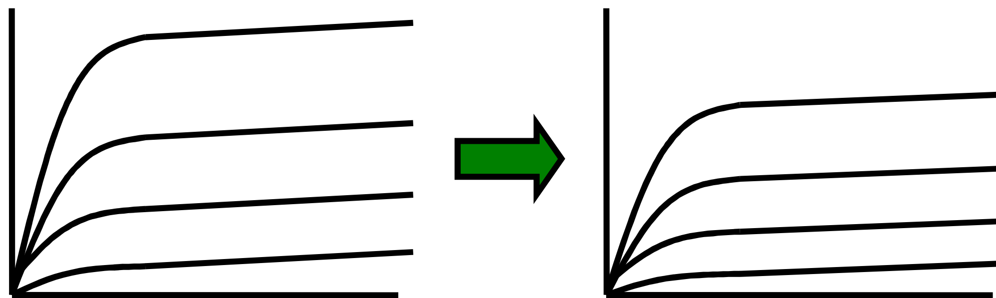


$$I_{DS} = \beta\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]\Bigg|_{V_{DS} = V_{GS} - V_T}$$

$$\Rightarrow I_{DS} = \frac{\beta}{2}(V_{GS} - V_T)^2,$$ For $V_{DS} \geq V_{GS} - V_T$: indep. of V_{DS}

- MOSEF is called Square-Law Device

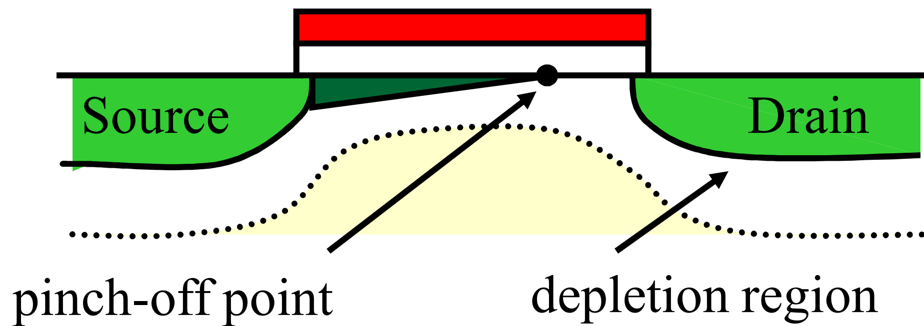
Remember β=qμnCoxW/L, where $\mu n \cong \frac{\mu_{n0}}{1+\theta(V_{GS} - V_T)}$ (surface scattering)



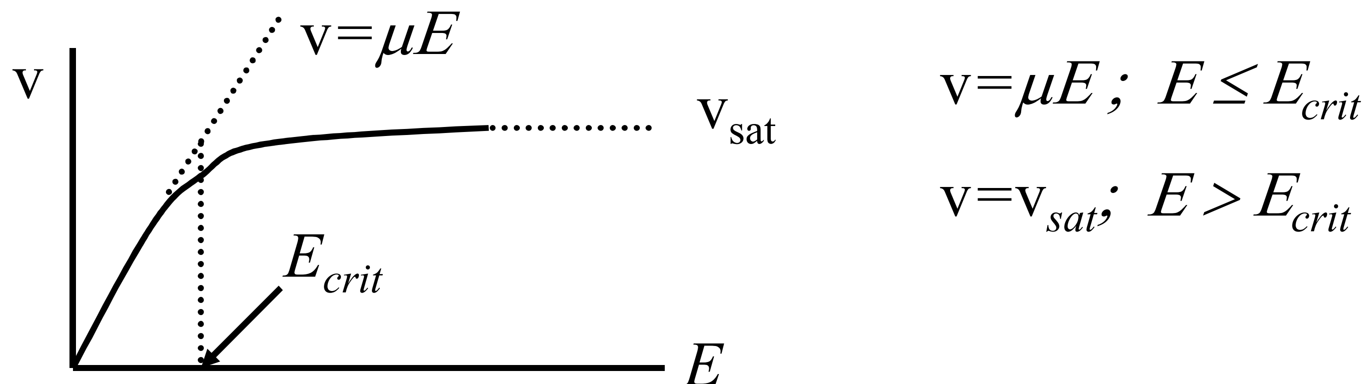
Actually less than square → Why?

Note: Two Causes for Current Saturation

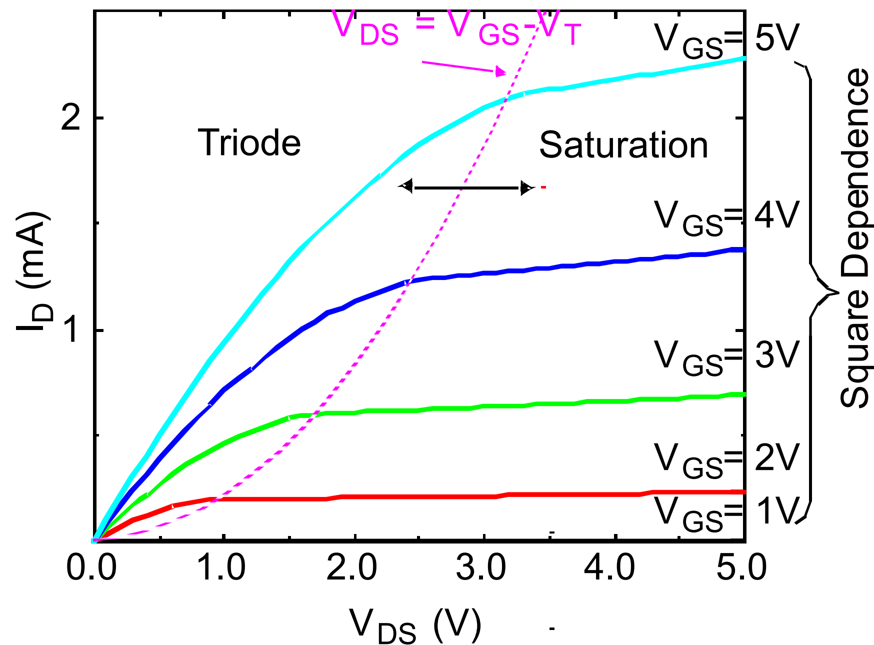
- Pinch-off in long-channel devices



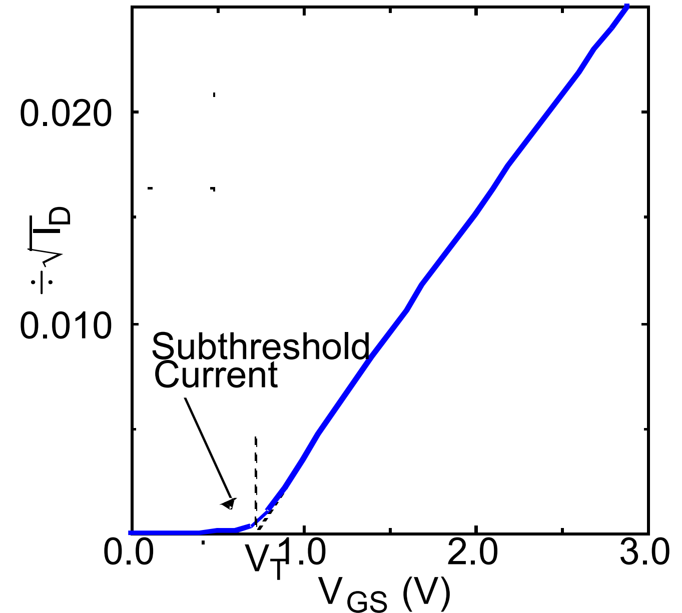
- Velocity saturation in short-channel devices



MOSFET I-V Characteristics



(a) I_D as a function of V_{DS}



(b) $\sqrt{I_D}$ as a function of V_{GS} (for V_{DS} = 5V)

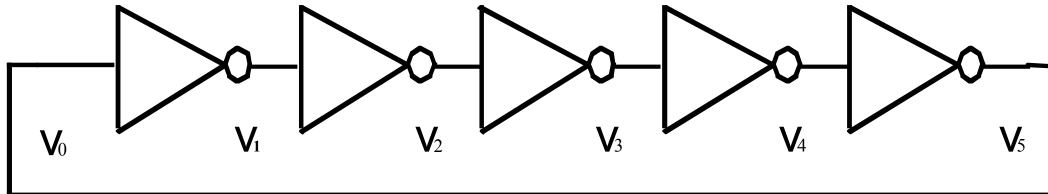
NMOS Enhancement Transistor: W = 100 μm, L = 20μm

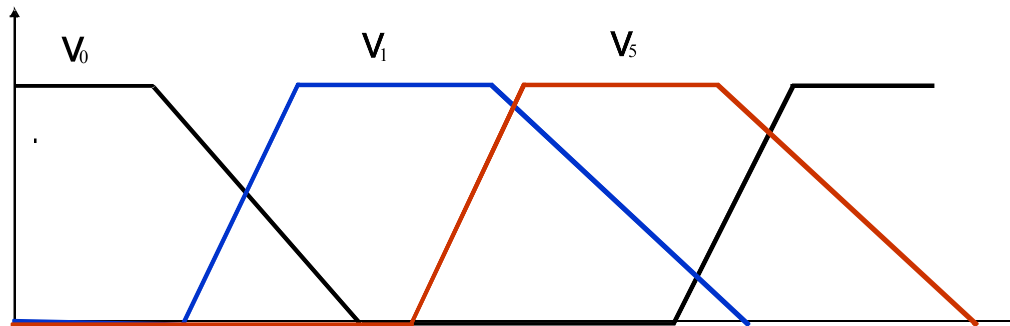
Lab. HSPICE Simulation

- I-V simulation
  - NMOS & PMOS

- Find Vth
  - Using HSPICE function
    - LV9
  - Write HSPICE input file to find Vth using Gm_max Method

Ring Oscillator Simulation





$$T = 2 \times t_p \times N$$

Where N is the number of inverters in the chain and factor 2 results from the full cycle

Circuit Designer should know the propagation delay of an inverter in terms of Fan-out ratio.

Device Physics for Circuit Designers

Channel Length Modulation

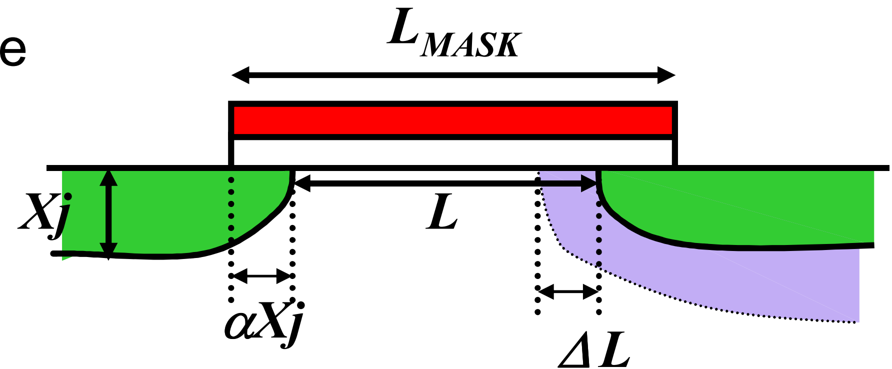
DIBL

Body Effect

Short Channel Effect & Short Channel Device

Channel Length Modulation

- I-V characteristics of short channel MOSFET is not satisfied with the square law due to CLM.



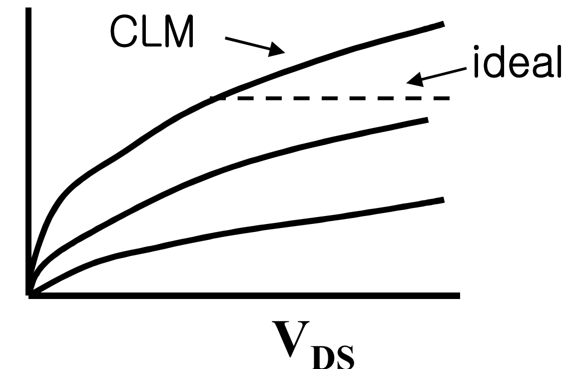
$$L = L_{MASK} - 2\cdot\alpha\cdot X_j$$

$$L_{eff} = L - \Delta L$$

$$\Delta L = \sqrt{\frac{2\varepsilon_s}{qN_A}\left[V_{DS} - \left(V_{GS} - V_T\right)\right]}$$

$$I \propto \frac{1}{L - \Delta L} = L^{-1}\cdot\left(1 - \frac{\Delta L}{L}\right)^{-1} \cong \frac{1}{L}\left(1 - \frac{\sqrt{V_{DS}}}{L}\right)^{-1} \cong \frac{1}{L}\left(1 + \lambda V_{DS}\right)$$

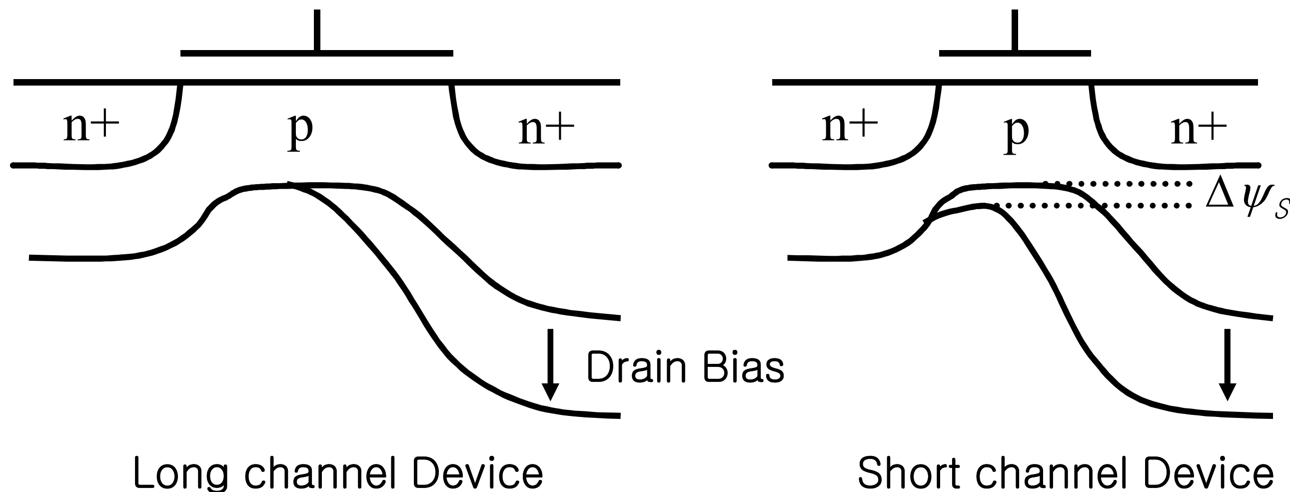
$$\Rightarrow I_{DS} = I_{DS,0}\left(1 + \lambda V_{DS}\right)$$



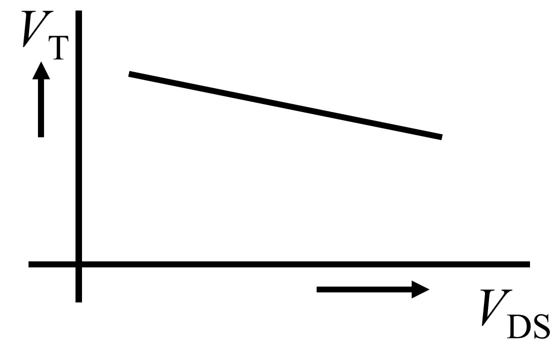
* Why is CLM is so important for analog circuit design?

Drain-Induced Barrier Lowering (DIBL)

- Usually for small L device, high drain bias can lead to early Punch-through



ex. DRAM cell leakage
current depends on the voltage
on the data line



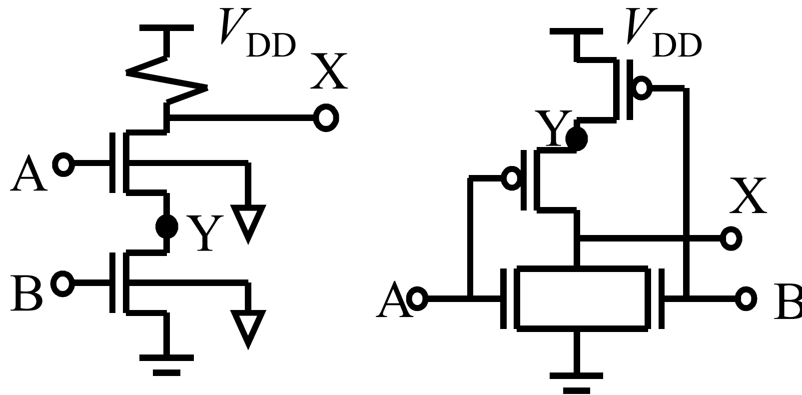
Body Effect

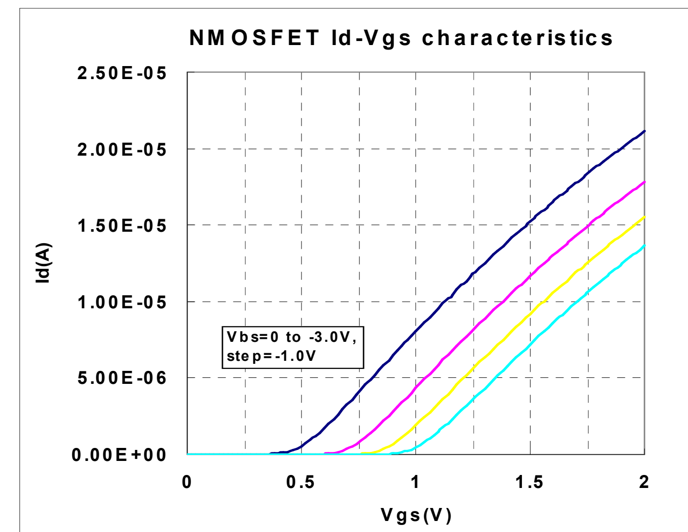
- Threshold Voltage depends on bulk bias

$$V_T = V_{T0} + \gamma(\sqrt{2\phi_F + V_{BS}} - \sqrt{2\phi_F})$$

Ex) Series-connected MOSFET's

- NMOSFET in 2-input NAND-gate
- PMOSFET in 2-input NOR-gate



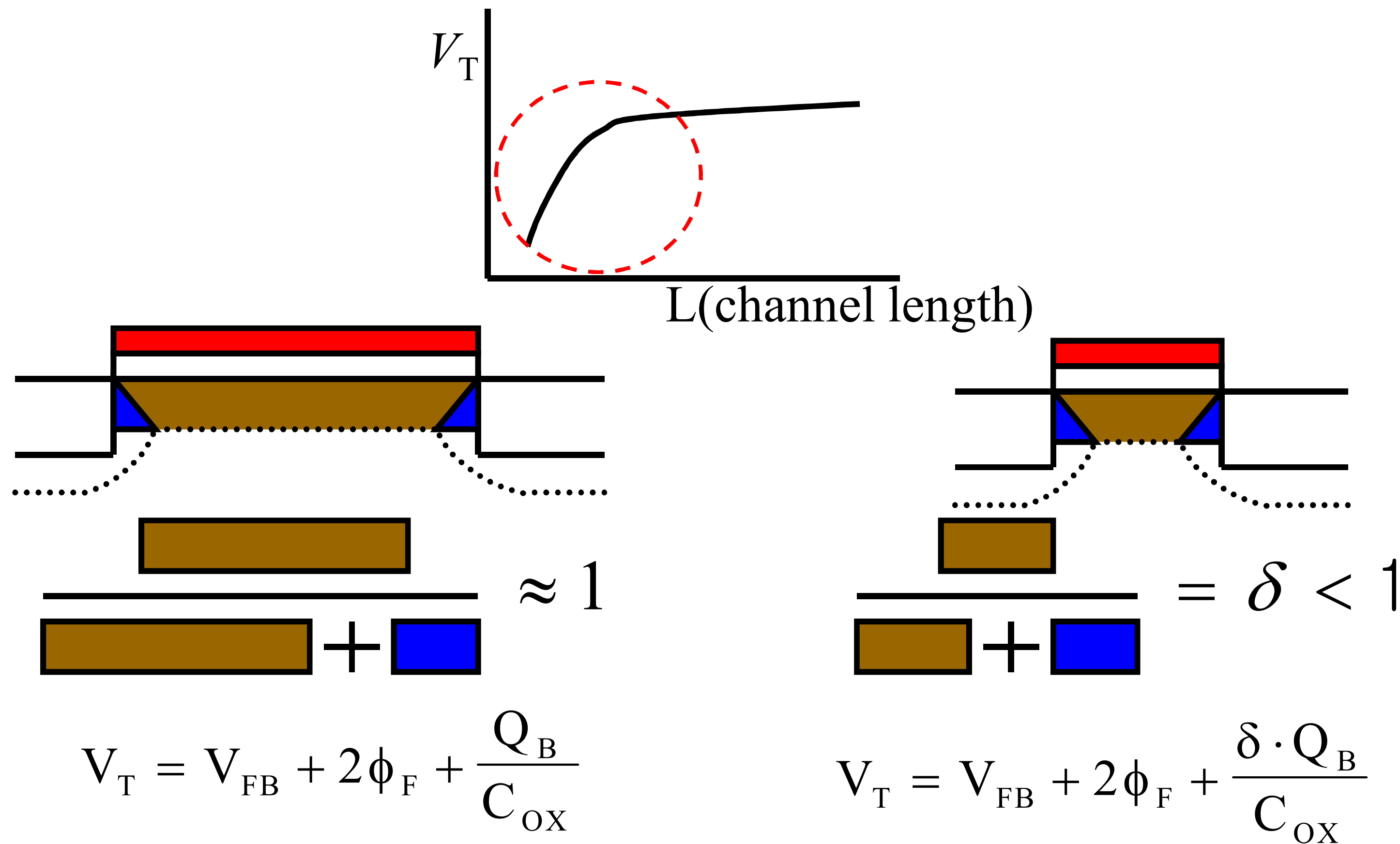


➡ V_T of A-NMOS & V_T of A-PMOS depend on V_Y

* How to eliminate body effect by layout technique?

Short Channel Effect

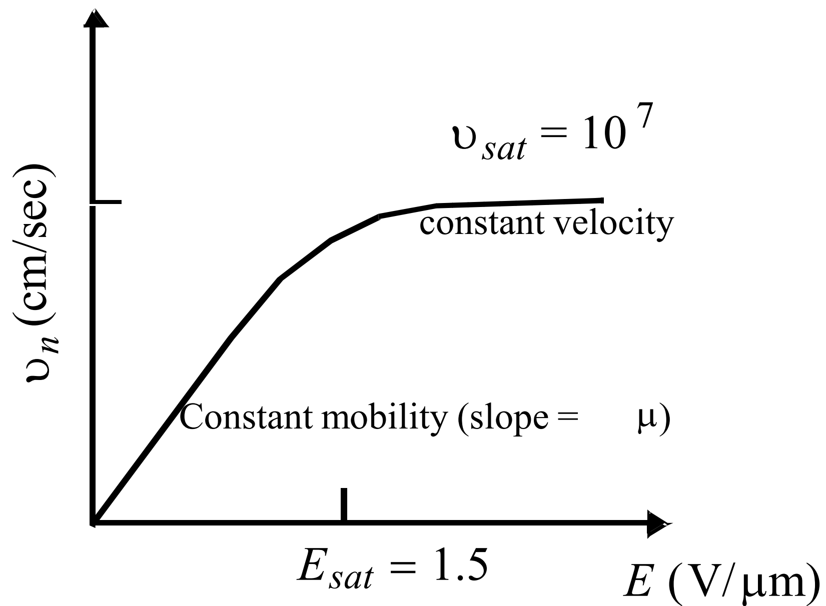
- Vth drops in short channel device



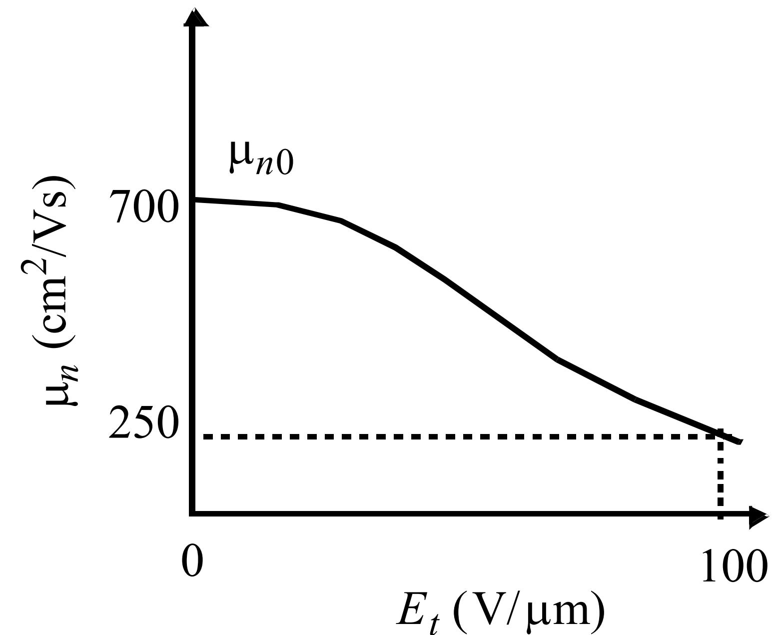
Q_B : (effective) charge per unit surface area

Short Channel Device

- Velocity Saturation



(a) Velocity saturation

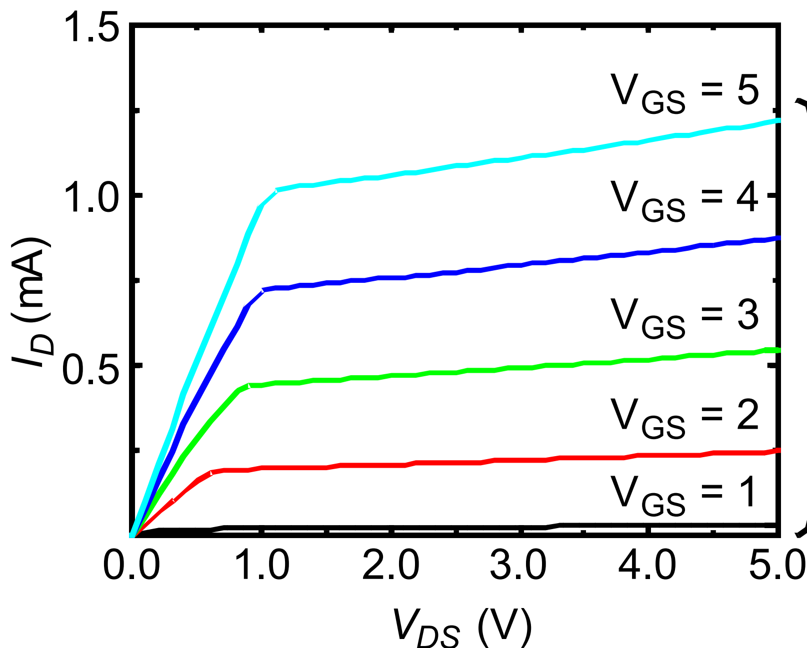


(b) Mobility degradation

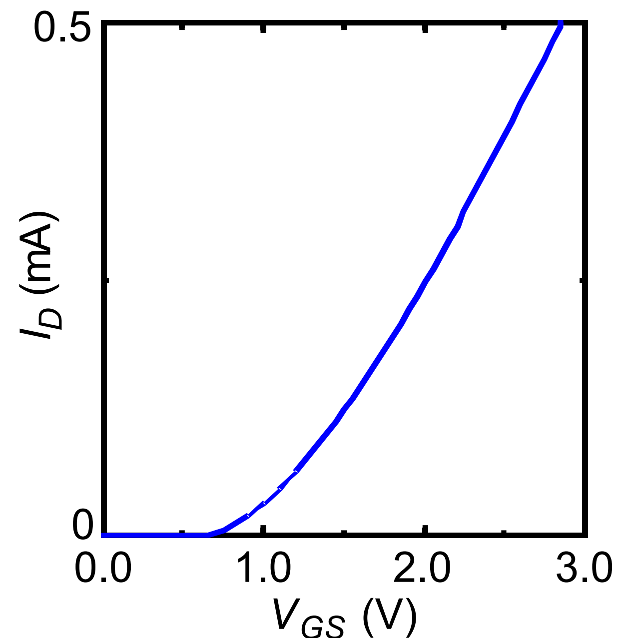
Attributed to the vertical component of E-field

(cont'd) Short Channel Device

- Short Channel Device Characteristics



(a) I_D as a function of V_{DS}



(b) I_D as a function of V_{GS} (for V_{DS} = 5 V).

Linear Dependence on V_{GS}

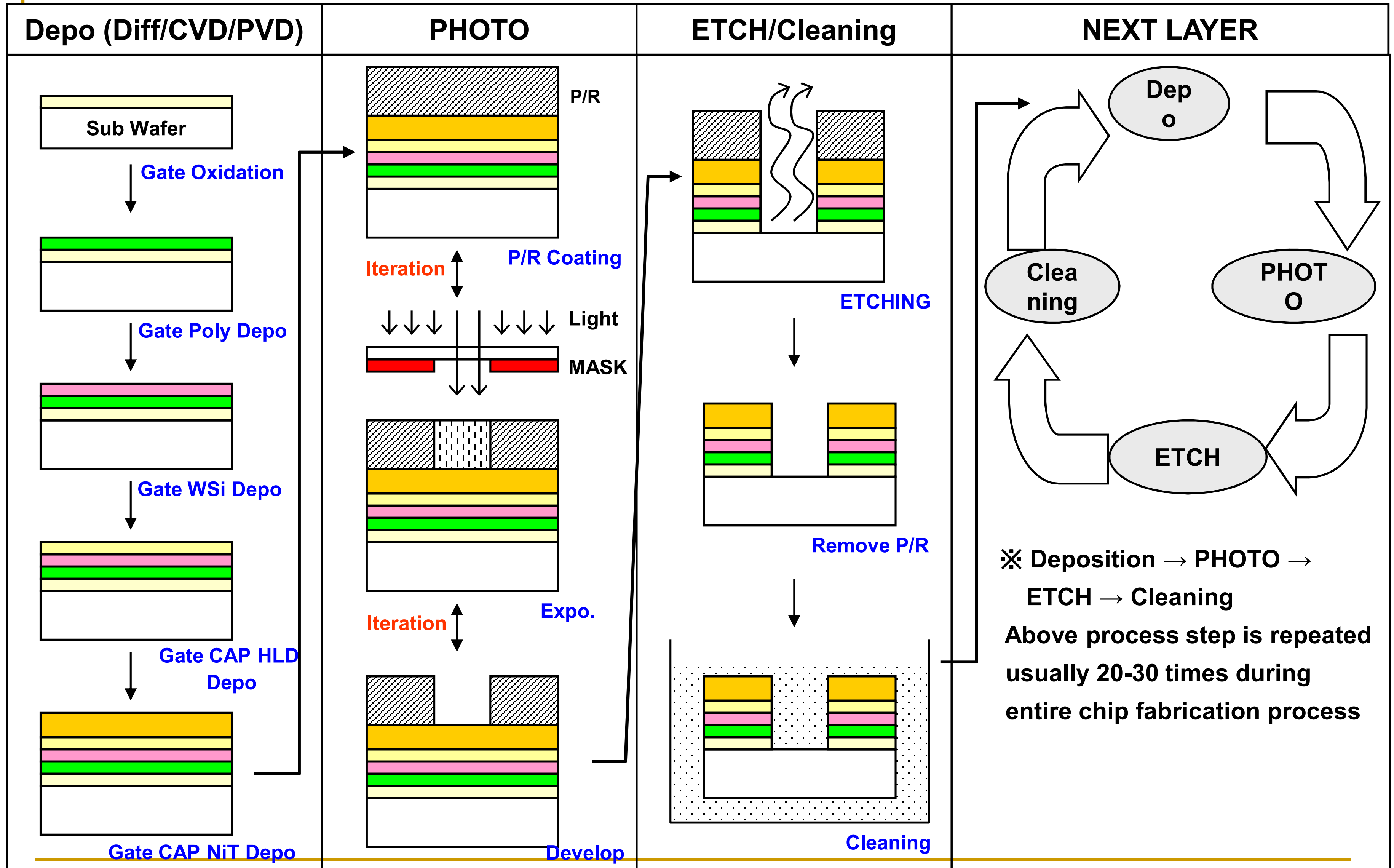
Device Fabrication

MOSFET Fabrication Process

Process Dependant Parameters

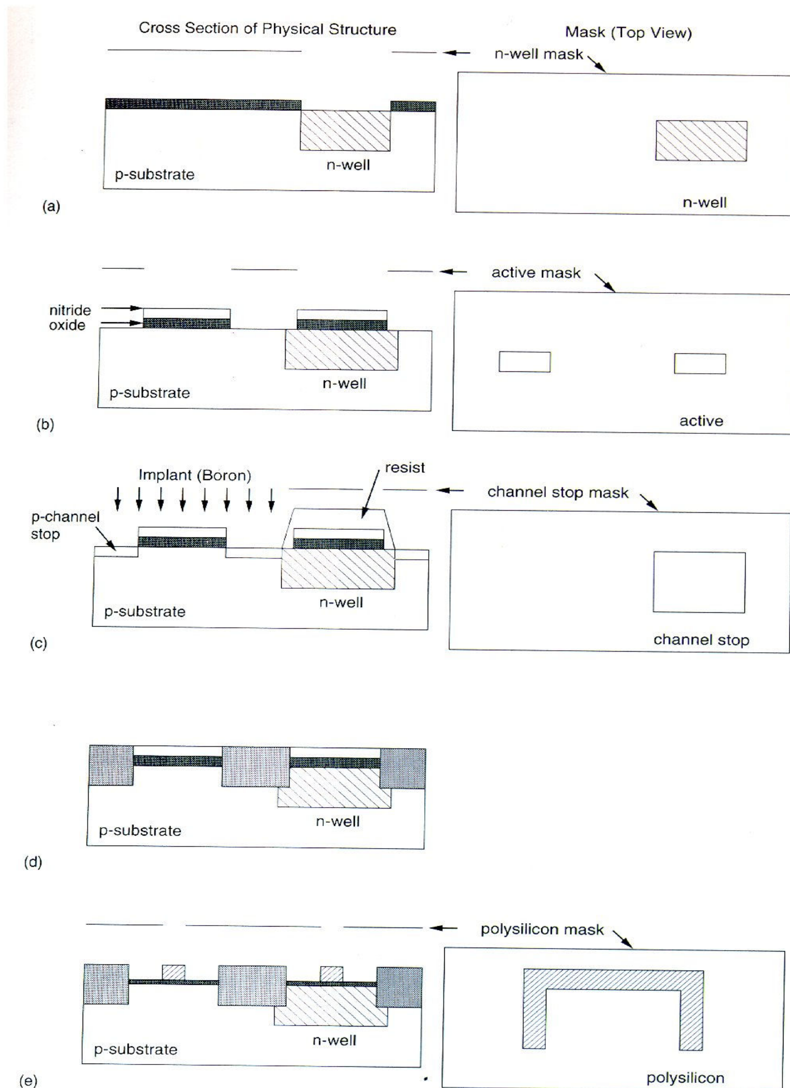
Design Rule

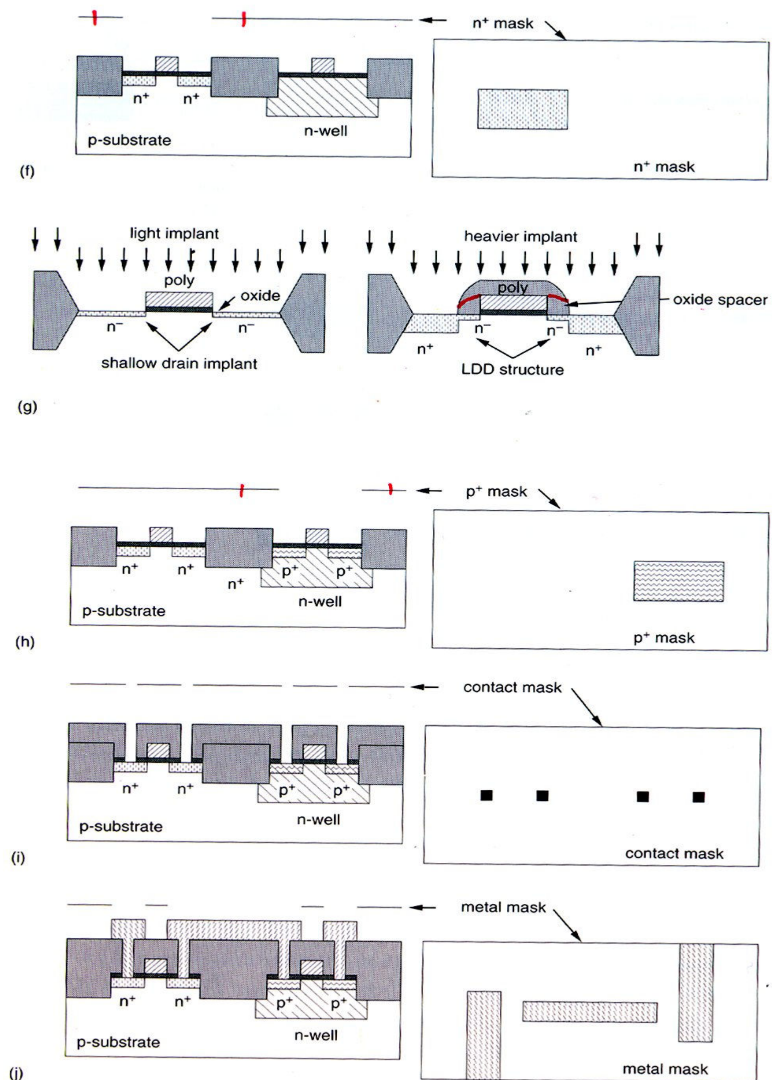
MOSFET Fabrication Process



(cont'd) MOSFET Fabrication Process

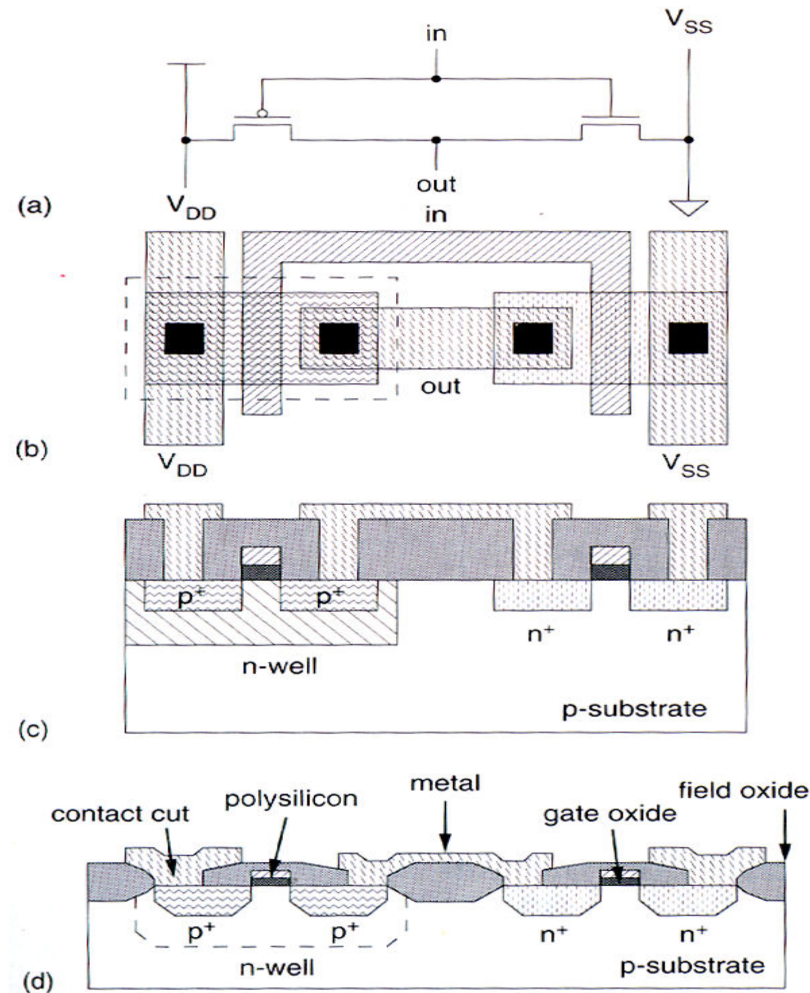
- Basic Nwell CMOS Process





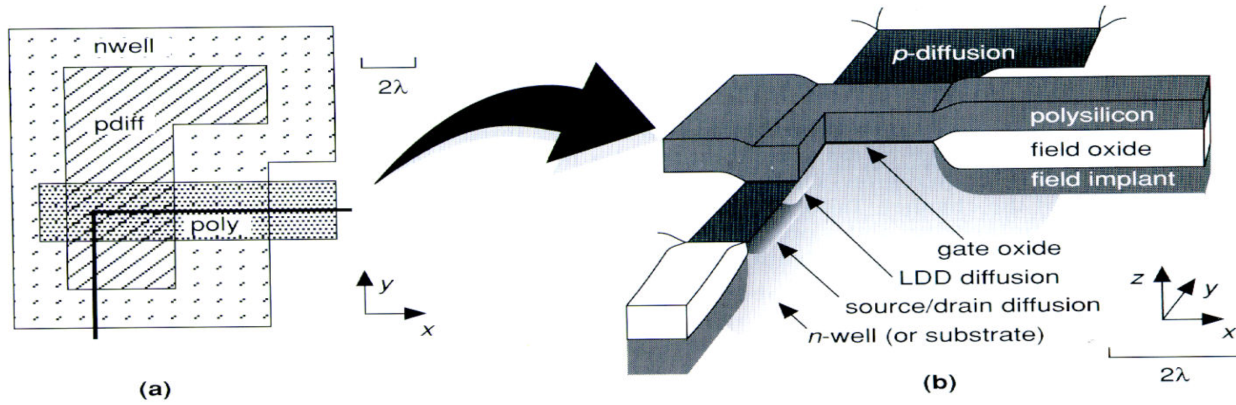
(cont'd) MOSFET Fabrication Process

- Cross-section of CMOS Inverter in N-well CMOS Process

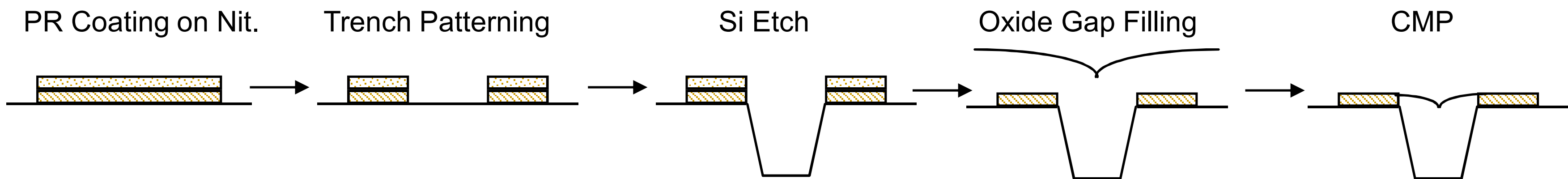


(cont'd) MOSFET Fabrication Process

- Isolation techniques



LOCOS Process

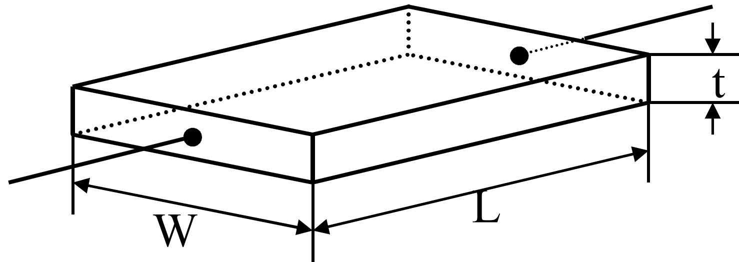


STI Process

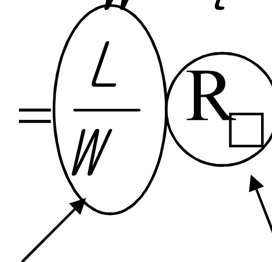
* What are the advantages and disadvantages of STI?

Process Dependant Parameters

- Sheet Resistance



$$R = \rho \frac{L}{W \cdot t} = \frac{L}{W} \cdot \frac{\rho}{t}$$



layout geometry process

TABLE 2.3 Sheet resistance (1 μm CMOS).

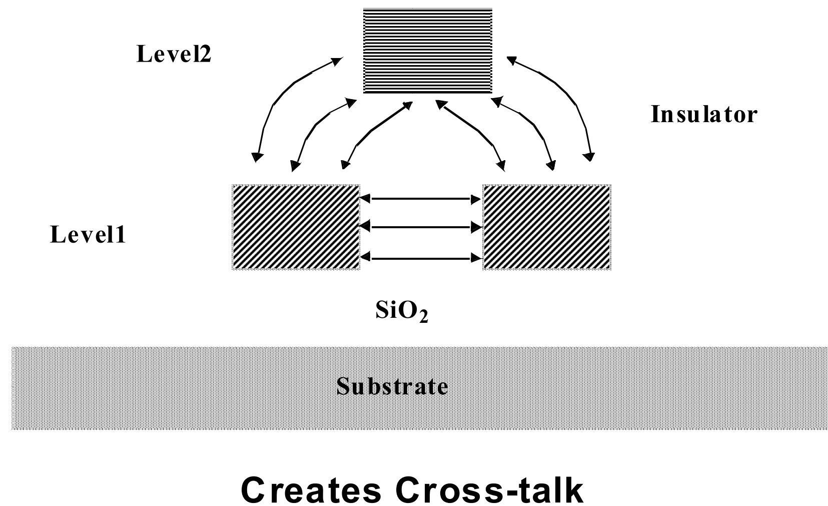
Layer	Sheet resistance	Units
n-well	1.15 ± 0.25	kΩ/square
poly	3.5 ± 2.0	Ω/square
n-diffusion	75 ± 20	Ω/square
p-diffusion	140 ± 40	Ω/square
m1/2	70 ± 6	mΩ/square
m3	30 ± 3	mΩ/square

TABLE 2.4 Sheet resistance (0.35 μm CMOS).

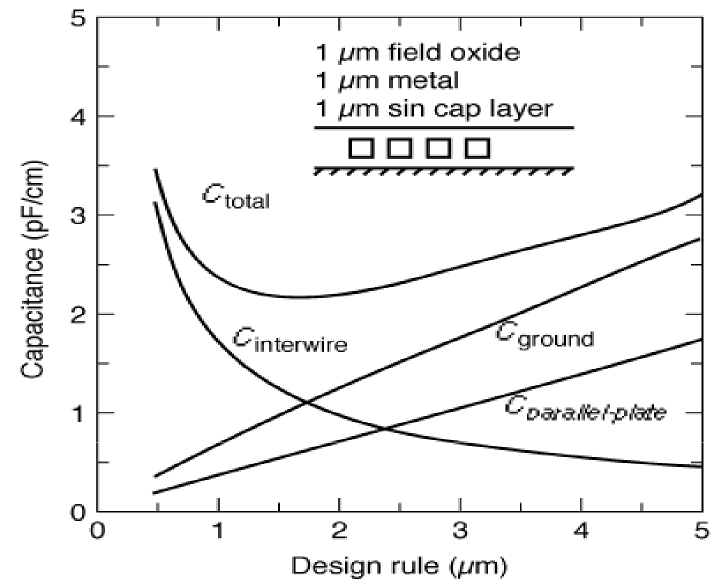
Layer	Sheet resistance	Units
n-well	1 ± 0.4	kΩ/square
poly	10 ± 4.0	Ω/square
n-diffusion	3.5 ± 2.0	Ω/square
p-diffusion	2.5 ± 1.5	Ω/square
m1/2/3	60 ± 6	mΩ/square
metal4	30 ± 3	mΩ/square

(cont'd) Process Dependant Parameters

- Interconnection wire Capacitance



Creates Cross-talk



	Area Capacitance (fF/μm^2)	Fringing Capacitance (fF/μm)
Metal1 to Polysilicon	0.055	0.049
Metal2 to Polysilicon	0.022	0.040
Metal2 to Metal1	0.035	0.046

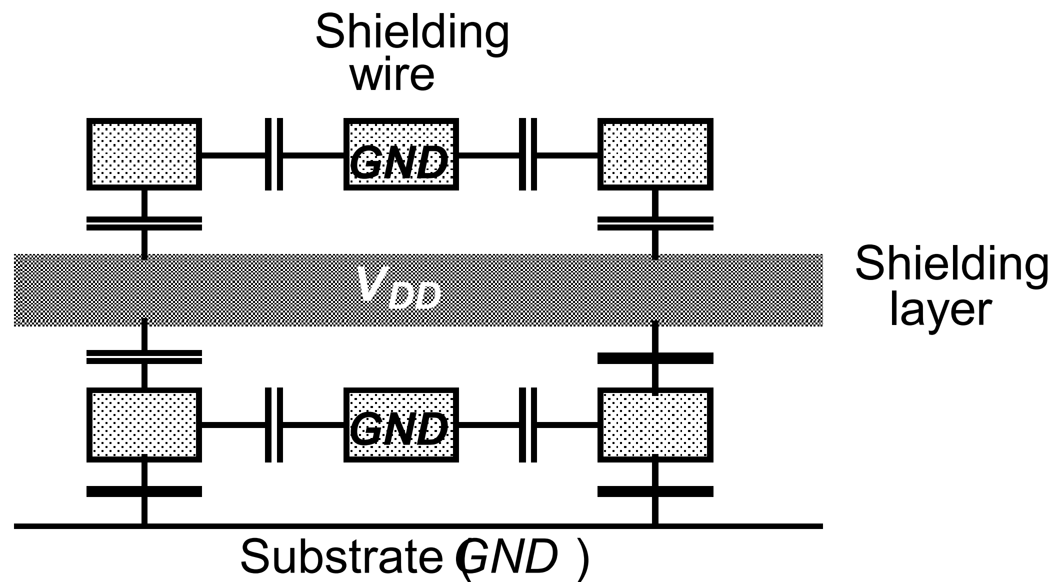
Inter-Wire Capacitance for 1 μm CMOS Process.

* The portion of interconnection capacitance in the total CMOS capacitance is dramatically increasing as design rule shrinks.

* How to reduce undesired crosstalk?

Note: How to battle capacitive crosstalk

- Avoid parallel wires
- Shielding



Insoo Kim

Design Rule

- λ-based design rule : all dimensions rep. as integer times λ, scalable.
  - ex. Mead-Conway rule, MOSIS rev. 4-6
- μm-based design rule : some dimensions are not scalable.
  - ex. Most company(foundry), MOSIS rev.7
- mixed($\lambda+\mu$) design rule
- 3 types of design rules
  - FEOL(Front End of the Line)
  - BEOL(Back End of the Line) ; metal interconnect
  - Glass layer

CMOS Process Layers

TABLE 2.2 CMOS process layers.

Mask/layer name	Derivation from drawn layers	Alternative names for mask/layer	MOSIS mask label
n-well	= nwell[1]	bulk, substrate, tub, *n*-tub, moat	CWN
p-well	= pwell[1]	bulk, substrate, tub, *p*-tub, moat	CWP
active	= pdiff + ndiff	thin-oxide, thinox, island, gate-oxide	CAA
polysilicon	= poly	poly, gate	CPG
n-diffusion implant[2]	= grow(ndiff)	ndiff, *n*-select, nplus, n+	CSN
p-diffusion implant[2]	= grow(pdiff)	pdiff, *p*-select, pplus, p+	CSP
contact	= contact	contact cut, poly contact, diffusion contact	CCP and CCA[3]
metal1	= m1	first-level metal	CMF
metal2	= m2	second-level metal	CMS
via2	= via2	metal2/metal3 via, m2/m3 via	CVS
metal3	= m3	third-level metal	CMT
glass	= glass	passivation, overglass, pad	COG

Via 1

[1] If only one well layer is drawn, the other mask may be derived from the drawn layer. For example, *p*-well(mask) = not(nwell(drawn)). A single-well process requires only one well mask.
[2] The implant masks may be derived or drawn.
[3] Largely for historical reasons the contacts to poly and contacts to active have different layer names. In the past this allowed a different sizing or process bias to be applied to each contact type when the mask was made.

Design Rule

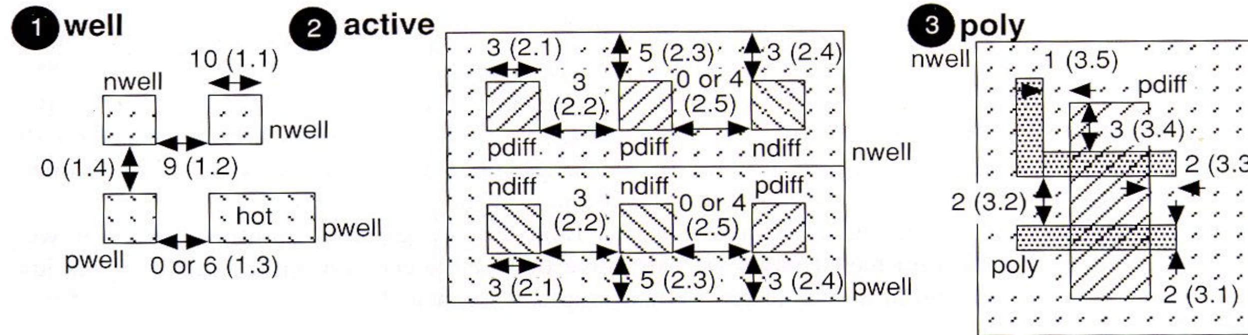
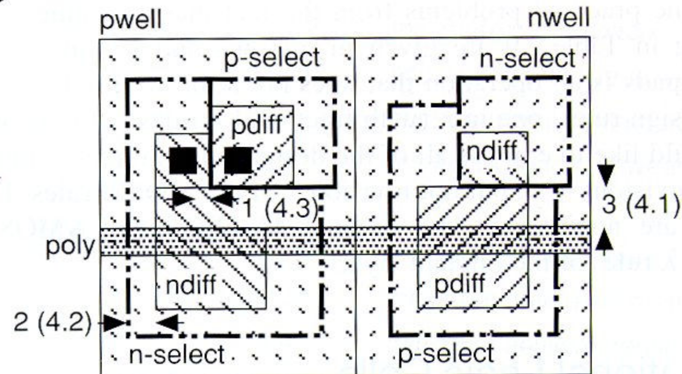
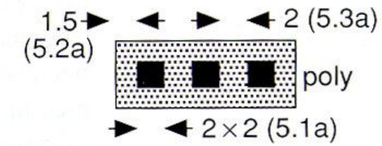


TABLE 2.7 MOSIS scalable CMOS rules version 7—the process front end.

Layer	Rule	Explanation	Value / λ
well (CWN, CWP)	1.1	minimum width	10
	1.2	minimum space (different potential, a hot well)	9
	1.3	minimum space (same potential)	0 or 6
	1.4	minimum space (different well type)	0
active (CAA)	2.1/2.2	minimum width/space	3
	2.3	source/drain active to well edge space	5
	2.4	substrate/well contact active to well edge space	3
	2.5	minimum space between active (different implant type)	0 or 4
poly (CPG)	3.1/3.2	minimum width/space	2
	3.3	minimum gate extension of active	2
	3.4	minimum active extension of poly	3
	3.5	minimum field poly to active space	1





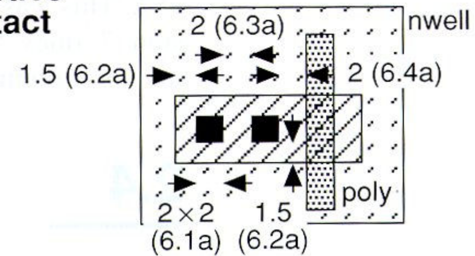
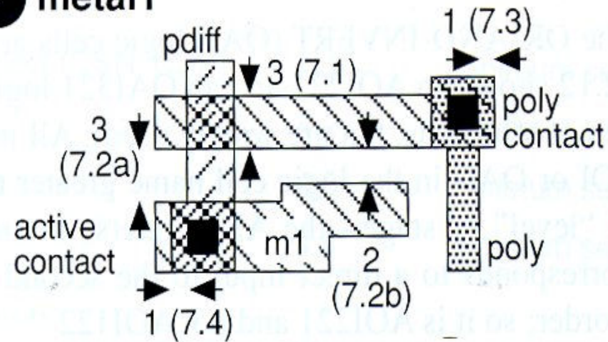


TABLE 2.7 MOSIS scalable CMOS rules version 7—the process front end.

Layer	Rule	Explanation	Value / λ
select (CSN, CSP)	4.1	minimum select spacing to channel of transistor[1]	3
	4.2	minimum select overlap of active	2
	4.3	minimum select overlap of contact	1
	4.4	minimum select width and spacing[2]	2
poly contact (CCP)	5.1.a	exact contact size	2×2
	5.2.a	minimum poly overlap	1.5
	5.3.a	minimum contact spacing	2
active contact (CCA)	6.1.a	exact contact size	2×2
	6.2.a	minimum active overlap	1.5
	6.3.a	minimum contact spacing	2
	6.4.a	minimum space to gate of transistor	2

[1]To ensure source and drain width.
[2]Different select types may touch but not overlap.



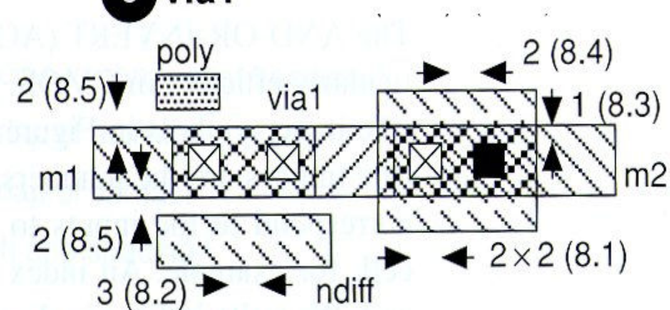


TABLE 2.8 MOSIS scalable CMOS rules version 7—the process back end.

Layer	Rule	Explanation	Value/λ
metal1 (CMF)	7.1	minimum width	3
	7.2.a	minimum space	3
	7.2.b	minimum space (for minimum-width wires only)	2
	7.3	minimum overlap of poly contact	1
	7.4	minimum overlap of active contact	1
via1 (CVA)	8.1	exact size	2×2
	8.2	minimum via spacing	3
	8.3	minimum overlap by metal1	1
	8.4	minimum spacing to contact	2
	8.5	minimum spacing to poly or active edge	2

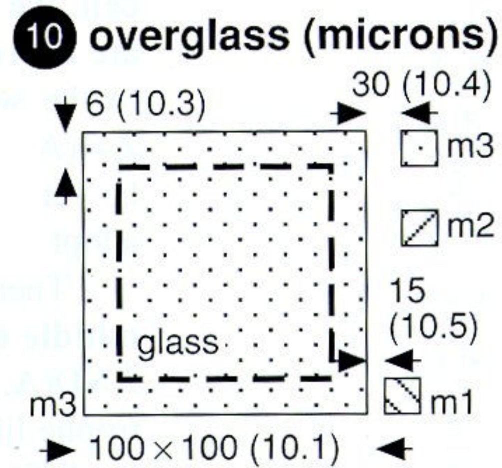


TABLE 2.9 MOSIS scalable CMOS rules version 7—the pads and overglass (passivation).

Layer	Rule	Explanation	Value
glass (COG)	10.1	minimum bonding-pad width	100μm × 100μm
	10.2	minimum probe-pad width	75μm × 75μm
	10.3	pad overlap of glass opening	6μm
	10.4	minimum pad spacing to unrelated metal2 (or metal3)	30μm
	10.5	minimum pad spacing to unrelated metal1, poly, or active	15μm

Etc.

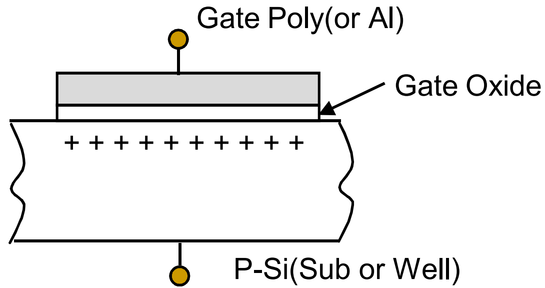
MOSFET Capacitances

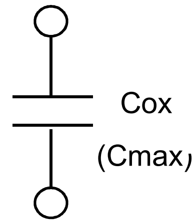
Latch-up

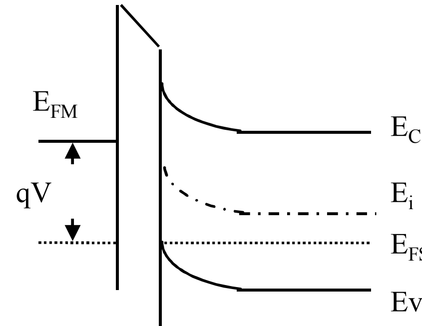
Device Reliability (TDDB, HCE)

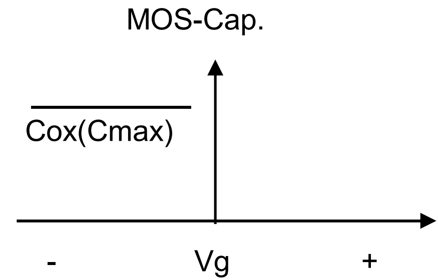
MOSFET Capacitance

1) Vg= negative : Accumulation

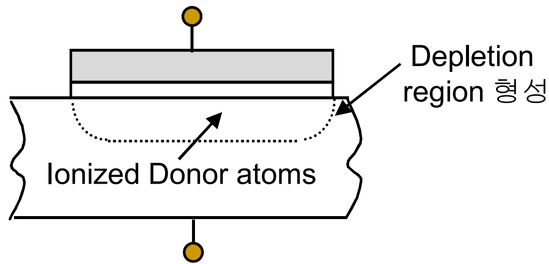


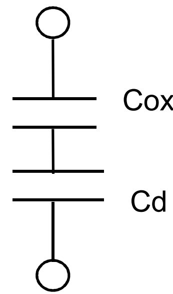


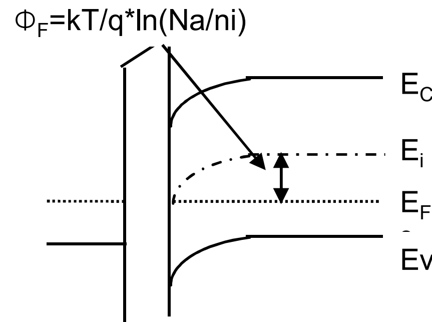


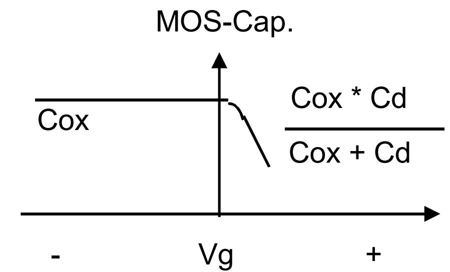


2) Vg= positive : Depletion

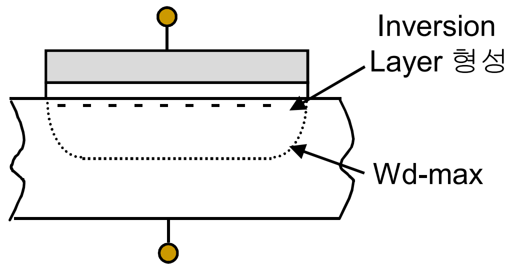


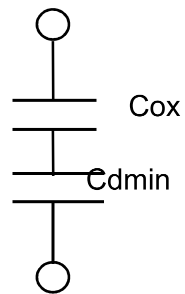


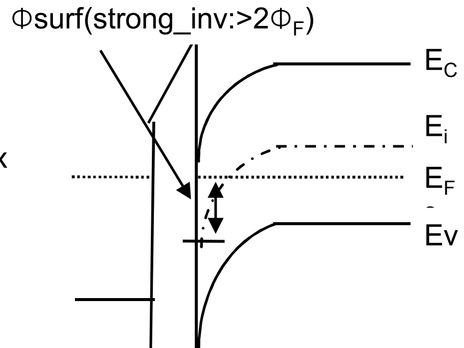


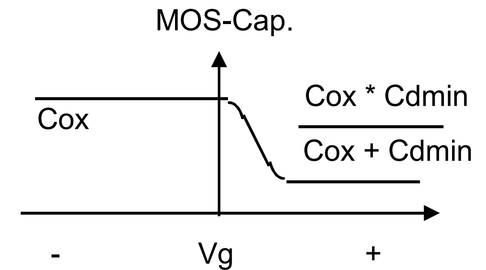


3) Vg= positive : Inversion



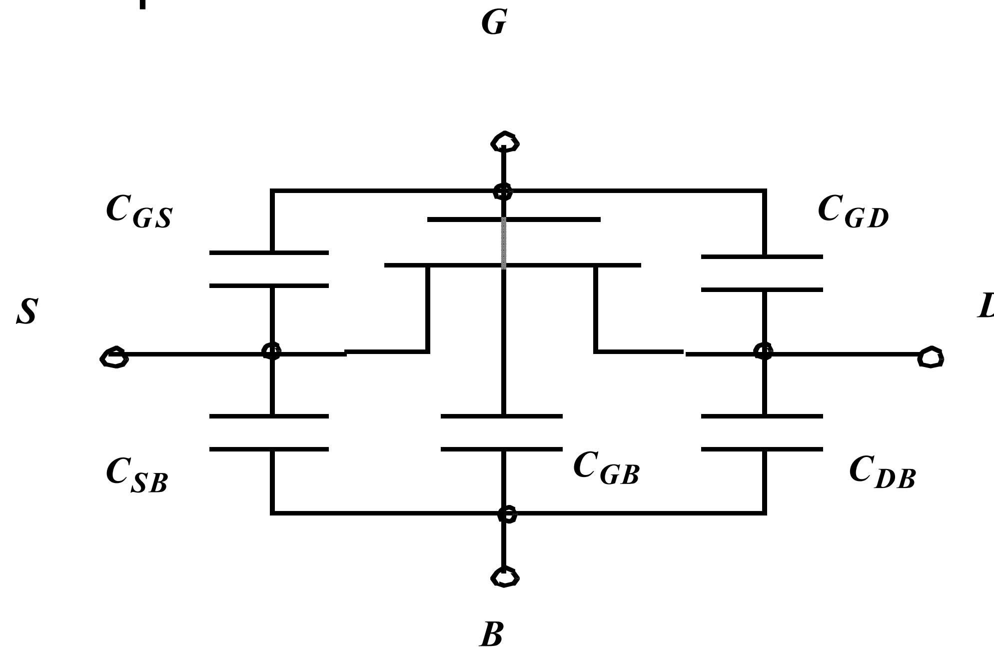






(cont'd) MOSFET Capacitance

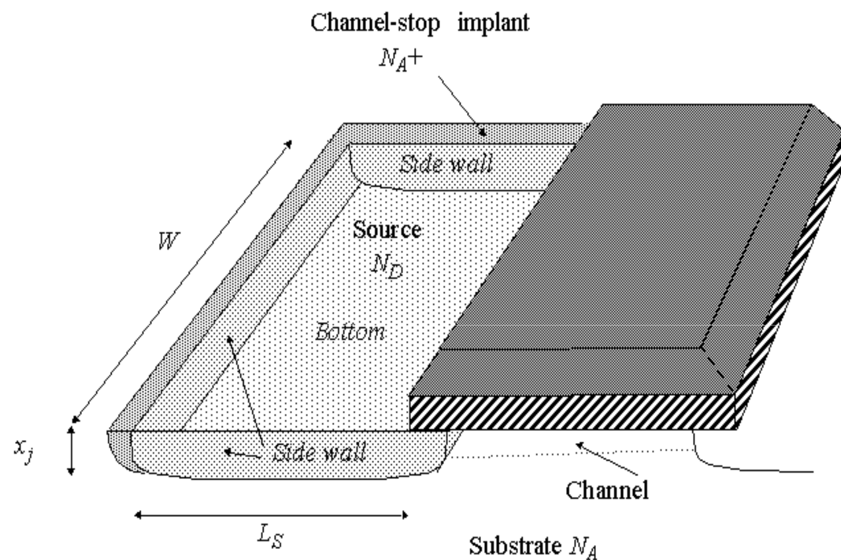
- Intrinsic Capacitance



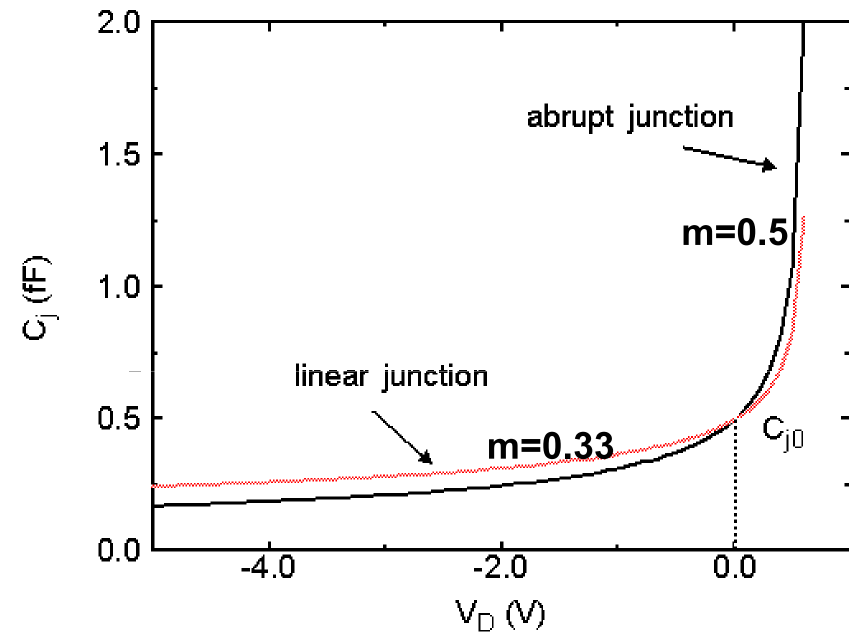
Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

(cont'd) MOSFET Capacitance

- Diffusion & Junction Capacitance



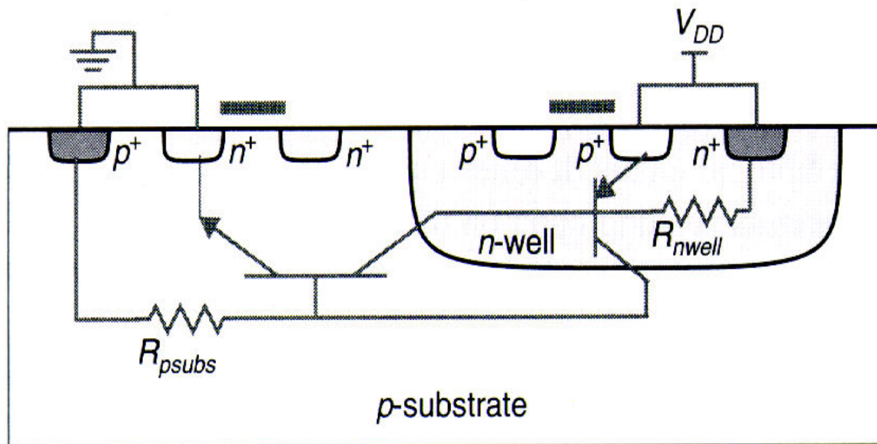
$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$



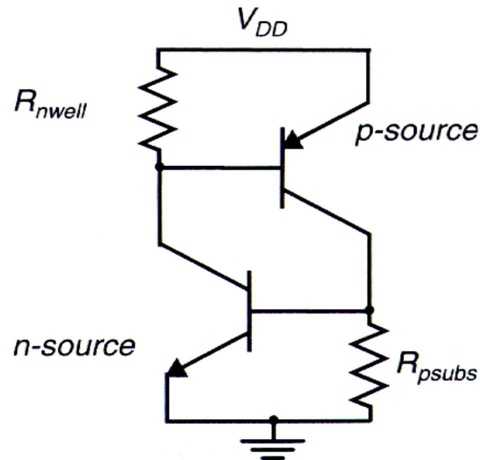
$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

Where m=grading coefficient

Latch-up



(a) Origin of latchup



(b) Equivalent circuit

i) When Rnwell = Rpsubs = 0

latch-up is impossible

ii) When Rnwell = Rpsubs = ∞

$\beta n \cdot \beta p \geq 1$ causes latch-up

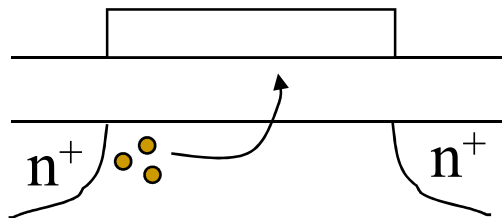
iii) When $0 <$ Rnwell, Rpsubs $< \infty$

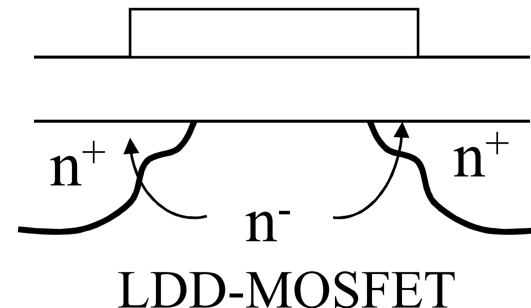
$\beta n \cdot \beta p \geq \alpha$ ($\alpha > 1$) causes trouble

- Why should circuit designers consider latch-up?
- When can Latch-up occur in real chip operation?
- How to eliminate latch-up?

Hot Carrier Effect (HCE)

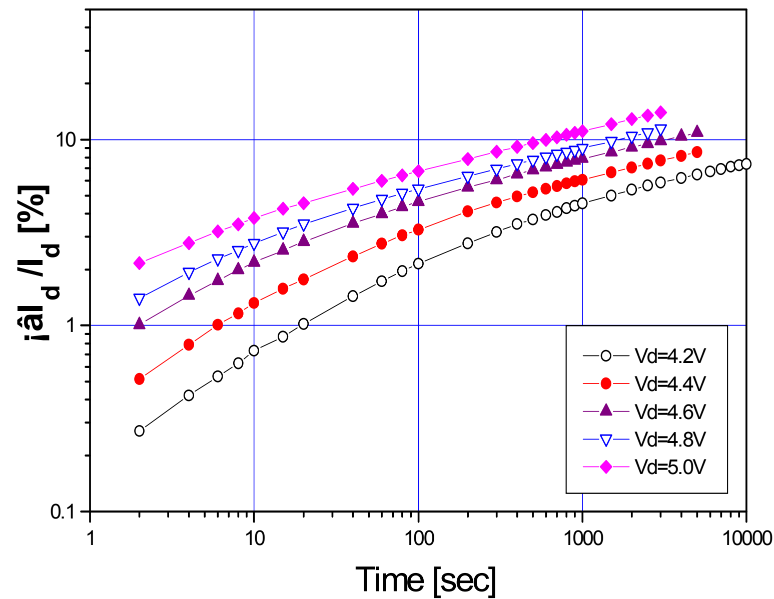
- For submicron MOSFET, electron becomes "hot" due to strong E(electric field) $\geq 10^4$ V/cm = 1V/μm
- E is very high near the drain junction
- LDD(Lightly-Doped Drain) MOSFET is effective for reducing the E-field near drain junction.
- Hot electron captured in the gate oxide through tunneling causes V_T instability (threshold drift).

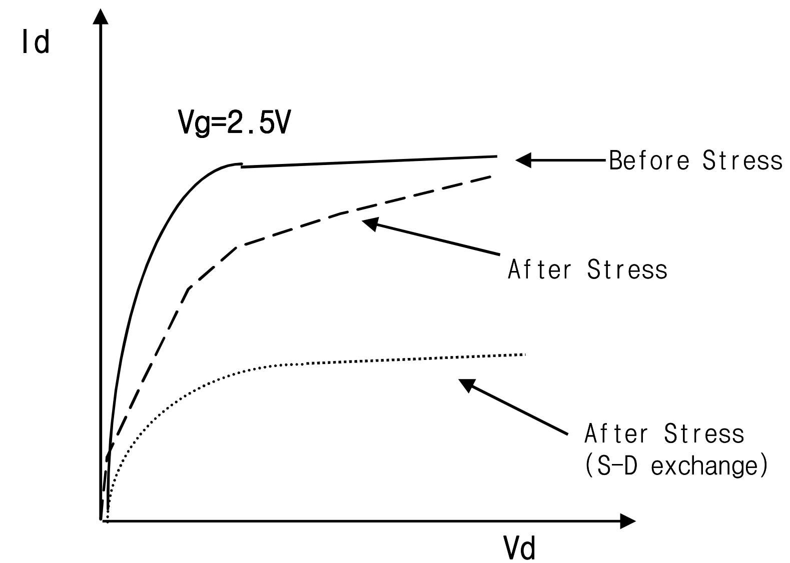




(cont'd) Hot Carrier Effect

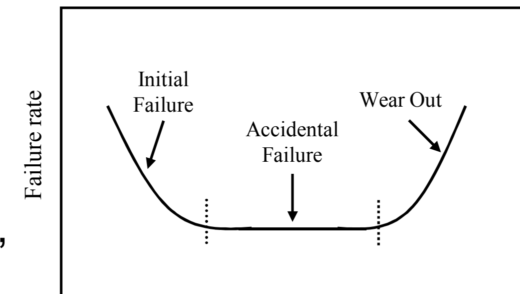
- Device degradation due to HCE



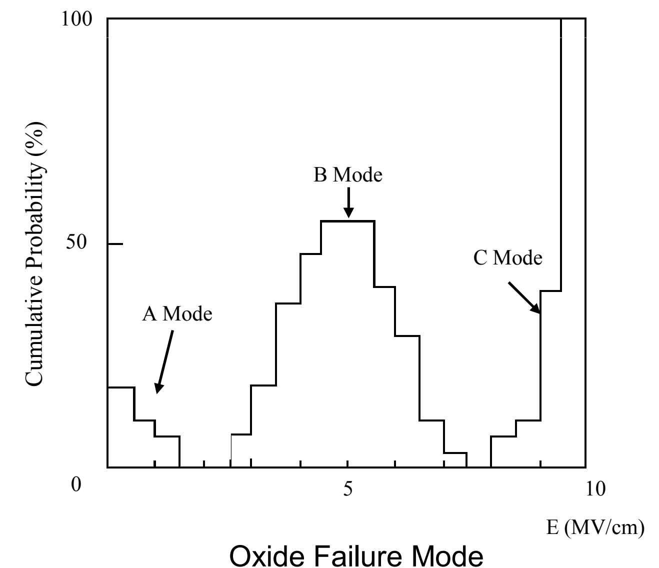


Dielectric Breakdown

- *TDDB (Time Dependent Dielectric Breakdown)*
  - Oxide lifetime estimation test
  - Bath tub curve (electronic system)
- *TZDB (Time to Zero Dielectric Breakdown)*
  - Voltage sweep test for characterizing oxide qualities, such as leakage current, BV, etc.
  - Oxide Breakdown Mode
    - *A Mode* : Initial failure
    - *B Mode* : TDDB range
    - *C Mode* : Failure by Critical Field Intrinsic failure range
- *Burn-in*
  - Accelerated *life test* for some fixed time period *to screen out* the weak components in order to improve reliability of components/systems



Time dependence of the failure rate of electronic system



Oxide Failure Mode