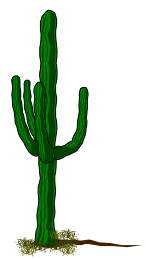
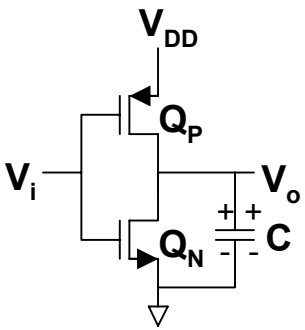
Power Dissipation

Power Dissipation
Active Versus Passive Power
“On” and “Off” Currents
High–K Dielectrics
Low-K Dielectrics

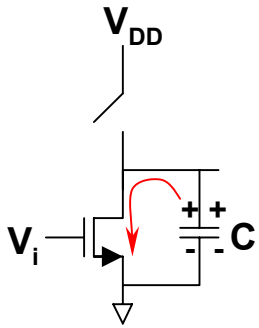


CMOS Power Dissipation

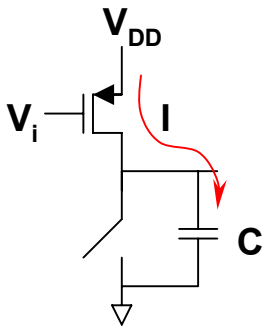
- CMOS is popular because it is a low power technology
- The main power dissipation occurs during switching



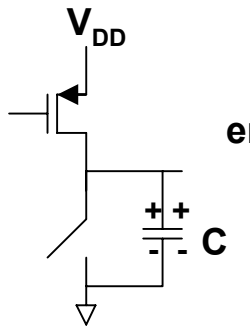
V_i low: Q_N off
C charged to V_{DD}
$E = CV_{DD}^2/2$



V_i high: Q_N on
C discharges through Q_N
$CV_{DD}^2/2$ dissipated in Q_N



V_i low: Q_P on, Q_N off
power supply delivers
$\int V_{DD} I dt = V_{DD} Q = CV_{DD}^2$ to C



V_i low: Q_P on, Q_N off
energy stored in C is $CV_{DD}^2/2$
$CV_{DD}^2/2$ dissipated in Q_P

CV_{DD}^2 total power dissipated

CMOS Power Dissipation

- **Power dissipation sources:**

$$P = P_{switch} + P_{sc} + P_{off}$$

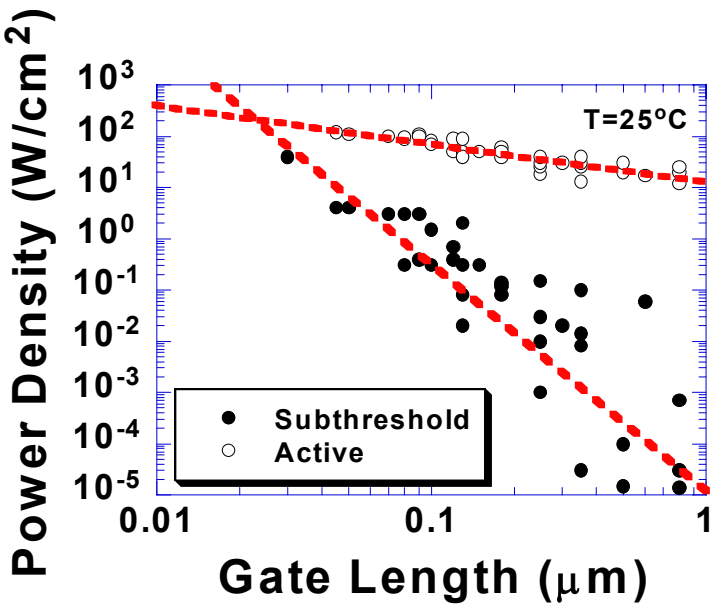
$$P_{switch} = \alpha f C V_{DD}^2;\ P_{sc} = I_{sc} V_{DD};\ P_{off} = I_{off} V_{DD}$$

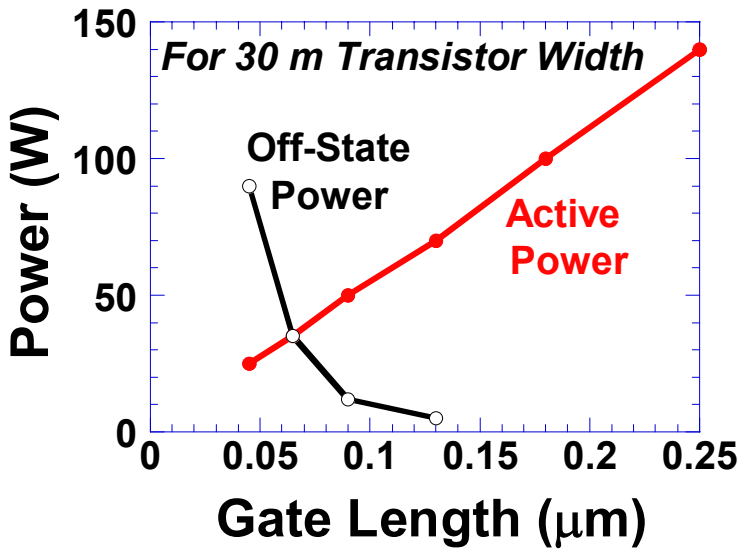
α: switching activity; I_{sc}: short circuit path when n and p-channel MOSFETs are "on"
I_{off}: drain leakage current and subthreshold leakage current when device is "off"

- **Reduce power by reducing**
  - Supply voltage V_{DD} $\Downarrow$; need to reduce V_T to maintain drive current
  - Capacitance C
  - Off current I_{off} - depends on V_T
  - Frequency f $\Downarrow$; parallel architectures

Active Versus Passive Power

- As V_T decreases, I_{off} increases $\Rightarrow$ P_{off} increases



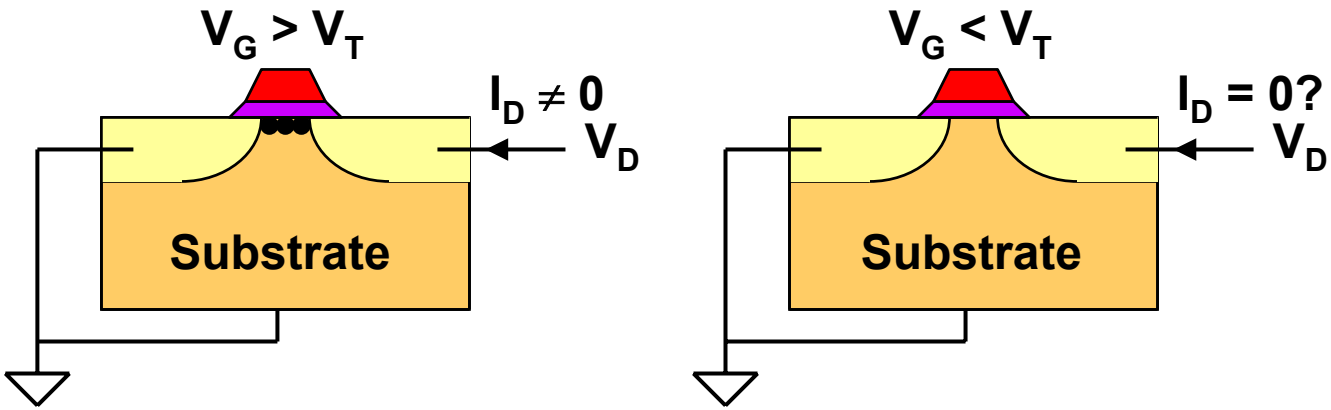


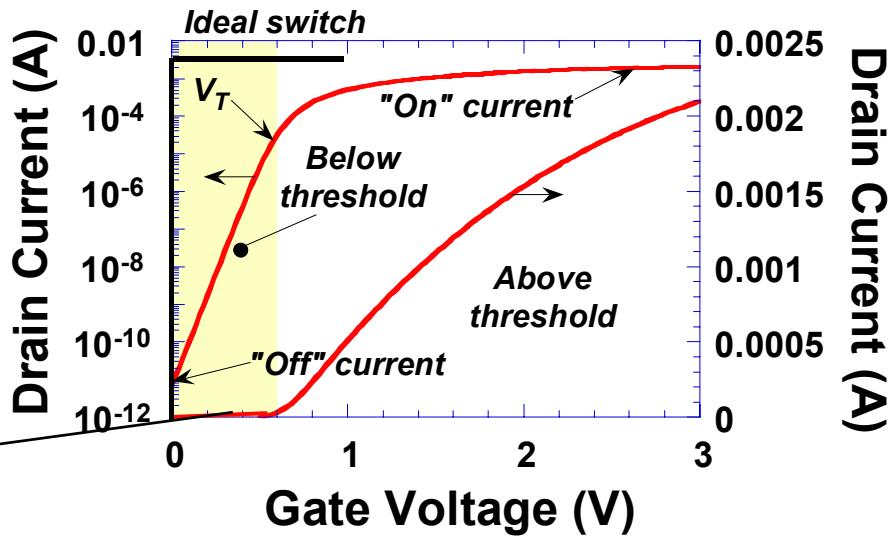
E.J. Nowak, *IBM J. Res. Dev.* **46**, 169 (2002)

B. Doyle, *Intel Technol. J.* 41 (May 2002)

MOSFET Switch

- In a digital circuit, a MOSFET is frequently used as a *switch*





$I_D = 0?$ No!

"On" – "Off" Current

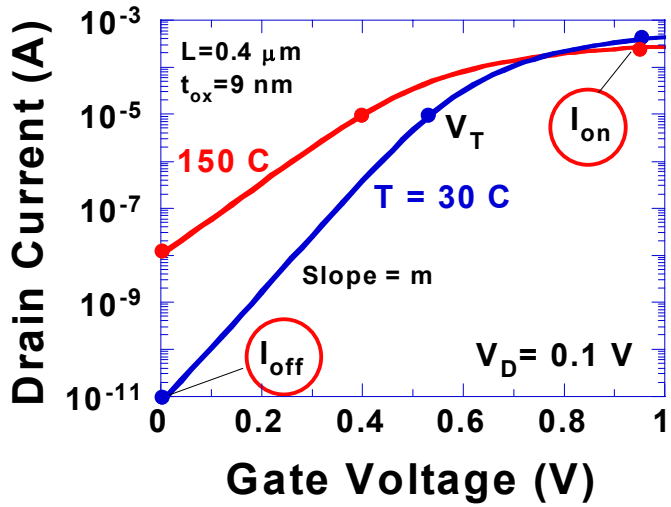
- ***Subhreshold***
  - ***Subthreshold slope = m; Subthreshold swing S = 1/m***

$$I_D = I_T e^{q(V_G - V_T)/nkT}$$

$$I_{off}(V_G = 0) = I_T e^{-qV_T/nkT}$$

$$S = \frac{dV_G}{d[\log(I_D)]} = \frac{2.3nkT}{q}$$

$$= 60n(T/300)\ mV/decade\ of\ I_D$$



- ***Above threshold***

$$I_{Dsat} = I_{on} = \frac{W\mu_{eff}C_{ox}}{2L}(V_G - V_T)^2$$

Want I_{on} high, I_{off} low !

"On" Current

- W/L ~ constant
- μ_{eff} ⇩
  - Reduced drive current
- V_G ⇩
  - Reduced electric field
  - Reduced power
  - Reduced drive current
  - Increased delay time
- V_T ⇩
  - Increased drive current
  - Increased "off" current

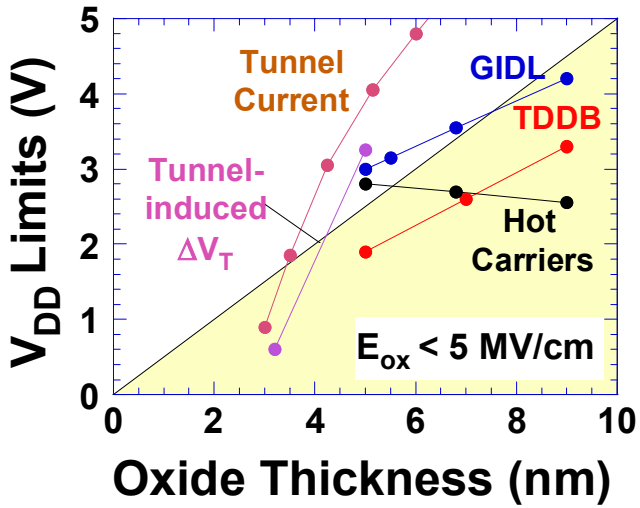
$$I_{on} = \frac{W}{2L}\mu_{eff}C_{ox}(V_G - V_T)^2$$

- $(V_G\text{-}V_T)$ ⇩
  - Reduced drive current
- C_{ox} ⇧ since t_{ox} ⇩
  - Increased drive current
  - Oxide leakage current
  - Boron penetration

I_{on} should not decrease!

Power Supply Voltage Limit

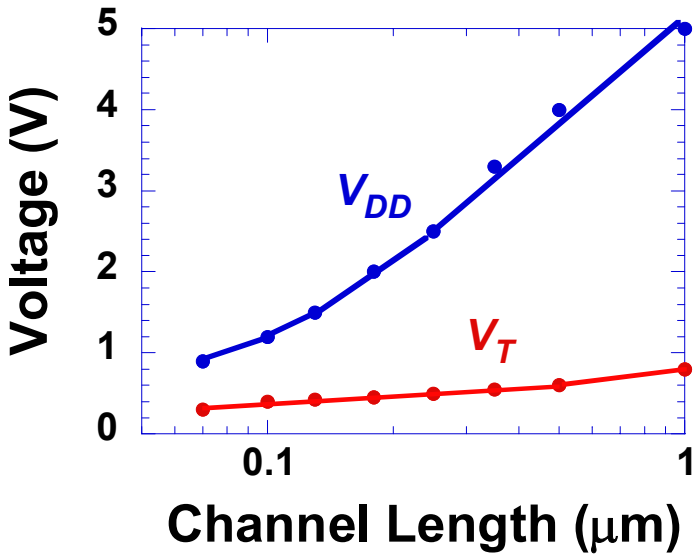
- $E_{ox} \approx 4$ - 5 MV/cm
- Power supply voltage is limited by
  - Power dissipation
  - Oxide leakage current
  - Gate-induced drain leakage current (GIDL)
  - Time-dependent dielectric breakdown
  - Hot carrier effects
  - Delay time



Data after: T. Hori,
Gate Dielectrics and MOS ULSIs,
Springer, 1997.

Threshold and Supply Voltages

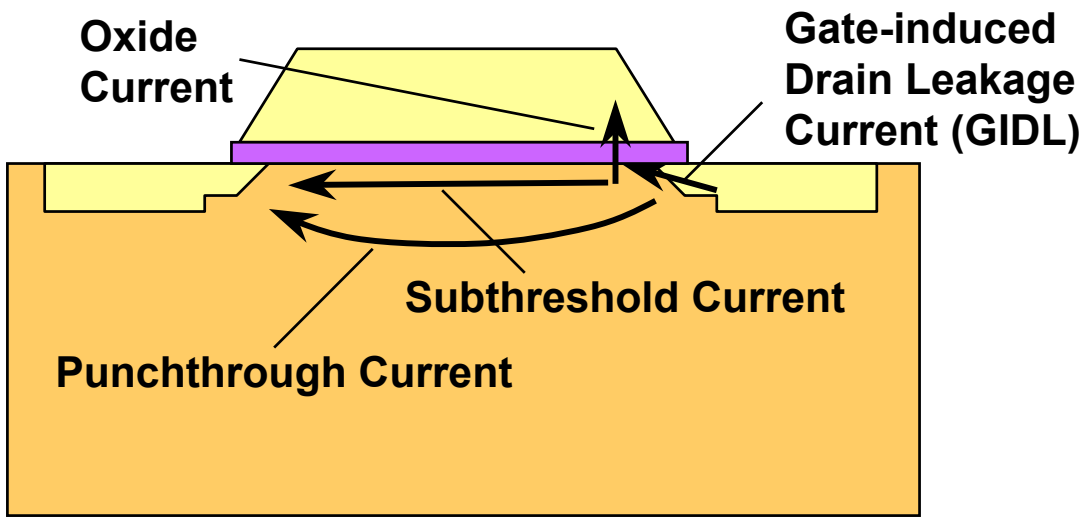
- How has V_T changed with V_{DD}? Less than called for by scaling rules
- V_{DD} - V_T is continually decreasing



$$(V_{DD} - V_T)^2 = 0.64V_{DD}^2$$

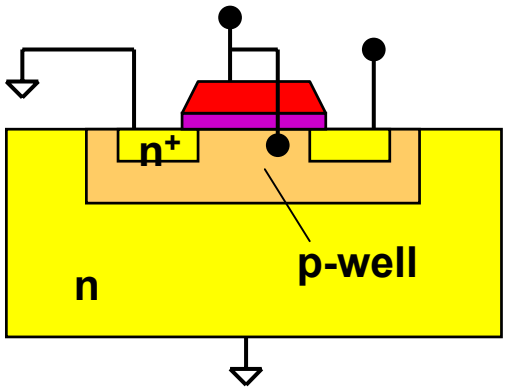
"Off" Current

- The "off" current is due to *subthreshold*, *punchtrough*, *gate-induced drain leakage*, and *oxide* currents

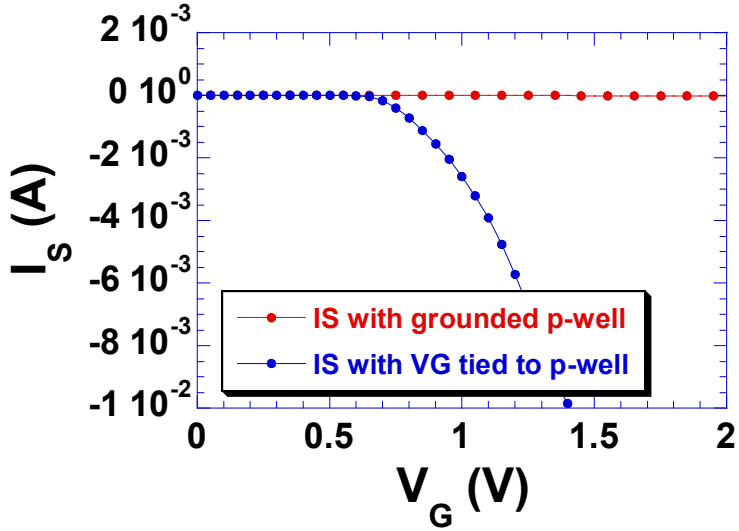


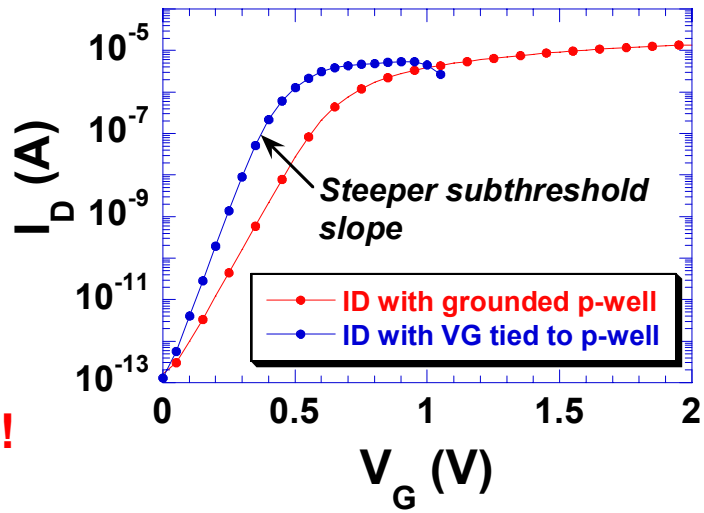
Positive Substrate Bias

- Forward bias $V_{SB} < 0$:
  - At $V_G = 0$, threshold voltage is high ⇒ low "off" current
  - At $V_G > 0$, threshold voltage is low ⇒ high "on" current



$$V_T = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F - V_{SB}}$$





$V_T \Downarrow$ with *forward*-biased S/B junction !

Propagation Delay Time

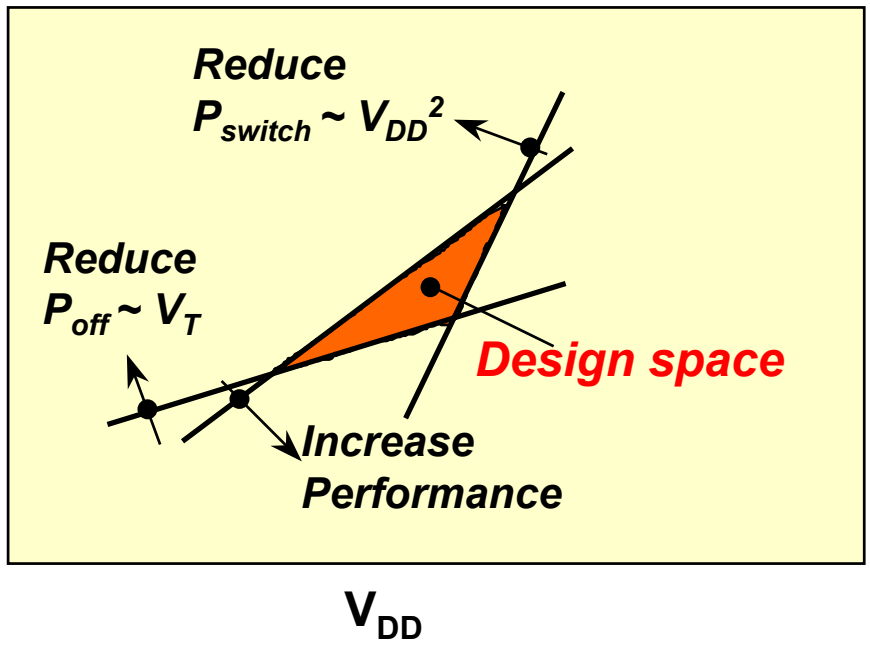
- Conflicting design requirements between reducing V_{DD}, V_T, I_{leak}, C, and increasing performance
- The propagation delay time is $t_d = \frac{C\Delta V}{I}$

$$t_d = \frac{CV_{DD}}{I_D}$$

$$= \frac{2LC}{W\mu_{eff}C_{ox}V_{DD}(1-V_T/V_{DD})^2}$$

$$= \frac{K}{C_{ox}V_{DD}(1-V_T/V_{DD})^2}$$

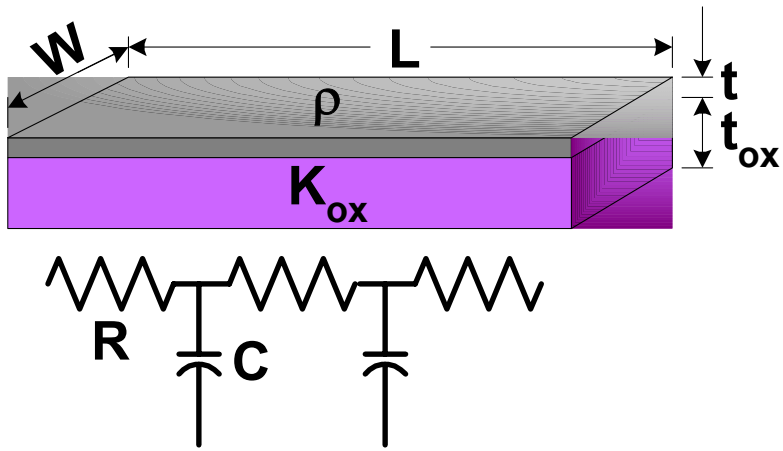
For low t_d want high V_{DD}, low V_T



Low - K Dielectrics

- Propagation delay along interconnects requires reduced K_{ox}
- Ideally K = 1 (air)
- Practically K < 3.5

$$\tau = RC = \frac{\rho L}{Wt}\frac{K_{ox}\varepsilon_o LW}{t_{ox}} = \frac{\rho K_{ox}\varepsilon_o L^2}{tt_{ox}}$$



Need low ρ and low K_{ox}

Low - K Dielectrics

- Low-K dielectrics reduce wiring capacitance
  $\Rightarrow$ reduce power

$$P = \alpha CfV^2$$

- Low-K dielectrics tend to be “fluffy”
- To reduce the dielectric constant, introduce air pockets into the material
  - Dielectric constant
  - Hardness
  - Adhesion
  - Thermal expansion
  - Process compatibility
  - Swelling

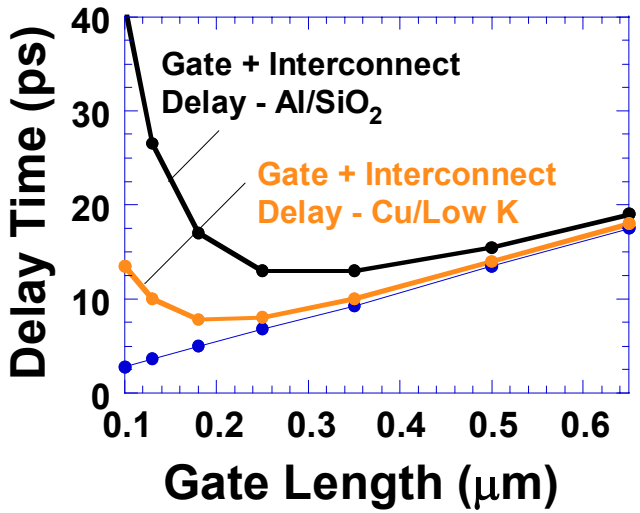
Low – K Materials

K Value	*Organic Polymers*	*Silsesquioxane Based*	*Silica Based*
4.2			SiO_2
3 – 4		FOX™	Fluorinated Silica
2.4 – 3	FLARE™	HOSP™	Aurora™
	BCB		Coral™
	SiLK™		Z3MS™
			Black Diamond™
2 – 2.4	Porous SiLK™	IPS™	Orion™
	PTFE	LKD™	Nanoglass™
		XLK™	
		Zirkon™	
< 2			Aerogel
			Xerogel

K. Maex et al., "Low Dielectric Constant Materials for Microelectronics," *J. Appl. Phys*. **93**, 8793-8841, June 2003.

Propagation Delay

- **Propagation delay depends on metal conductivity and interlevel dielectric constant**



Al: ρ = 3 $\mu\Omega$-cm
Cu: ρ = 1.7 $\mu\Omega$-cm
SiO_2: K_{ox} = 4
Low *K*: K_{ox} = 2
Al/Cu: 0.8 μm thick
Al/Cu: 43 μm long

M. T. Bohr, Interconnect Scaling - The Real Limiter to High Performance ULSI", *Proc. IEDM*, 241-242, 1995.

High - K Dielectrics

- **Why do we need high-K dielectrics?**

$$I_D = \frac{W\mu_{eff}C_{ox}}{L}(V_G - V_T)^2 = \frac{W\mu_{eff}K_{ox}\varepsilon_o}{Lt_{ox}}(V_G - V_T)^2$$

- **With scaling**
  - ***W*** **and** ***L*** **decrease same amount**
  - μ_{eff} **remains about the same or decreases**
  - $(V_G\text{-}V_T)$ **decreases**
- **To keep drain current constant**
  - t_{ox} **decreases – oxide leakage current increases**
  - K_{ox} **increases – thicker insulator, reduced oxide leakage current**

High - K Dielectrics

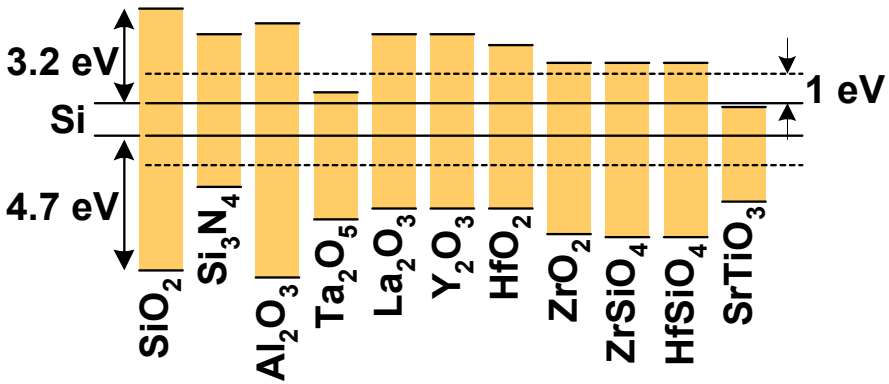
- The dielectric constant, band gap and dielectric/Si barrier height are important
- Tunneling probability

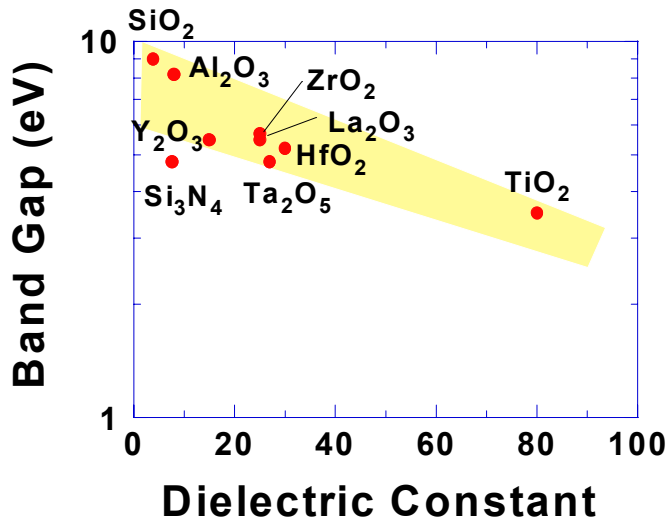
$$T = \exp\left(-2t_{ox}\sqrt{\frac{2qm^{*}\phi_{B}}{\hbar^{2}}}\right)$$

- Need
  - High dielectric constant
  - High band gap
  - High barrier at insulator/Si interface
  - Low leakage current
  - High reliability
  - Good insulator/Si interface quality
  - Low flatband voltage shift

High - K Dielectrics

- There is a trade off between
  - Dielectric constant
  - Band gap
  - Oxide/Si barrier height





HfO_2 and nitrided HfO_2 most promising

J. Robertson, *J. Vac. Sci. Technol*. **B18**, 1785 (2000)

High - K Dielectrics

- Problems
  - Low band gap
  - Low barrier height
  - Poor insulator/Si interface
    - Thin intervening SiO_2 layer
  - Oxide charge
  - Low electron/hole mobility
    - Strained Si
- MOS process compatible ?

Review Questions

- What determines CMOS power dissipation?
- What are “on” and “off” currents
- What determines propagation delay time?
- Why do we need low-K dielectrics?
- Why do we need high-K dielectrics?
- What are the conflicting demands of high *on* current and low *off* current?
- What are the conflicting demands of CMOS power dissipation and propagation delay time?