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Electrical Characterization of sub-30nm Gatelength SOI MOSFETs

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Abstract

Demonstrations of sub 20nm gate length MOSFET devices involving various FEOL (front end of line) schemes such as Silicon On DEpletion Layer (SODEL) FET's, asymmetric-gate FinFET devices, planar Ultra-thin body SOI (UTSOI) FET's, and, more recently, independently oriented surface channels for (110) pMOS and (100) nMOS described as Simplified Hybrid Orientation Technology (SHOT).[1-4, 7-18] have been reported.

SHOT FEOL integration for FinFETs can be combined on the same wafer as planar PDSOI and UTSOI MOSFETs [18].

According to International Technology Roadmap for Semiconductors (ITRS) guidelines [5] 20nm silicon layers with +/-5%, 6σ uniformity will be needed in 2004 timeframe[8] to guarantee threshold voltage (V_t) control [6].

Bonded Silicon on Insulator (SOI) processes that achieve +/-10 A film thickness have been shown [6] for these Ultra-Thin SOI (UT-SOI) devices at the 65nm node and beyond.

UT- SOI devices combined with SHOT (110) pMOS and (100) nMOS oriented surface channels offer optimizeed channel carrier mobility as well meeting issues of threshold voltage levels[4-18].

Discrete electrical characterization of sub 30nm gatelength thickness SOI MOSFET devices incorporating 20nm silicon layer thickness and less present challenges to conventional methods of electrical physical contact probing.

Besides involving feature sizes below optical light resolution limits, discrete devices at this technology node incorporate an effective-oxide-thickness (EOT) of less than 1.5nm. and gate lengths less than 30nm[1-4, 7, 15-17]. Shrinking critical dimensions (CD) mean SRAM cell sizes of less than 0.75um^2

Additionally, the 20nm silicon layer thickness and the thinning SOI box thickness of 80nm – 150nm [1-4, 15-17] in UT-SOI devices may be more sensitive to charging effects from incident energetic SEM electron-beams or Focused Ion Beam (FIB) gallium beams.

Atomic Force Probe (AFP) techniques are therefore particularly suited for electrical characterization of sub-65nm node SOI devices with multiple metal interconnect levels and low-k back end of line (BEOL) interlevel dielectric films.

AFP electrical measurements of sub-30nm gatelength SOI MOSFET devices will be described.

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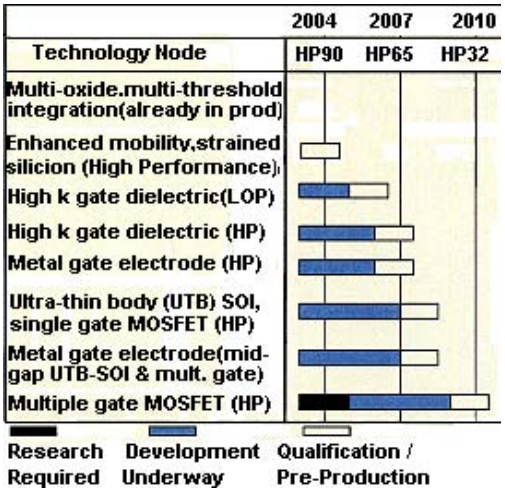
Introduction

Sub-30nm Gate length SOI MOSFET Devices

Continued scaling trends at the 65nm technology node and beyond present challenges not only for design and manufacturing but also for discrete device electrical characterization.

According to the 2003 International Technology Roadmap for high performance logic [5] development of UT-SOI MOSFET devices is fairly advanced at the 65 nm nodes. This is shown in TABLE I. [5]

Table 1: 2003 ITRS Roadmap for High Performance Logic[5]



Challenges of UT-SOI MOSFET Devices

Published reports of advanced FEOL integration approaches involving SHOT combined with UT-SOI have demonstrated, optimum pMOS and nMOS carrier mobilities.in smaller CD footprint cell sizes [15--17]. Separately, device performance enhancements with tungsten gates and HfO_2 gate dielectrics have also been demonstrated [4].

The device performance gains offered by these advanced FEOL approaches reflect the technology node performance levels predicted by the 2003 ITRS (International Technology Roadmap for Semiconductors for High Performance Logic).

Table 1 and Table II describe these predicted device parameters [5].

Recent reports of advanced FEOL integration approaches such as UT-SOI combined with Simplified Hybrid Orientation Technology (SHOT) show real promise for high performance CMOS.

Table II: 2003 IRTS High Performance Logic Roadmap [5]

YEAR	2004	2005	2007	2010
Technology Node (nm)	90	80	65	45
Physical Gate Length (nm)	37	32	25	18
Saturation Threshold Voltage	0.2	0.2	0.18	0.15
EOT (nm) equivalent oxide thickness	1.2	1.1	0.9	0.7
Nominal gate Ikg (A/ cm2) (current density limit @ 25 C)	4.5 E + 02	5.2 E + 02	9.3 E + 02	1.9 E + 0
NMOS Id sat (mA/mm) (saturation drive current)	1110	1090	1510	1900

Manufacturable solutions exist and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known

These developments include optimum pMOS and nMOS carrier mobilities.in smaller CD footprint cell sizes [16, 17]. Further device performance enhancements with tungsten gates and $HfO_{2\ gate}$ dielectrics that exhibit desirable threshold voltage characteristics with UT-SOI MOSFETS have also been reported [1-18].

UT-SOI MOSFET and Simplified Hybrid Orientation Technology (SHOT)

Advanced FEOL integration approaches involving FinFET devices and, more recently UT-SOI combined with Simplified Hybrid Orientation Technology (SHOT) have been reported [1-18]

In recent work reported by B.Doris et. al of UT-SOI combined with SHOT, show significant advances for high performance CMOS [17,18]. These developments include optimum pMOS and nMOS carrier mobilities.in smaller CD footprint cell sizes [17-18].

Figure 1 by B.Rainey, et al shows a micrograph of a FinFET device detailing each feature [19]

Figure 2 by B.Doris, et al. shows a micrograph of an SRAM cell where the FinFETs and UPTSOI – SHOT are combined in a small CD footprint [17,18].

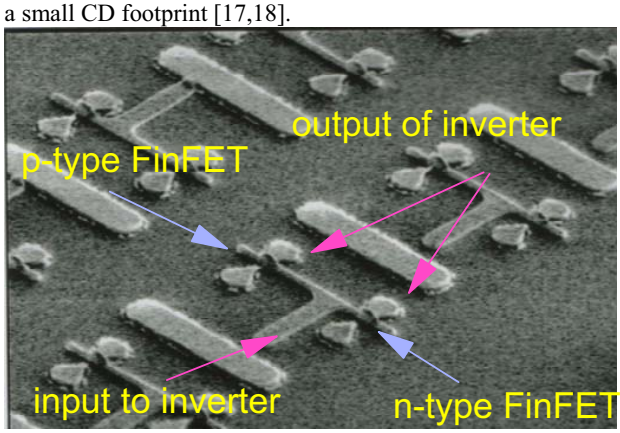


Figure 1: Micrograph by B.Rainey, et al [19] detailing individual FinFET features

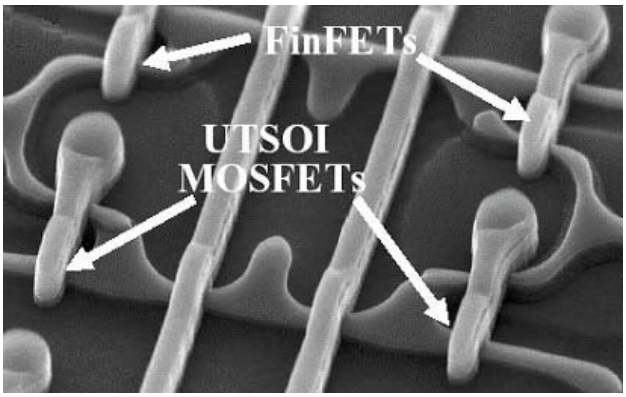


Figure 2: SEM FinFET SRAM cell involving UT-SOI integrated with SHOT. Figure 2 courtesy of B. Doris, et.al. [17,18]

AFP Probing of 30nm Gate length SOI MOSFET Devices

At the 65nm node and below, scaling trends in thinner silicon layer thickness, thinner gate dielectric films combined with SOI wafer substrate materials underscores the desirability of AFP in electrical characterization

This technology node typically employs BEOL low-k dielectric interconnect films combined with optically irresolvable copper via interconnects. Clearly, alternatives to conventional tungsten wire probing of the copper interconnects are required to avoid damaging the underlying low modulus BEOL dielectric films [19].

AFP avoids the risks attendant with highly energetic incident SEM electron beams or FIB gallium ion beams that could rupture the thin gate films or induce charging effects on the thin silicon layer.

Moreover, gallium ion implantation during FIB deposition of tungsten pads for electrical contact probing pose real issues of ion induced shifts in threshold voltage characteristics of SOI MOSFET devices. [20,21].

Figure 3 shows three AFP probes contacting a 30nm gate length SOI MOSFET in an SRAM array. Here the SRAM array cell size is less than 0.75 μm^2 for this 65nm node technology.

Figure 4 shows the family of curves for this 30nm gate length NFET transfer following AFP probing of area shown in Figure 3

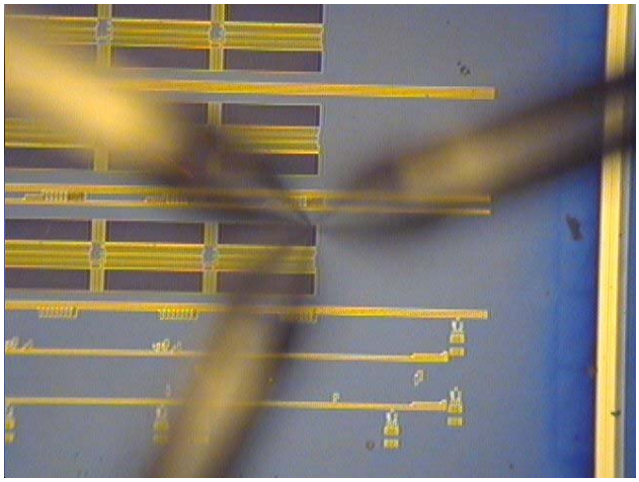


Figure 3: AFP three-point probe of a 30nm gate length SOI SRAM MOSFET array.

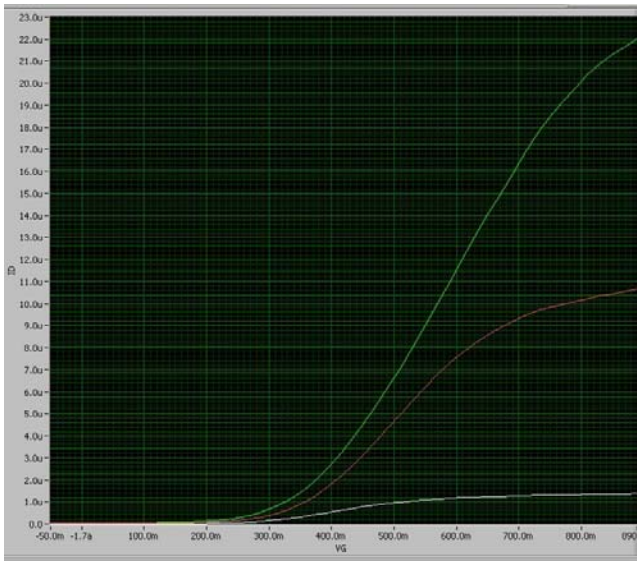


Figure 4: Family of curves for 30nm gate length NFET transfer device in SRAM array following AFP probing of area shown in Figure 3.

AFP Sample Preparation Procedures

As with any atomic force instrument (scanning capacitance microscopy [SCM], scanning probe microscopy [SPM], or scanning sheet resistance microscopy [SSRM]), sample surface preparation is all-important for any successful outcome.

For discrete MOSFET device electrical characterization, the region of interest must be planar and deprocessed to slightly expose the tungsten interconnects level. For optimum AFP scanning, imaging, the dielectric layer surrounding the tungsten interconnection must be recessed below the height of the tungsten via. This is accomplished by brief buffered hydrofluoric wet etch. The objective is to recess the dielectric layer surrounding the tungsten via to a depth of approximately 20 to 60 angstroms. Wet etching is usually accompanied by an ethanol or isopropyl rinse to remove any residuals and a nitrogen gas aerosol blast.

It is recommended to immediately begin AFP probing of the sample. If this is not the case, the sample should be stored in a nitrogen purge atmosphere cabinet to minimize surface oxidation of the tungsten interconnect.

BEOL via interconnect deprocessing is dependent on the type of BEOL build such as via metal type (copper or aluminum-copper), interlevel dielectric type (low-k dielectric, conventional oxide deposited film, or FTEOS).

Surface preparation is not only essential for electrical contact but also for satisfactory AFP scanning. /imaging of the specific site under investigation. A surface with a topology roughness of greater than 10 RMS is not optimum for scanning / imaging and can, like any other AFM technique, damage the tips.

Figure 5 is an example of a properly prepared surface that yields an adequate AFM surface image necessary for site-specific probe tip touch down and subsequent electrical characterization.

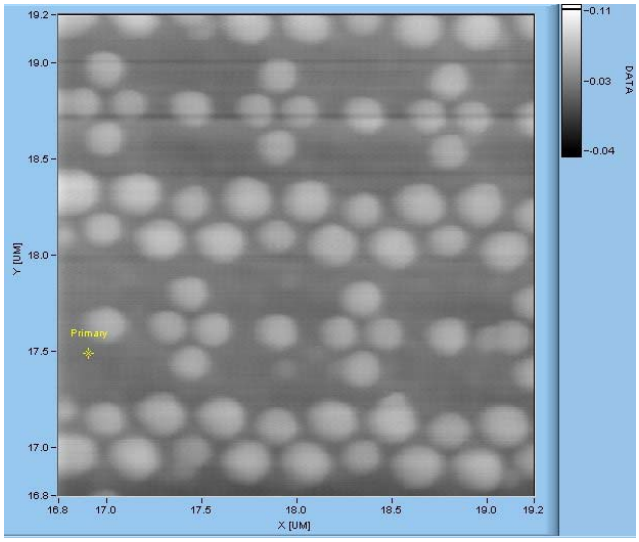


Figure 5: AFP scanning image of tungsten interconnects in 30nm gate length SOI MOSFET SRAM array.

AFP Characterization of Ion Beam Damage in 90nm SRAM Array

As device geometries shrink and gate dielectric film thick nesses are reduced below 2nm, the susceptibility of MOSFET devices (particularly SOI MOSFET devices) to charge induced damage becomes pronounced.

In dense, minimum spacing array regions like SRAM CACHE arrays, incident energetic SEM electron beams (above 5 kEV)

or Focused Ion gallium beams become especially vulnerable to charge induced device damage [21,22].

AFP electrical probing was performed in an area adjacent to a FIB deposited oxide pad in preparation for FIB deposited tungsten probe pads. In this experiment, the incident FIB beam was 7kEV acceleration voltage whereas in another region, the acceleration voltage was 50kEV.

In areas adjacent to the FIB deposited oxide pads, AFP was performed on exposed tungsten via interconnects. AFP electrical results disclosed leaky gates adjacent to these FIB deposited oxide pad regions. Other areas, remote from the FIB deposited pad areas showed normal electrical characteristics.

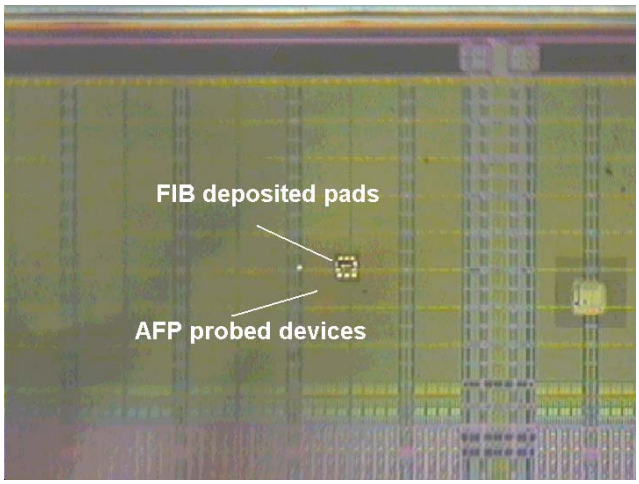


Figure 6: SRAM array with FIB deposited tungsten pads for contact electrical probing. Note adjacent region characterized by AFP

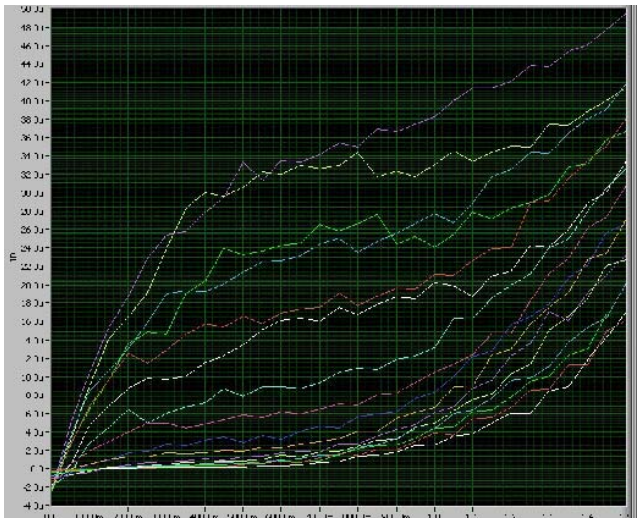


Figure 7: Family of curves obtained by AFP probing SRAM device in region adjacent to FIB tungsten deposited pads. Note leaky gate characteristics.

Conclusions

The applicability of AFP (atomic force probing) for electrical characterization of sub 30nm gate length SOI MOSFET devices and beyond has been described. AFP is particularly suitable for electrical characterization of 65nm node BEOL structures where the copper interconnects is no longer optically resolvable with conventional light optics

AFP probing 65nm technology node and below where BEOL build involves low k, low modulus dielectric films is especially applicable.

Requisite sample preparation steps required for AFP probing have been discussed. Both AFP probe tip life, AFP image quality as well as the AFP electrical outcome are all dependent on planar surface topology and necessary recessing of the dielectric surrounding the metal interconnect to be AFM imaged and contacted.

The extendibility of AFP to multi gate, non-planar MOSFET devices (FinFETs) is currently under investigation with satisfactory results to date [20]

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