The Enhancement of Gate-Induced-Drain-Leakage (GIDL) Current in Short-Channel SOI MOSFET and its Application in Measuring Lateral Bipolar Current Gain β

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***Abstract*—A new off-state leakage current unique for short-channel SOI MOSFET's is reported. This off-state leakage is the amplification of gate-induced-drain-leakage (GIDL) current by the lateral bipolar transistor in a SOI device due to the floating body. The leakage current can be enhanced by as much as 100 times for 1 / 4-μm SOI devices. This can pose severe constraints in future 0.1-μm SOI device design. A novel technique was developed based on this mechanism to measure the lateral bipolar transistor current gain β of SOI devices without using a body contact.**

I. Introduction

MINIMIZATION of off-state leakage current is an important issue in high-density, very low-power, battery-powered CMOS technologies. With the scaling of VLSI technology, MOS device channel lengths and gate oxide thickness decrease continuously. In bulk MOSFET's, one type of leakage current for very thin gate oxide is the gate-induced-drain-leakage (GIDL) current caused by band-to-band tunneling in the gate/drain overlap region [1]–[3]. A SOI device with ultrathin Si film (less than 100 nm) offers several advantages over bulk devices including reduced short-channel effects and significantly reduced junction and punchthrough leakage currents [4]. In this paper, we report for the first time a new off-state leakage current especially important for short-channel SOI MOSFET's. This off-state leakage is the amplification of GIDL current due to the floating body, and can pose severe constraints in 0.1-μm SOI device design. A novel technique is also developed, based on this mechanism, to measure the lateral bipolar transistor current gain β of SOI devices without body contact. This gain has a major impact on the breakdown voltage of SOI devices.

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II. The Enhancement of GIDL in SOI MOSFET

The SOI devices used in this study were LDD and non-LDD MOSFET's fabricated with modified submicrometer CMOS technology on SIMOX (Separation by IMplanted OXygen) wafers. The SIMOX wafers were implanted with a high dose of oxygen ions ($10^{18}/cm^2$) at 200 keV and subsequently annealed at 1230°C. The n^+ polysilicon gate is *in-situ* doped with phosphorus and the p^+ polysilicon gate is implanted with boron. The n^+ polysilicon gate thickness, the p^+ polysilicon gate thickness, and the buried oxide thickness are 250, 300, and 400 nm, respectively. The gate oxide thickness is 12 nm and the Si film thickness is 85 nm.

Fig. 1 shows the schematic diagram of current flow in a SOI n-channel MOSFET at GIDL mode with the front channel turned off. The high electric field in the gate/drain overlap region causes electron tunneling from valence band to conduction band. In a bulk NMOS, electrons flow to the drain and the holes flow to the substrate as substrate current. It is well known that the GIDL current is independent of bulk MOSFET channel length [1]–[3]. However, in the case of a SOI MOSFET, since the body is floating, holes can only flow to the floating body and forward bias the source–body junction. The source-body junction serves as the emitter–base junction, and the GIDL current serves as the base current of the lateral bipolar transistor (BJT).

The off-state leakage currents in SOI NMOS are measured for different channel lengths at $V_G = -5$ V as shown in Fig. 2. The gate oxide thickness is 12 nm and the channel width is 10 μm. The device is biased such that the front channel is turned off and there is no surface channel current. The GIDL current I_{GIDL}, which is independent of channel length L, is amplified by the lateral BJT. The current amplification due to drain impact ionization can be neglected in the drain voltage range of our study. The measured drain current is therefore $(\beta + 1)I_{GIDL}$, where β is the current gain of the lateral BJT.

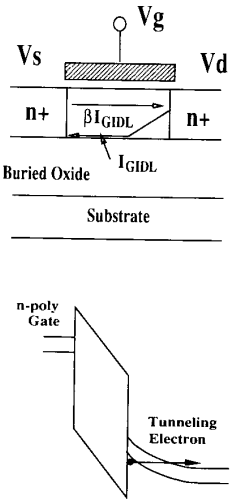

Fig. 1. Schematic of n-channel SOI MOSFET current flow in GIDL mode when the front channel is turned off and high electric field is present between drain and gate. Band-to-band tunneling occurs at the gate/drain overlap region.

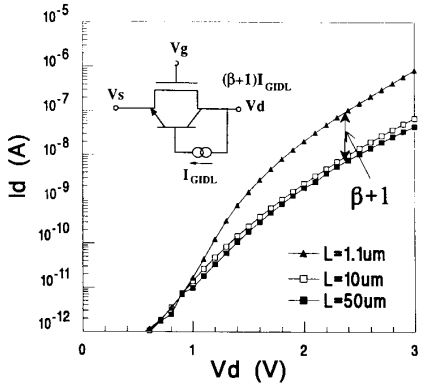

Fig. 2. Off-state leakage currents of long- and short-channel SOI MOSFET's. I_{GIDL} is the base current of the lateral bipolar transistor and gets amplified. From the ratio of those two the bipolar current gain β of the short-channel device can be deduced.

For the long-channel device, e.g., $L = 50$ μm, $\beta = 0$ and the measured drain current is simply I_{GIDL}. But for very short-channel devices, as the channel length decreases, the base width of the lateral BJT decreases and the current gain β increases, thus amplifying the GIDL current.

The GIDL currents for $L = 10$-μm and $L = 50$-μm devices are the same as shown in Fig. 2, which is expected since they both have long base width and, therefore, near zero current gain. However, as shown in Fig. 2, when the channel length (base width) decreases, the GIDL current is amplified and is higher than the current for long-channel devices. Comparing the devices with $L = 1.1$ μm and $L = 10$ μm, the currents are equal for low I_D because β is very small at very low collector current levels [5]. Current gain β increases with increasing collector current level.

Temperature measurements are performed to verify the above theory. GIDL currents are measured for devices with $L = 1$ μm and $L = 50$ μm at 25°C and 150°C as shown in Fig. 3. For the $L = 50$-μm device, the GIDL current increases uniformly by a factor of 2. This is because all the measured drain current is band-to-band tunneling current. The measurement agrees with the well-known tunneling current temperature dependence [1], [5]. However, for the device with $L = 1$ μm, the current increases more than 5 times. Tunneling current temperature dependence alone cannot explain the increase. Note that at low current levels, the current increase at 150°C is about 2 times, and approaches 5 at higher current levels. This is because with increasing collector current level β increases, while β increases with increasing temperature [5]. The temperature dependence further confirms the theory of amplification of GIDL current in SOI MOSFET's.

III. Discussions

Lateral bipolar transistor effects are very important for understanding of SOI MOSFET breakdown [6], [7]. Some efforts were made to measure the lateral bipolar gain [8], but a body contact was required. It is desirable to be able to measure the lateral bipolar transistor current gain in SOI MOSFET's with body contact. Recall that the ratio of the drain current for a short-channel and a long-channel device is $\beta + 1$. This can be used to measure the lateral BJT current gain without a body contact. Fig. 4 shows the measured β for different channel lengths at substrate bias $V_{BS} = 0$ V and $V_{DS} = 2$ V. As can be seen from Fig. 2, the current gain β is relatively a constant for collector current ranging from 10^{-6} to 10^{-9} A. The current gain is close to zero for channel lengths above 4 μm, and is not sensitive to gate voltages. β is also plotted against channel length L in logarithmic scale in the insert. The slope is approximately 2 for channel length less than 4 μm. This is interesting from a modeling point of view. It is estimated from this that the electron diffusion length is approximately 4 μm, which is very close to the value reported in [8].

The enhancement of off-state leakage GIDL current can be a serious problem for short-channel SOI MOSFET's. From measurement and previous study [1]–[3], for a device with $T_{ox} = 6$ nm operating at $V_d = 3.3$ V and $V_g = 0$ V, the leakage current for a long-channel device is about 10 pA/μm. But the leakage current for a short-channel device with $L = 1$ μm is about 100 pA/μm. For even shorter channel length, the amplification could be even more severe. So far all the studies have been conducted on NMOS devices with n^+ polysilicon gate. In order to obtain reasonable threshold voltage for CMOS SOI devices, it has been suggested that an n-channel device with p^+ polysilicon should be used [9]. Because of the work-function difference of 1 V for n^+ and p^+ poly

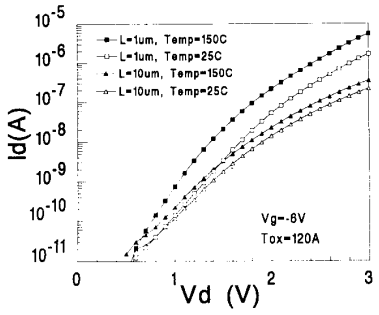

Fig. 3. Measured off-state leakage current as a function of temperature for both long- and short-channel SOI devices.

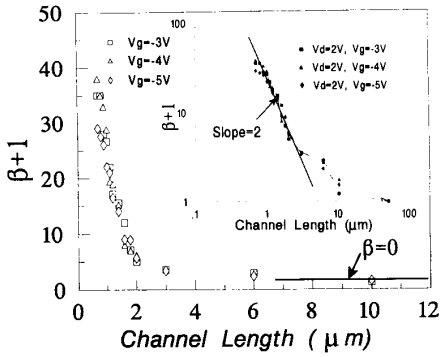

Fig. 4. Measured SOI lateral bipolar transistor current gain β for different channel lengths. The electron diffusion length is estimated to be 4 μm.

gates, devices with p^+ gate will suffer from GIDL current at lower drain voltage [2]. This is important at low power supply operation when total V_{DD} is only less than 2 V. It is expected that for the future 0.1-μm SOI devices with gate oxide thickness in the range of 5–6 nm, this enhancement of off-state leakage current could be a major problem for the intended high-density battery-based operations. LDD structures must be used to reduce the electric field and lateral BJT current gain, therefore reducing the enhancement of GIDL current.

IV. Conclusions

The enhancement of off-state gate-induced-drain-leakage current is significant for short-channel SOI MOSFET's. The mechanism is due to the floating body of SOI structure; the GIDL current serves as base current of the lateral bipolar transistor and gets amplified. For very short-channel devices, this current gain can be as high as 100, and the leakage current will be enhanced as much as 100 times. This may be another barrier to SOI MOSFET scaling, especially for the future 0.1-μm SOI device used in battery-based low-power applications. Possible solutions are the use of lightly doped drain devices which will lower the electric field between drain/gate and the bipolar current gain, therefore lowering both the GIDL current and the amplification due to lateral BJT. Utilizing the phenomenon of enhancement of GIDL current in SOI, a novel method was also developed to measure the SOI lateral bipolar transistor current gain β without using a body contact.

Acknowledgment

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References

[1] J. Chen, T. Y. Chan, I. C. Chen, P. K. Ko, and C. Hu, "Subbreakdown drain leakage current in MOSFET's," *IEEE Electron Device Lett.*, vol. EDL-8, p. 515, 1987.

[2] T. Y. Chan, J. Chen, P. K. Ko, and C. Hu, " The impact of gate-induced-drain-leakage on MOSFET scaling," in *IEDM Tech. Dig.*, Dec. 1987, p. 718.

[3] C. Chang and J. Lien, "Corner-field induced drain leakage in thin oxide MOSFET's," in *IEDM Tech. Dig.*, Dec. 1987, p. 714.

[4] S. Veeraraghavan and J. G. Fossum, "Short channel effects in SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 36, p. 522, 1989.

[5] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981.

[6] K. K. Young and J. A. Burns, "Avalanche-induced drain-source breakdown in silicon-on-insulator n-MOSFET's," *IEEE Trans. Electron Devices*, vol. 35, p. 426, Apr. 1988.

[7] J. S. T. Huang, J. S. Keung, and T. Fabian, "An analytical model for snapback in n-channel SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 38, p. 2082, Sept. 1991.

[8] J. M. Hwang, H. Lu, Y. D. Sheu, W. Bailey, P. Mei and G. Pollack, "Premature breakdown in non-fully depleted SOI/MOSFETs with body-tied-to-source structure," in *IEEE 1991 Int. SOI Conf.* 1991, p. 34.

[9] L. K. Wang *et al.* "Enhanced performance of accumulation mode 0.5 μm CMOS/SOI operated at 300K and 85K," in *IEDM Tech. Dig.*, Dec. 1991, p. 679.