INFN
Sezione di Genova

LHCb

Glue Logic Interface

for Smart PC and Test Board

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Glue Card Features

Busses: 4 I2C (100/400Kb/s), 3 JTAG (≈1Mb/s), 1 PLX 9030 Local Bus @ 40Mhz

FPGA Program: The Xilinx FPGA is connected to the CC-PC parallel port in order to be able to use the commercial programs but also a PROM can be used.

Access during use: All the devices on the glue card are connected to the 9030 local bus and can be reached from the PCI bus.

Logical Devices: The three logical devices of the glue card are the I2C controller (2 addresses), the JTAG controller (8 addresses) and the Enable register (1 address).

Addresses: All the addresses will be located under the PLX9030 address space 0. The Chip select 0 (CS0) is used by the glue card so it cannot be used by users.

Reset Logic

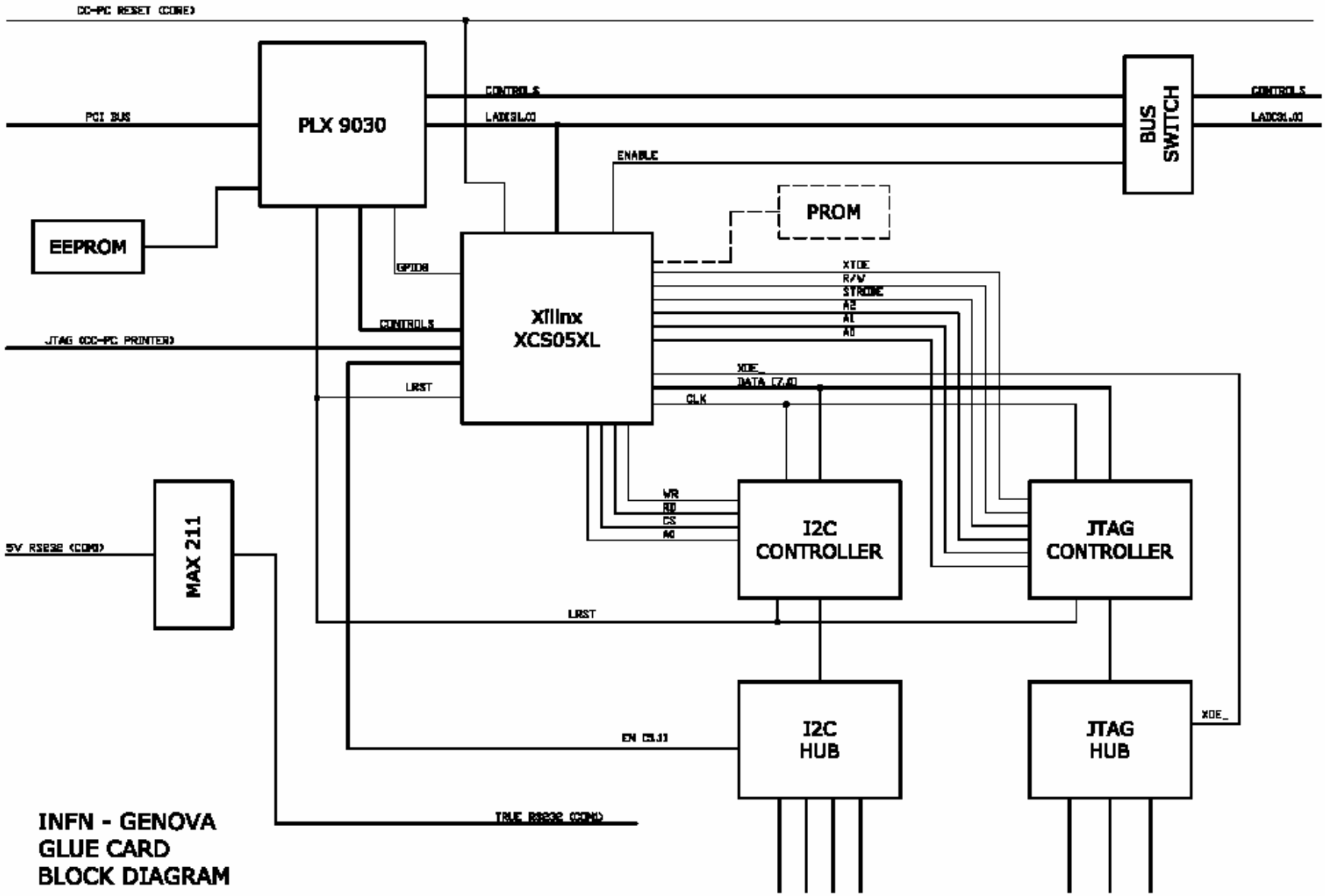
1. Each bus can be tri-stated individually setting or resetting the right bit on the enable register (9030 local bus - 1 bit, I2C hub - 4 bit, JTAG hub - 1 bit).

2. At power on all the busses are tri-stated and the computer program must enable the various busses before using them.

3. The FPGA program automatically tri-states all the busses if a hardware reset is sent to the CC-PC.

4. Before a soft re-boot of the CC-PC the user can easily tri-state all the busses by accessing the
enable register.

5. It's possible to send a reset to the glue logic through the 9030 LRESET signal (software controlled)


PCI BUS
PLX 9030
EEPROM
PROM
BUS SWITCH
Xilinx XCS05XL
I2C CONTROLLER
JTAG CONTROLLER
MAX 211
I2C HUB
JTAG HUB
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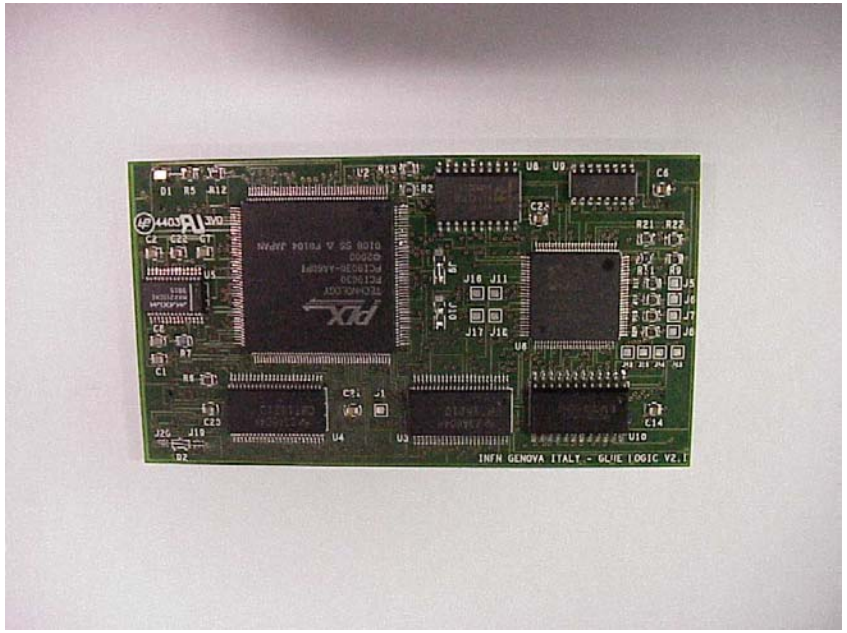
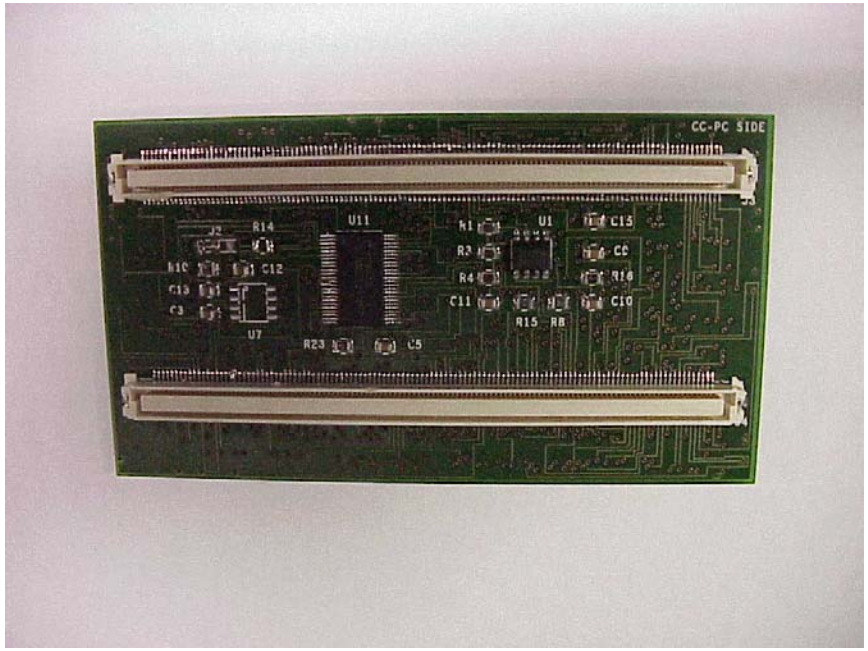
GLUE CARD
BLOCK DIAGRAM



Glue Card Components Side

Glue Card Connectors



Production

Pre-production of 20 samples being delivered in the *next days*

Production divided in *two batches*

1st batch 100 pieces

order	july	2004
ready & tested	november	2004

2nd batch 700 pieces

order	january	2005
ready & tested	july	2005