Experiment 5
MOS Device Characterization

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1.0 Objective

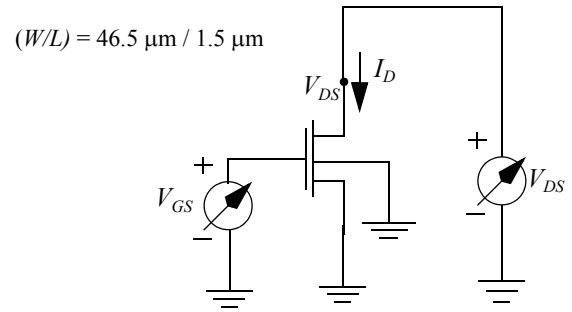
In this experiment, you will find the device parameters for an n-channel MOSFET. From the parameters, you will reproduce its *I-V* characteristics and compare them to SPICE. The characteristics will be compared to the SPICE level 1 model. We will also compare your data with data from the HP 4155 analyzer. The key concepts you should learn in this lab are:

- determining which region of operation the MOSFET is in depending on the values of V_{GS} and V_{DS},
- application of correct equations for I_D depending on the region of operation,
- extraction of basic SPICE parameters from experimental measurements

2.0 Prelab

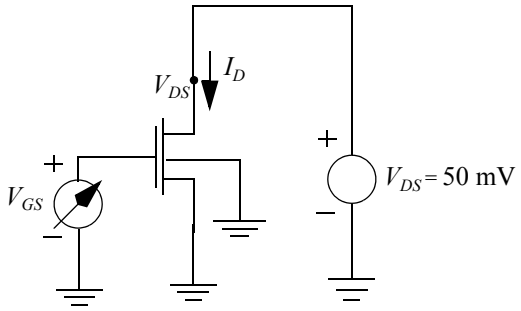
1. Review: H & S Chapter 4.1 - 4.3, 4.5-4.6.
2. Prepare a SPICE deck for the circuit in Fig. 1. Let V_{DS} range from 0 - 5 V in 0.1V increments and let V_{GS} range from 0 - 5V in 1V increments. Print a plot of I_D vs. V_{DS} with V_{GS} as a parameter. Using this plot, explain how one would obtain the parameters V_{TOn}, $K_n = \mu_n C_{ox}$ and λ_n. Use the following SPICE parameters for getting started: (note SPICE uses K_p for K_n.)
    - V_{TOn} =1 V
    - K_p=100 (μA/V^2)
    - λ_n = 0.05 V^{-1}

FIGURE 1. Circuit for SPICE simulation as described in Prelab procedure 2.



3. Prepare a SPICE deck for the circuit in Fig. 2. Print a plot of I_D vs. V_{GS}. Let V_{GS} range from 0 to 5V. Using this plot, explain how one would obtain the parameters V_{TO} and $K_n = \mu_n C_{ox}$. Use the same SPICE parameters as procedure 2.

FIGURE 2. Circuit for SPICE simulation as described in prelab procedure 3.



3.0 Procedure

1. Use the FET V_{DS}-I_D program in the 4155 to obtain the I-V characteristic for the MOS transistor; press the **CHAIN** key and select this program using softkeys.
2. Place chip Lab Chip 1 into the test fixture and connect the SMUs according to how they are configured in the **Channel Definition** screen. Pinouts for NMOS1 are as follows: (drain = PIN3 gate = PIN4 source = PIN 5). Set SMU4 to common and connect to pin 14 to provide a ground reference for the chip.

   Figure 3 shows how SMUs are connected to the pins of the chip. Figure 4 shows how the SMUs are being used in the experiment.

FIGURE 3. 4155 Test Fixture showing SMU1 being connected to pin 2 of a 28pin chip.

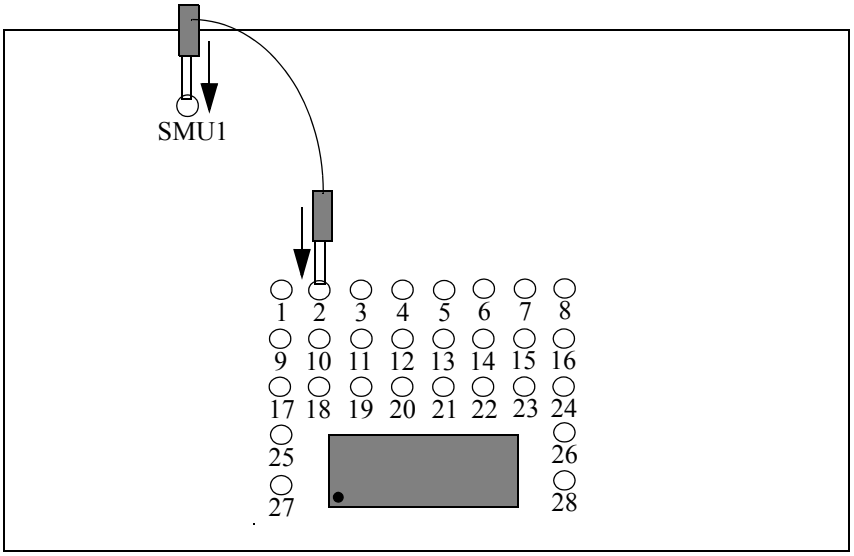
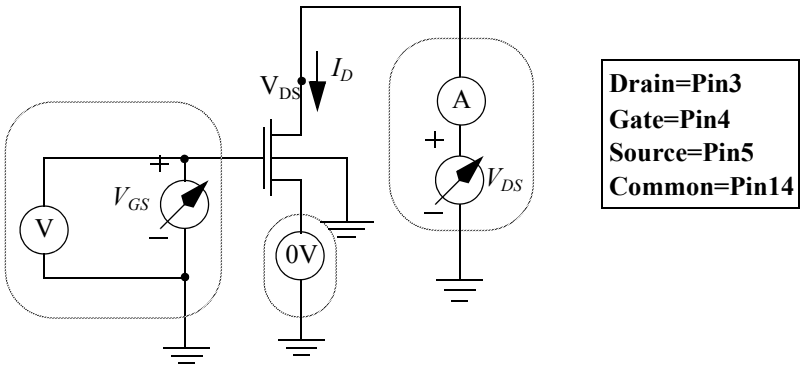


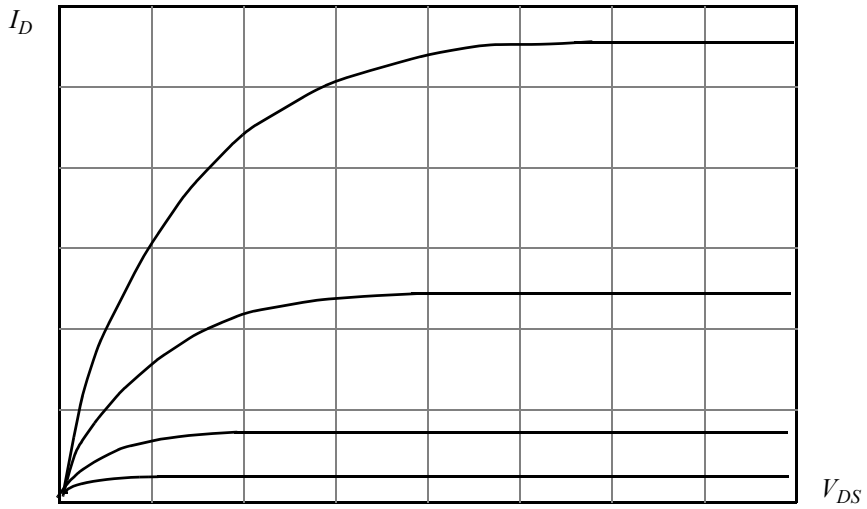
FIGURE 4. Circuit to gather data for I_D vs. V_{DS} plot. Note SMUs in dashed boxes.



3. Go to the **SOURCE SETUP** page using the **[NEXT]** or **[PREV]** key and note what voltages/currents are constant and what voltages/currents are variables. Continue to the **MEAS & DISP MODE SETUP** page and note the settings. Change the parameters to the appropriate values (i.e., step the gate voltage from 0 to 5 V and sweep V_{DS} from 0 t0 5 V).

4. Go to the **Graphics PLOT** page, hit the **[SINGLE]** key. This will perform the measurement. Hit **{AUTO SCALE}** to optimize the display of the results. The CRT should look something like figure 5.

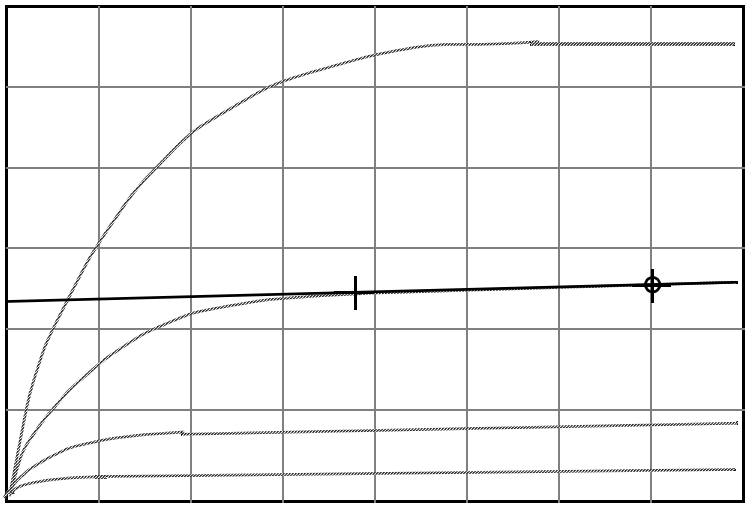
FIGURE 5. Sample I_D vs. V_{DS} characteristic of NMOS



3.1 Finding λ_n

1. Hit the **{MARKER}** softkey and you will notice a small **o**.
2. Hit the softkey **{MARKER SKIP}** twice until you reach the third curve (V_{GS}=3V). You can move the marker using the cylindrical knob. Notice that as you move the marker along the V_{DS} axis, the corresponding I_{DS} value is displayed on the CRT. Move the marker to V_{DS} = 2V. What is the region of operation of the MOSFET?
3. Fit a line between V_{DS} = 2V and V_{DS} = 4V. If you have forgotten how to fit a line, consult the instructions in Lab2.
4. Find λ_n from the slope of the line.
5. Comment on the shape of the graph. In particular, how does $V_{DS(SAT)}$ compare with theory? How does $I_{D(SAT)}$ compare with theory? Your comparisons should be quantitative.

FIGURE 6. Sample I_D vs. V_{DS} characteristic showing a best fit line to find λ_n

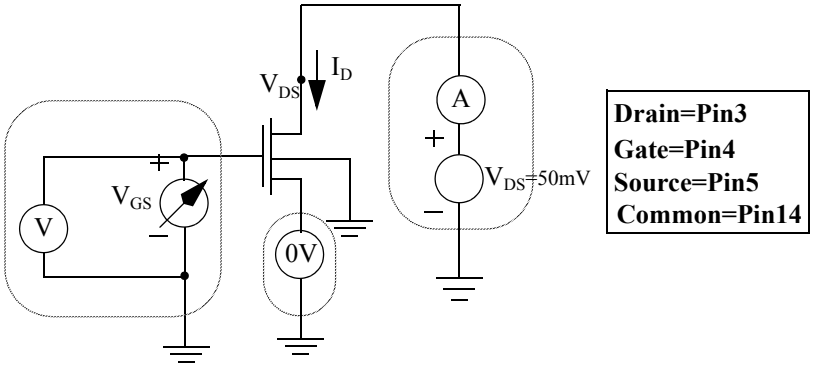


6. Obtain a plot of your data by keying in **[PLOT] [EXE]**.

3.2 Finding V_{TOn} and K_n in the Triode Region.

1. Now use the FET V_{GS}-I_D program in the 4155.
2. Connect the SMUs according to how they are configured in the **Channel Definition** screen.
3. Once again, observe the setup in the **SOURCE SETUP** page and the **MEAS & DISP MODE SETUP** page.
4. The figure below (Fig. 7) shows the functions of the SMUs. Note that the MOSFET is in the triode region for $V_{GS} > V_{TOn}$ + 50 mV; write the equation for I_D that corresponds to this region of operation.

FIGURE 7. Circuit to gather data for I_D vs. V_{GS} plot. Note SMUs in dashed boxes.



5. Toggle to the **Graphics PLOT** page and the **[SINGLE]** key to perform the measurement. Hit **{AUTO SCALE}** to rescale the curve. From your plot of I_D vs. V_{GS} in the triode region, find the best-fit line and estimate both V_{Tn} and the K_n parameter. Use the W and L values from the prelab in your calculations.
6. Obtain a plot of your data.

3.3 Finding V_{TOn} and K_n in the Saturation Region.

1. Continue to use the FET V_{GS}-I_D program.
2. Connect the SMUs according to how they are configured in the **Channel Definition** screen.
3. Once again, observe the setup in the **SOURCE SETUP** page and the **MEAS & DISP MODE SETUP** page.
4. Figure 8 shows the functions of the SMUs. Note that the MOSFET is in the saturation region for $V_{GS} < V_{TOn} + 5$ V; write the equation for I_D that corresponds to this region of operation.
5. Toggle to the **Graphics PLOT** page and the **[SINGLE]** key to perform the measurement. Hit **{AUTO SCALE}** to rescale the curve.
6. Obtain a plot of your data.
7. As you did with the I_D vs. V_{DS} plot in Section 3.2, find the best fit line for the plot of $I_D^{1/2}$ vs. V_{GS} in the saturation region, as shown in Fig. 10. Use the slope and intercept of the best-fit line to estimate both V_{Tn} and the K_n parameter.

FIGURE 8. Circuit to gather data for $(I_D)^{1/2}$ vs. V_{GS} plot. Note SMUs in dashed boxes.

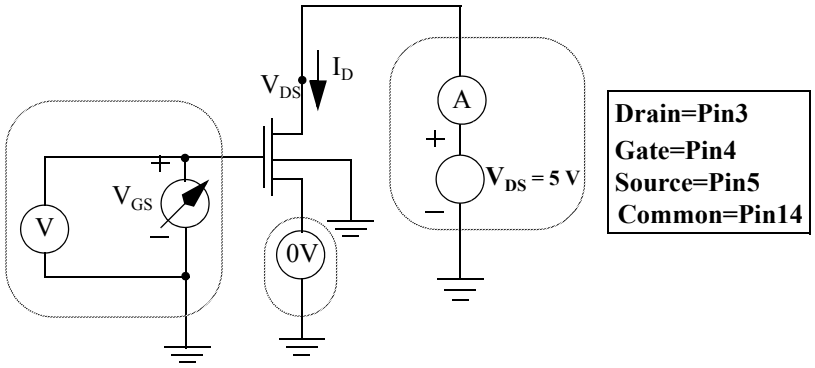


FIGURE 9. Sample I_D vs. V_{GS} characteristic of NMOS

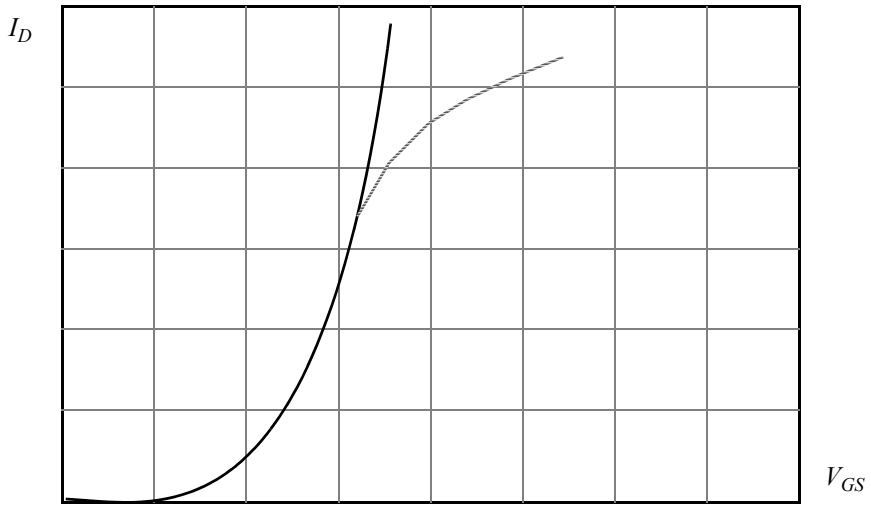
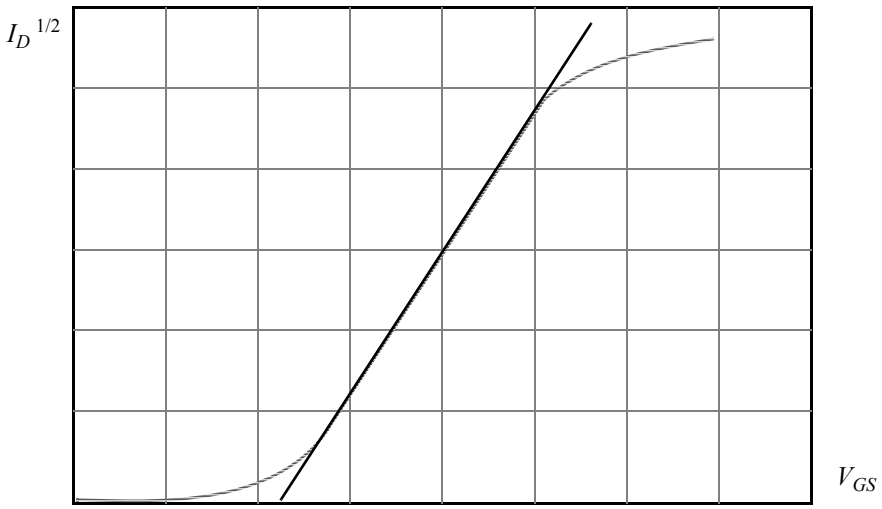


FIGURE 10. Sample $(I_D)^{1/2}$ vs. V_{GS} characteristic showing a best fit line to find V_{To} and K_n.



3.4 Comparison with SPICE

1. Fill in the value of V_{TO}, K_n, and λ_n in the data sheet in the appendix. You will need to refer to these values in future labs.
2. The values you extracted will be used in SPICE to model the NMOS. Using the SPICE decks that you have done for prelab, replace the values of $V_{To,}$ K_n, and λ_n with the ones you just found. (note that K_n is defined as K_p in SPICE)
3. Obtain plots of I_D vs. V_{DS} and I_D vs. V_{GS} as you did in prelab.
4. Compare the experimental plots with the plots you generated in SPICE. How do the values of $I_{D(SAT)}$ compare for a given $V_{DS(SAT)}$? On page 9 of the "Interlinear Becomes Chip Set for Undergraduate Laboratories in Microelectronic Devices and Circuits," two Level 1 SPICE models are given for the NMOS transistor in this technology, an "analog" model and a "digital" model. Compare plots of these models with the experimental measurements. Note that the Level 1 SPICE model is not adequate for accurate modeling of devices with channel lengths shorter than around 2 μm.

4.0 Optional Experiments

4.1 PMOS Characterization

1. Using the programs **PVT** and **PIDVD**, change the settings in the **CHANNEL DEFINITION** and **SOURCE SET UP** page to perform the experiments for the PMOS1 device on Lab Chip 2.

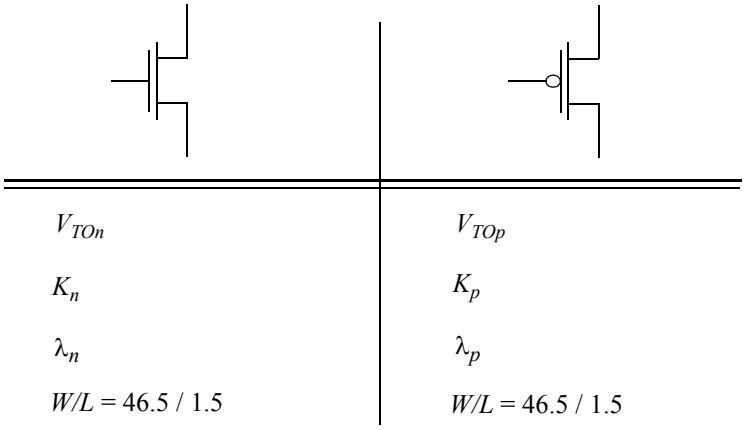
4.2 Characterization of NMOS2, NMOS3, PMOS2, and PMOS3 transistors

These devices consist of stacks of 2 (NMOS2) or 6 (NMOS3) NMOS1 transistors. The effective channel lengths are 3 μm and 9 μm, respectively. See the Appendix for the circuit schematic and layout of NMOS2 and NMOS3. Perform the same measurements on these devices. Do they better fit the simple Level 1 SPICE model?

5.0 Appendix

5.1 Data Sheet

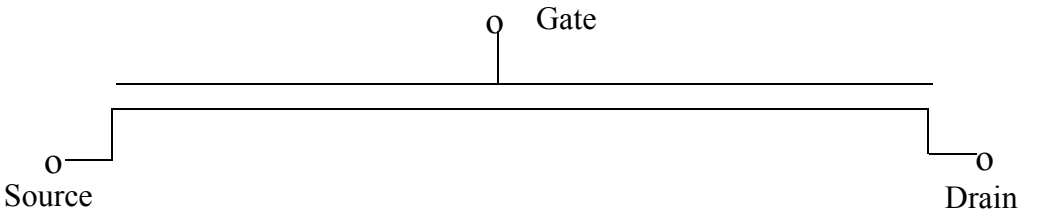
Data Sheet for NMOS1 (Lab Chip 1) and PMOS1 (Lab Chip 2)



5.2 A Note on Layout and MOSFET Geometry

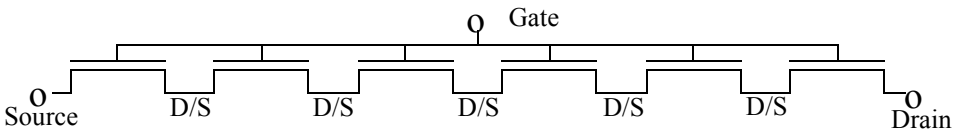
Consider the following NMOS:

FIGURE 11. Long Channel MOSFET



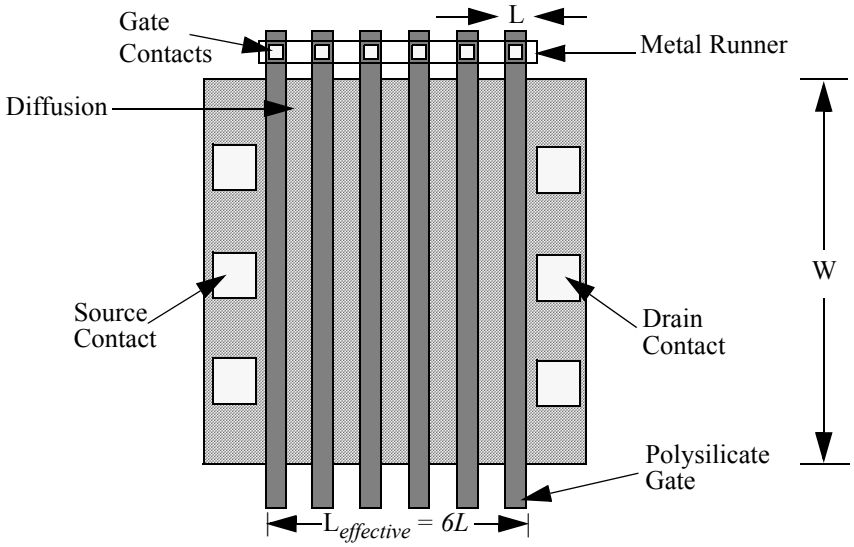
This long channel MOS transistor is the equivalent of the “stack” shown in figure 11.

FIGURE 12. Equivalent MOSFET



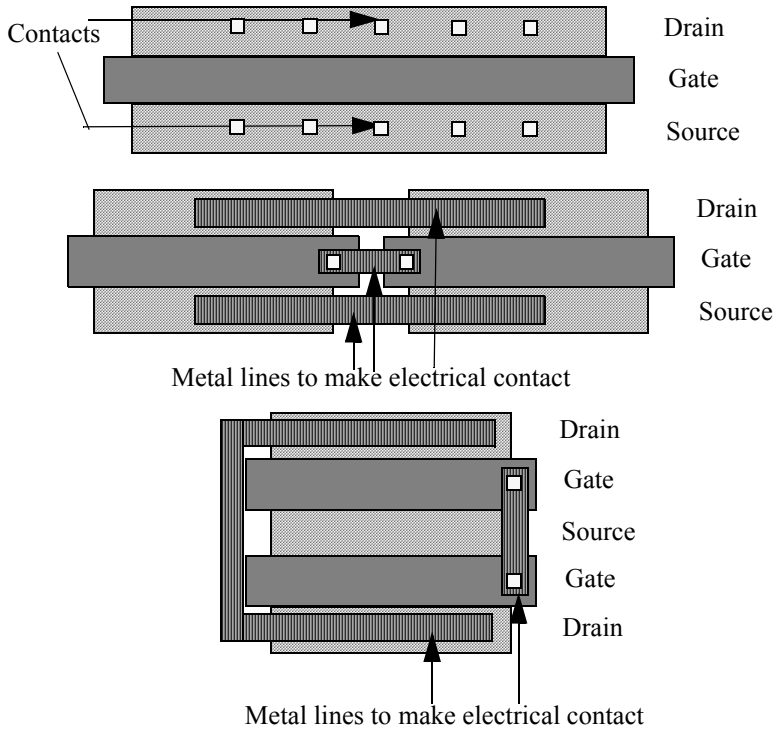
It is possible to make a “long” channel device using a series of short channel devices. The effective channel length is the sum of the channel lengths. For the tile array on which these chips were built, there were only the N3515 short channel devices. Hence, the designer chose to put the devices in series to achieve the longer gate lengths. The above MOS composite translates to the following layout design.

FIGURE 13. Layout of six transistors in series



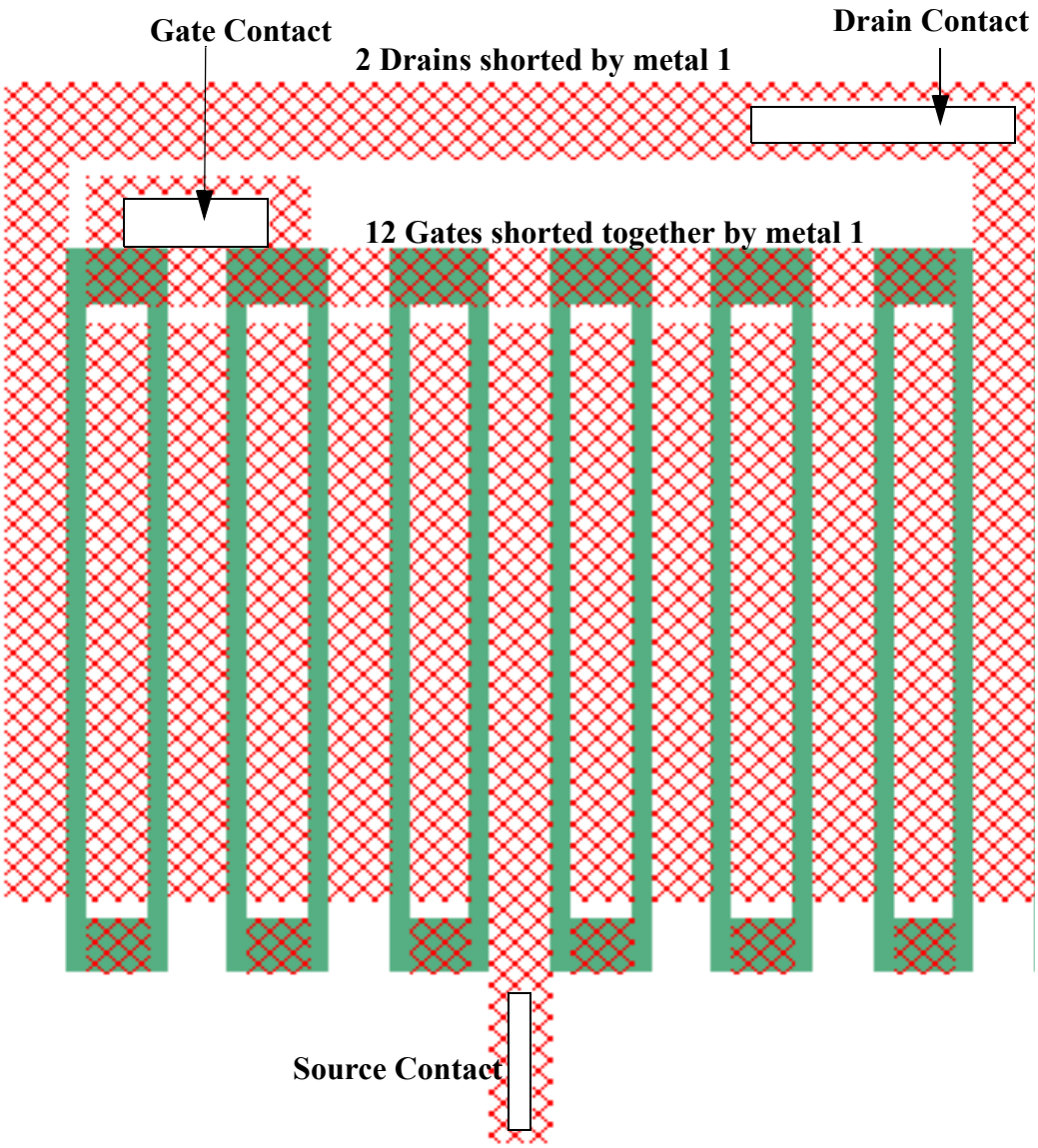
Not only can devices be hooked up in series, they can also be hooked up in parallel. We saw in the above example how the length of a device can be increased by arranging the basic transistor in series. The same can be done to the width of the device by arranging them in parallel. This is illustrated in figure 14.

FIGURE 14. The three devices below are equivalent



The following layout is one of the transistors which you will be using. Note there are 12 poly gates which are shorted together with metal 1. Note that there is one source that is shared between the two MOSFETs. So there are two MOSFETs which are in parallel. Each of the two MOSFETs in parallel is actually six MOSFETS in series. The drains of the devices are at the left and right end and are shorted together with metal 1. If the width of diffusion area is 46.5 μm and each gate has a length of 1.5 μm, what is the equivalent *W/L* ratio for the MOSFET in figure 14.

FIGURE 15. Layout of MOSFET



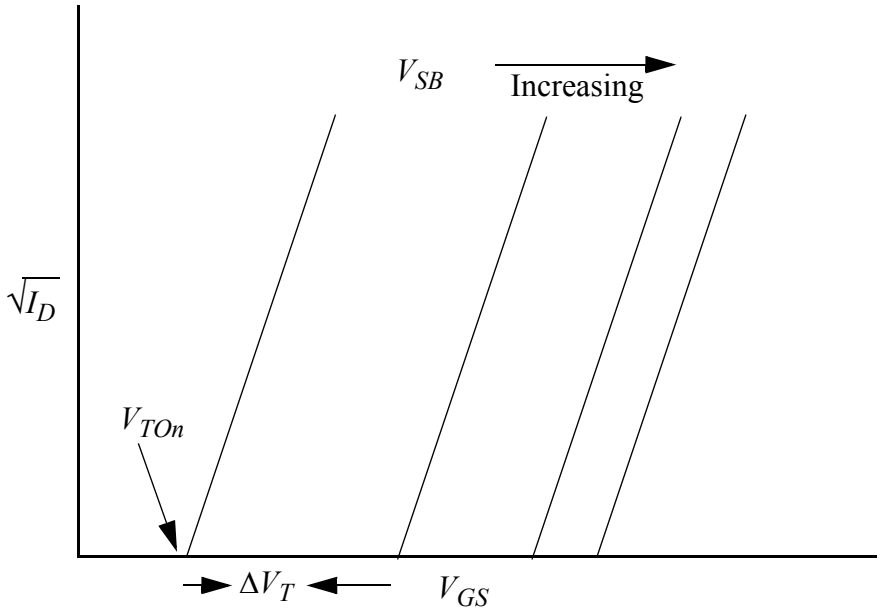
5.3 MOSFET Parameter Extraction (Saturation Region)

The equation for the drain current of an NMOS operating in the saturation region is

$$I_{D_{SAT}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} \angle V_{Tn})^2$$

If we plot the square root of $I_{D(SAT)}$ vs. $(V_{GS} - V_{Tn})$ for several values of V_{SB}, we would get a series of straight lines (Here, V_{GS} is equal to V_{DS}).

FIGURE 16. Square root of I_D vs. V_{DS} for NMOS in saturation (not assigned)



5.3.1 V_{To} Extraction

Taking the square root of the equation gives

$$\sqrt{I_{D_{SAT}}} = \sqrt{\mu_n C_{ox} \frac{W}{2L}} (V_{DS} \angle V_{Tn})$$

After normalizing the curve, the x-intercepts will find V_{Tn} for the given V_{SB}. For $V_{SB} = 0$ V, we find $V_{Tn} = V_{TOn}$.

5.3.2 γ Extraction

To find γ, we note that

$$\Delta V_{Tn} = \gamma(\sqrt{2|\phi_p| + |V_{SB}|} \angle \sqrt{2|\phi_p|})$$

By finding the appropriate value of V_{SB} and ΔV_{Tn}, we can calculate γ, since $2|\phi_p|$ ($\cong$ 0.6V) is a weak function of the doping concentration.

5.3.3 μ_n Extraction

From the square root of I_D equation, you can tell that K_n is found from the slope of the line. Since C_{ox} is specified, μ_n can be found.

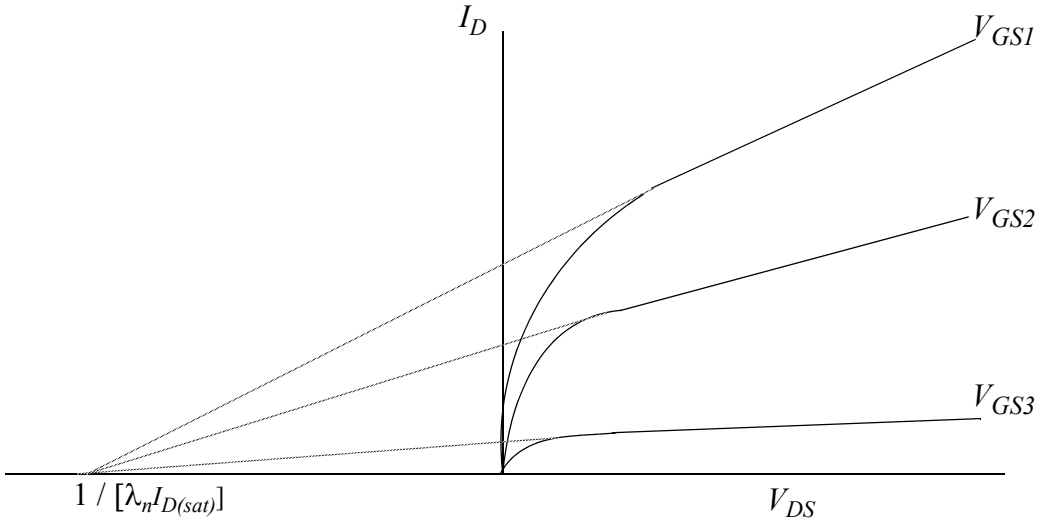
5.3.4 Channel Length Modulation

Theoretically, once the MOS enters into the saturation region, the drain current should remain constant. The theory presented so far treated the channel length L as being a constant. However, this is not so. The space charge region at the drain junction varies with the drain voltage. This makes L a function of V_{DS}. As the channel length decreases with increasing V_{DS}, the drain current increases. This is easily modeled using a parameter λ_n which is a constant linearly proportional to V_{DS}. The drain current is then modified to

$$I_{D_{SAT}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} \angle V_{Tn})^2(1 + \lambda_n V_{DS})$$

The value $1/\lambda_n$ is merely the x-intercept of the tangents to the curves of the I_D vs. V_{DS} plot.

FIGURE 17. I_D vs. V_{DS} plot for MOSFET



On the above graph, the best thing to do is to find an "average" λ_n. From the saturation region, find I_D at a given V_{DS} and another I_D at another V_{DS} (several volts further along

the graph). The inverse of the slope should be the output resistance. Remembering that $r_o = 1/(\lambda_n I_D)$, you can calculate λ using an average I_D. Take several values of λ_n for different values of V_{GS} and average them.

Note that the circuit parameters can be obtained from the MOSFET in the *linear*, or *triode* region as well.