Simulation and Characterization of SOI MOSFETs

Dual Degree Project Presentation

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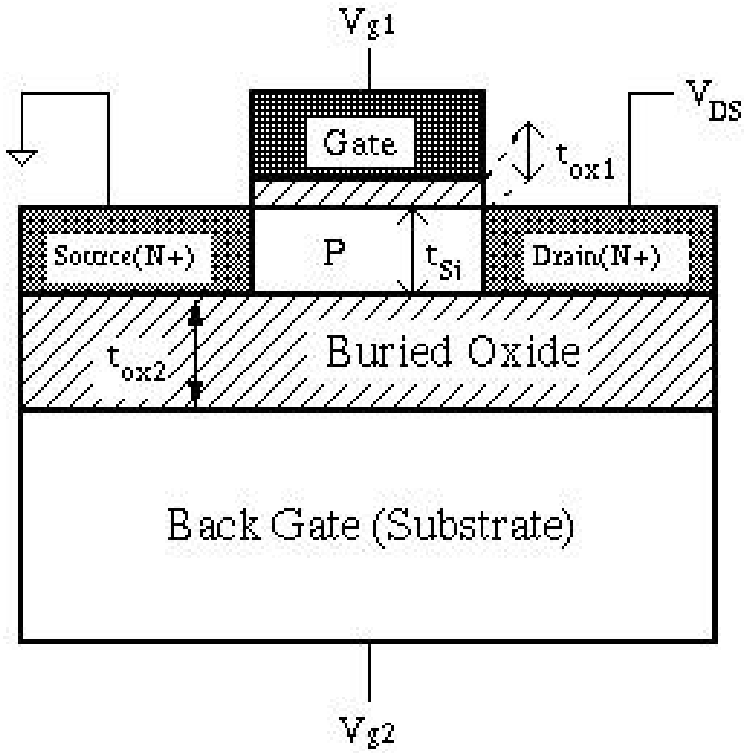
Outline of the presentation

- **Introduction to SOI Devices**
- **SOI Vs Bulk Devices**
- **Characterization and Simulation Results**
- **Gate Induced Drain Leakage (GIDL) Current Studies**
- **Multi-Frequency Transconductance Technique**
- **Conclusions**

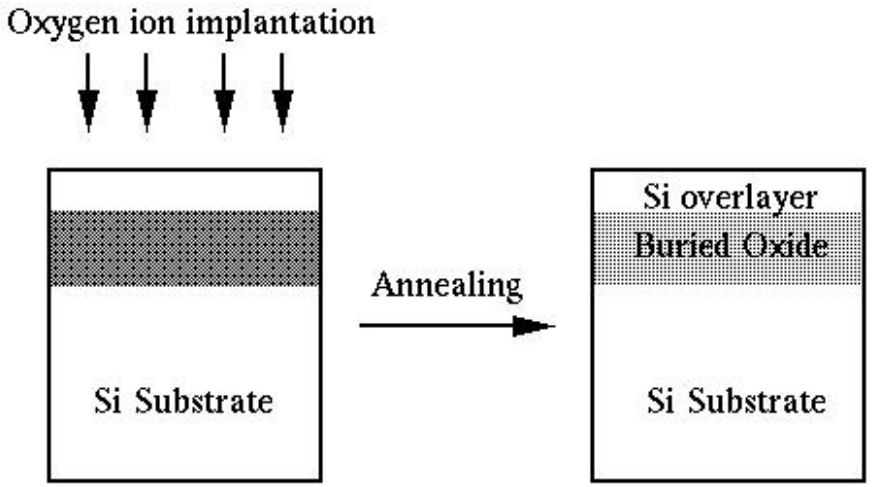
Why SOI??



An SOI nMOSFET

- Active region in bulk MOSFET is limited to top 0.1% of the device.
- Remaining 99.9% of the wafer is inactive and interaction between device and substrate gives rise to a range of parasitic effects like *latchup*.
- In SOI devices, the active device overlay is isolated from the detrimental influence of silicon substrate by a buried oxide layer, preventing the occurrence of many parasitic effects.

SOI Technology (SIMOX)



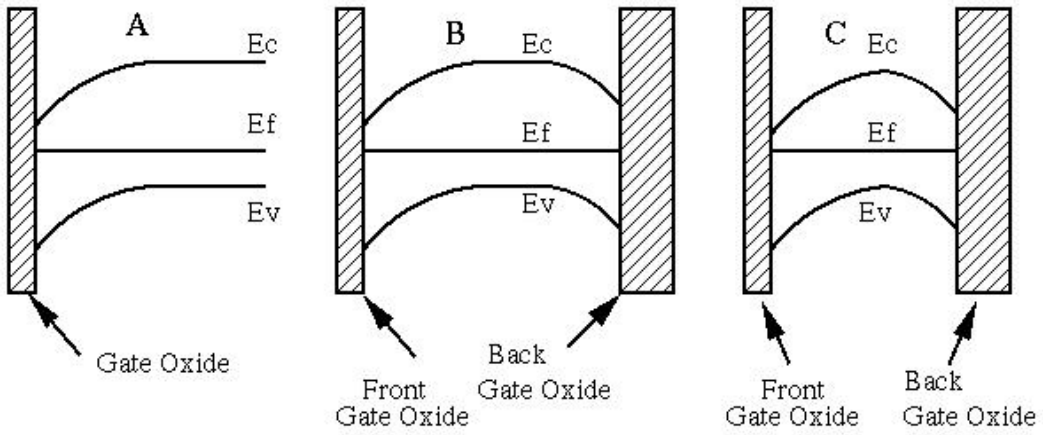
SIMOX Process

*** Acronym for "Separation by IMplantation of Oxygen " Process**

*** Most promising among SOI Technologies**

- Buried Oxide synthesized by internal oxidation during the deep implantation of oxygen ions into silicon.
- Postimplantation annealing is necessary to recover the crystalline quality of the Si overlay.
- In regular quality SIMOX wafers, the buried-oxide interfaces are found to be sharp and uniform.
- $D_{it2} \sim 0.5\text{-}2\text{x}10^{11}$ $cm^{-2}eV^{-1}$, which is more than $D_{it1} \sim 10^{10}$ $cm^{-2}eV^{-1}$, but, small enough not to adversely affect device performance.

Classification of SOI Devices



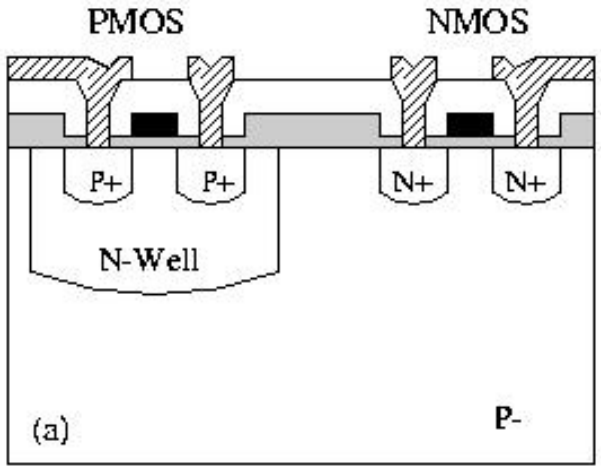
Band diagram in a
(A) Bulk device,
(B) Thick film SOI device,
(C) Thin film SOI device.

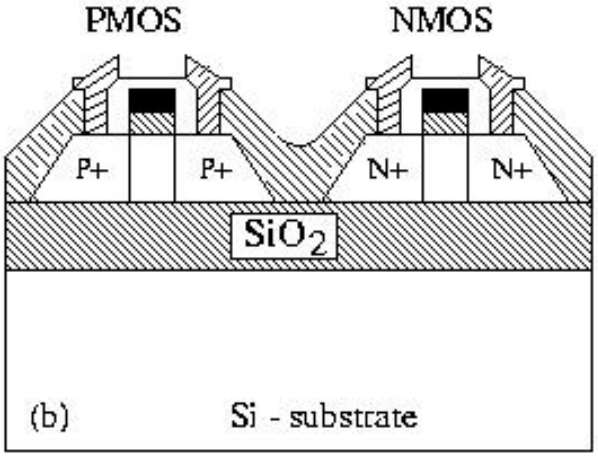
- Done on the basis of doping concentration and silicon film thickness
- Maximum depletion width

$$x_{d\max} = \sqrt{\frac{4\varepsilon_{Si}\Phi_F}{qN_A}}$$

- For thick film SOI device, $t_{Si} > x_{dmax}$
- For thin film SOI device, $t_{Si} < x_{dmax}$

SOI Vs Bulk Devices





Schematic Configuration of CMOS Transistors on bulk and SOI wafers

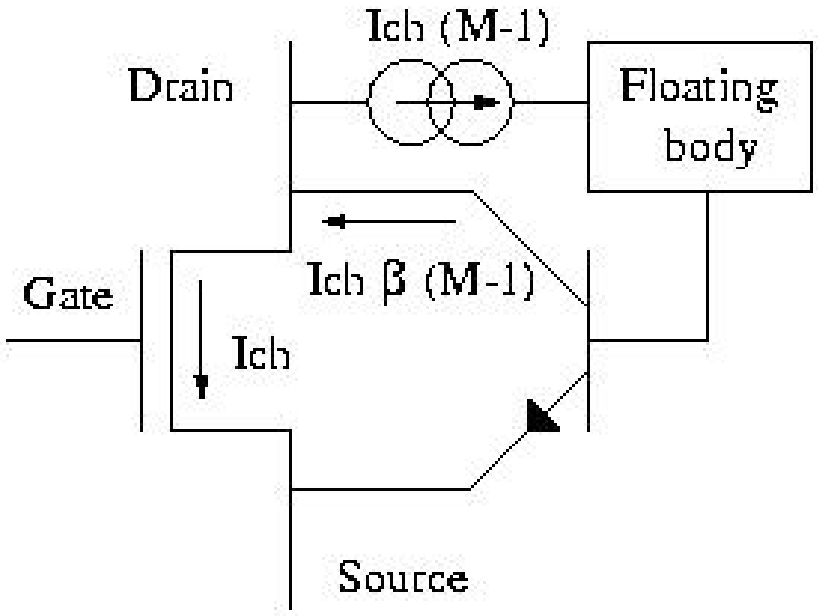
Advantages:

- ↗ Dielectric Isolation
- ↗ Vertical Junctions
- ↗ Lesser Short Channel Effects

Disadvantages:

- ↗ Self Heating Effects
- ↗ Floating Body Effects
- ↗ Parasitic Bipolar Effects

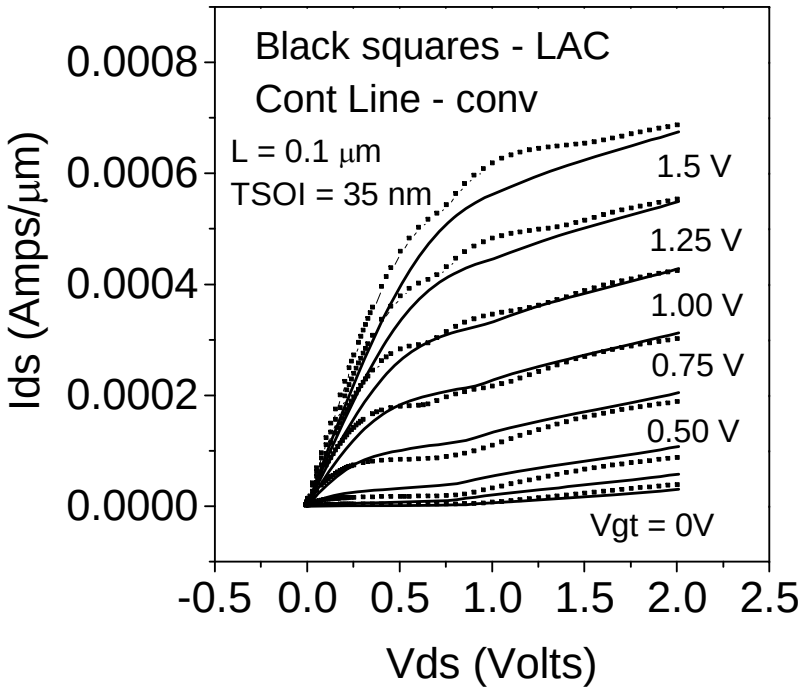
Floating Body and Parasitic Bipolar Effects



Parasitic Bipolar Transistor of SOI nMOSFET

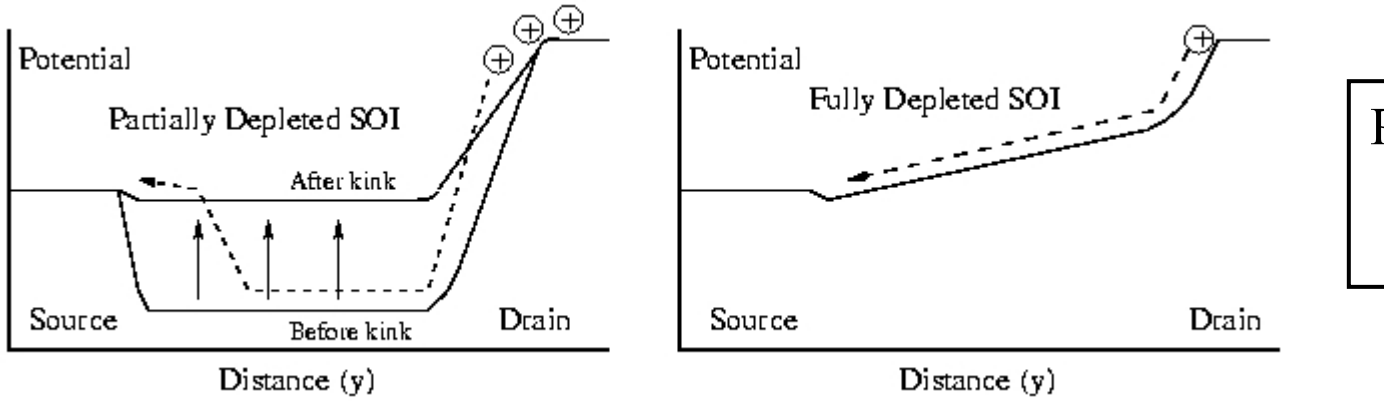
- Presence of floating volume of silicon beneath the gate gives rise to several effects unique to SOI generically referred to as *floating body effects*.
- In an n-channel transistor, n^+ source, p-type body and n^+ drain form the emitter, base and collector of an NPN bipolar transistor.
- In bulk MOSFETs, base is grounded by substrate contact. But, in SOI MOSFETs, base of the bipolar transistor is floating.
- This parasitic bipolar transistor is source of many undesirable effects.

Kink Effect



- Refers to the appearance of kink in output characteristics of an SOI MOSFET operating in strong inversion
- Kink very strong in nMOSFETs as compared to pMOSFETs
- Thin film fully depleted SOI MOSFETs don't exhibit kink effect. It's only seen for thick film partially depleted SOI MOSFETs
- Kink effect can be eliminated from partially depleted SOI MOSFETs by providing a body contact and by other channel engineering and source engineering methods

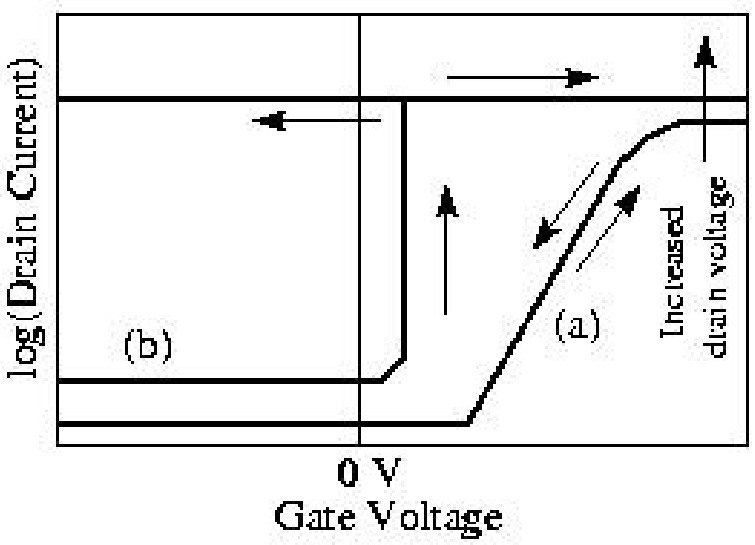
Kink Effect (contd.)



Potential in neutral region from source to drain in PD and FD SOI Devices

- At high enough drain voltage, energetic channel electrons produce electron-hole pairs by impact ionization mechanism. Electrons move into the channel and drain, whereas holes move to the place of lowest potential *i.e.* the floating body.
- Injection of holes in the floating body leads to increase in body potential, lowering source-body potential barrier and threshold voltage.
- More carriers flow from source to channel, causing a positive feedback mechanism, which leads to sudden increase in drain current causing kink in the output characteristics.

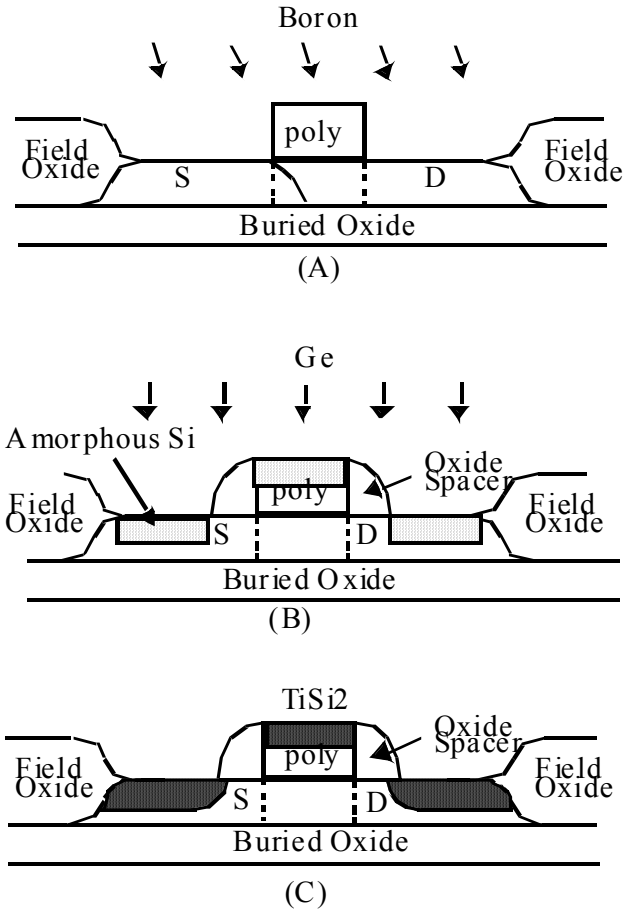
Anomalous Subthreshold Slope and Latchup



(a) "Normal" subthreshold Slope at low drain voltage,
(b) Device latch up at higher drain voltage

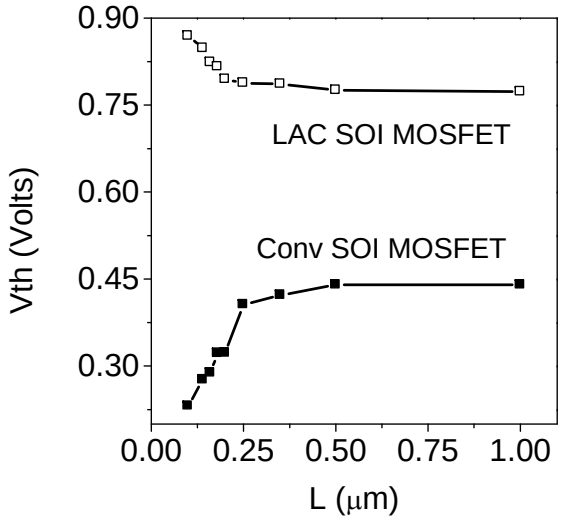
- At high enough drain voltage, impact ionization can occur even in the sub-threshold region
- When gate voltage is increased slightly, the weak inversion current can lead to impact ionization in the high electric field region near the drain.
- Threshold voltage shifts and currents can increase with gate voltage with a slope lower than 60 mV/decade.
- Parasitic BJT turns on causing sudden increase in drain current and device can't be turned off leading to latchup of the device.

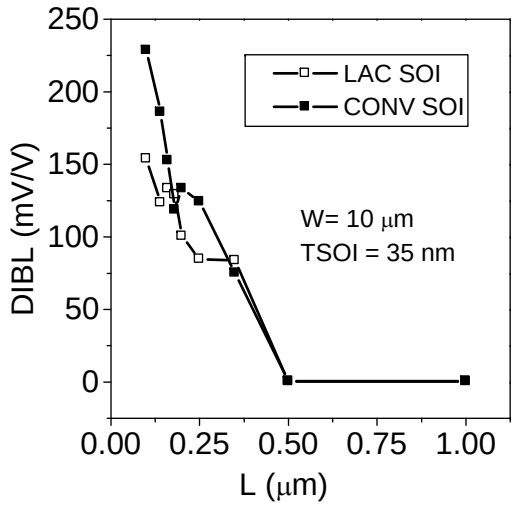
Process flow for SOI MOSFETs



- Starting Material
- SOI Wafers Si Film Thinning Down (35 nm, 50 nm, and 80 nm)
- Active Area Definition and LOCOS
- Threshold Voltage Adjustment (For Conventional MOSFET)
- Gate Oxidation (4 nm) and Poly Deposition (200 nm)
- E-beam Poly Gate Lithography and Poly Etch
- Source/Drain Extension Implant
- (A) Large Angle Tilt Implant for V_{TH} Adjustment (for LAC MOSFET)
- RTA Anneal (1020 ^{o}C, 15 seconds)
- Oxide Spacer
- (B) Ge Implantation, 12, 20, and 40 Kev, 1×10^{15} cm^{-2}
- (C) Ti Deposition (20~35 nm) Two Step RTA Silicidation
- Contact Hole
- Metallization and Forming Gas

V_{Th} Roll-off and DIBL Results



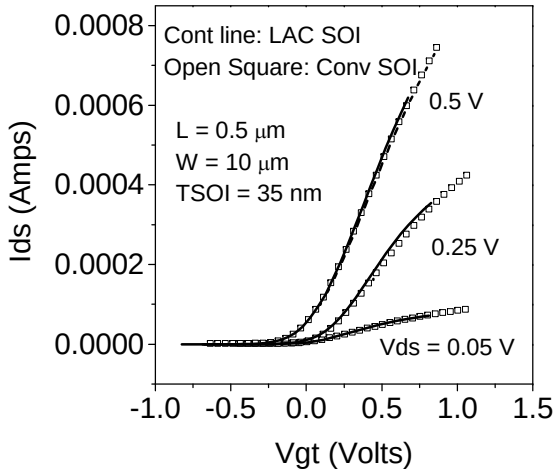


V_{Th} Roll off and DIBL for LAC and conventional SOI nMOSFETS

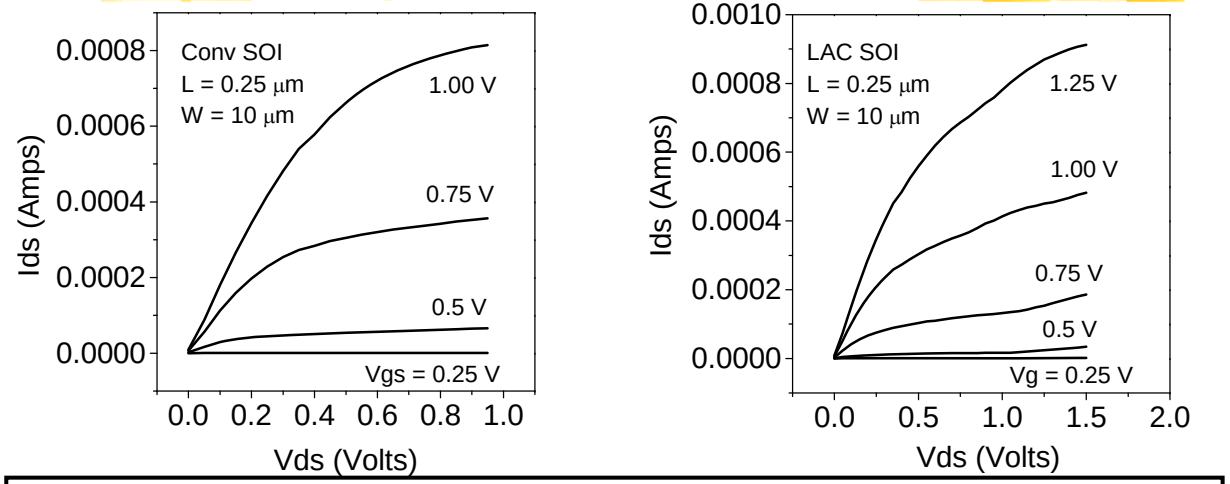
↗ V_{TH} roll off not appreciable for devices less than 0.5 μm devices. V_{TH} roll-up observed in LAC devices. Can be explained by higher effective doping in the channel for smaller channel lengths.

↗ LAC devices show lesser DIBL than conventional devices due to higher doping near the source end causing the barrier to be higher there, rendering it less prone to drain bias variations.

Transfer and Output Characteristics



Transfer Characteristics

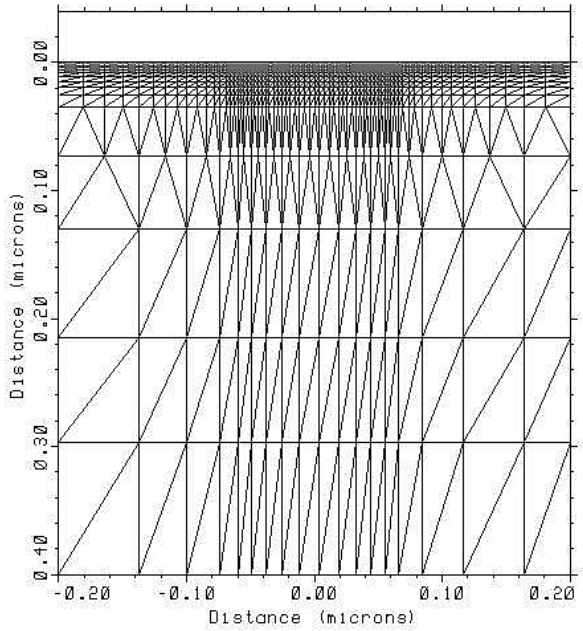


Output Characteristics of Conv and LAC SOI Devices

- LAC SOI MOSFETs show marginal increase in transconductance values as compared to conventional SOI MOSFETs. Can be attributed to reduction in scattering centers near the drain end and also due to early velocity overshoot near the source region.

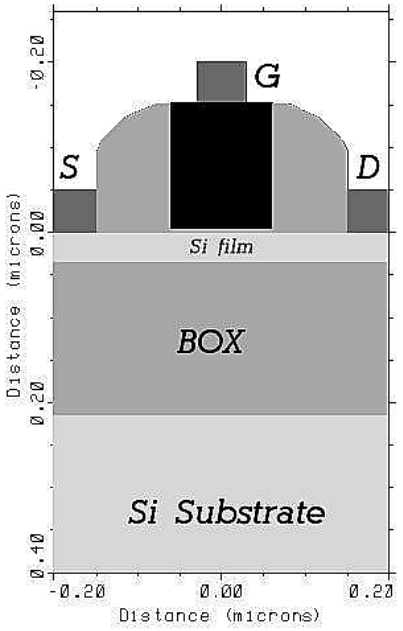
- LAC devices exhibit kink effect whereas conventional devices don't show kink, implying that LAC device is operating in partial depletion mode whereas conventional is in full depletion mode under the given biasing conditions.

Simulations Performed



Final Mesh Structure

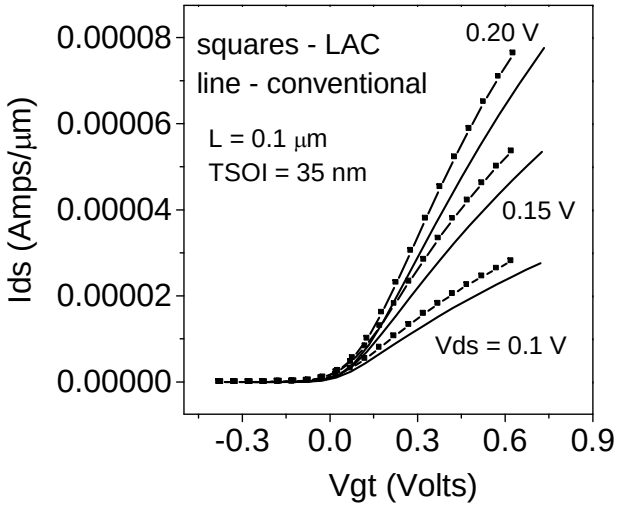
Final Device Structure



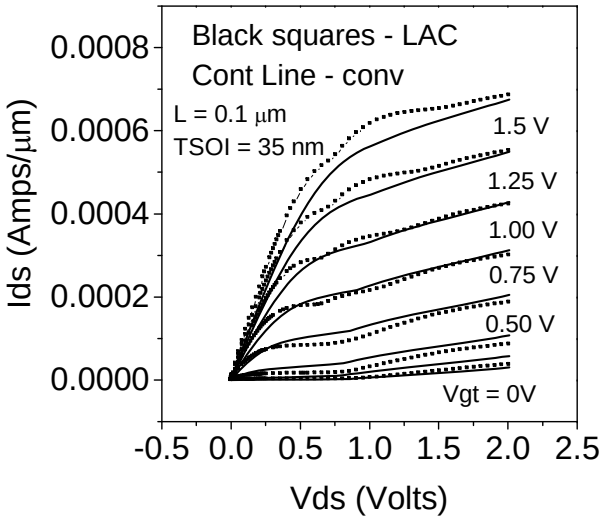
- Two dimensional process simulator, TSUPREM-4 used to simulate the devices. LAC as well as conventional devices were simulated.

- The process simulated devices were extracted into Medici, a two dimensional device simulator and characteristics were obtained under different biasing conditions.

Simulation Results



Transfer Characteristics

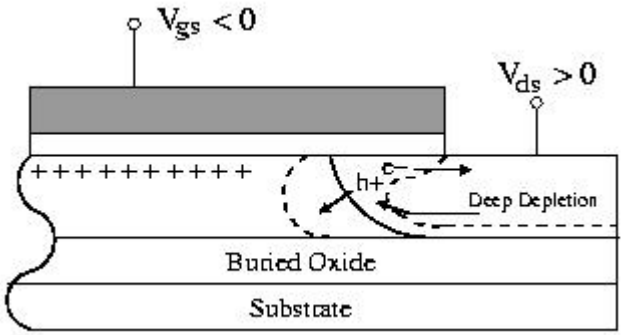


Output Characteristics

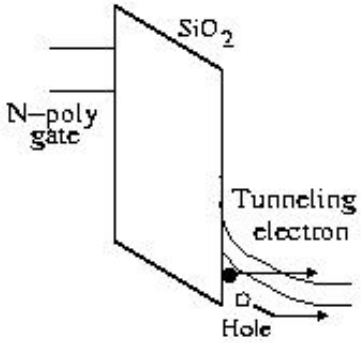
↗LAC devices show higher transconductance than conventional devices, and can be attributed to reasons as discussed previously

↗ Simulations also show kink in output characteristics for LAC devices, as obtained from experiments.

Gate Induced Drain Leakage (GIDL) Studies



Depletion Regions in the gate drain overlap region under GIDL bias



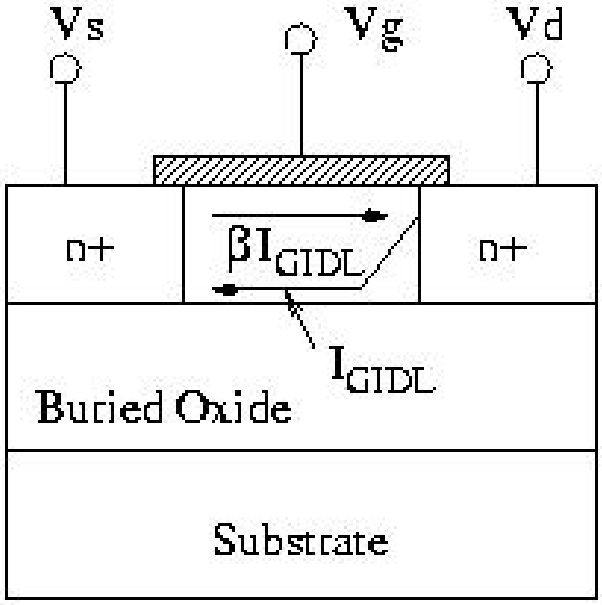
Band Diagram in the gate drain overlap region under GIDL bias

↗ GIDL current is due to tunneling current, which flows from drain to substrate, when the channel is off or in accumulation and a high drain bias is applied.

↗ The tunneling of valence band electrons into the conduction band generates electron-hole pairs due to high vertical electric field in the gate-drain overlap region.

↗ Due to vertical electric field present, the electrons and holes are collected by the drain and substrate respectively.

GIDL Currents in SOI Devices

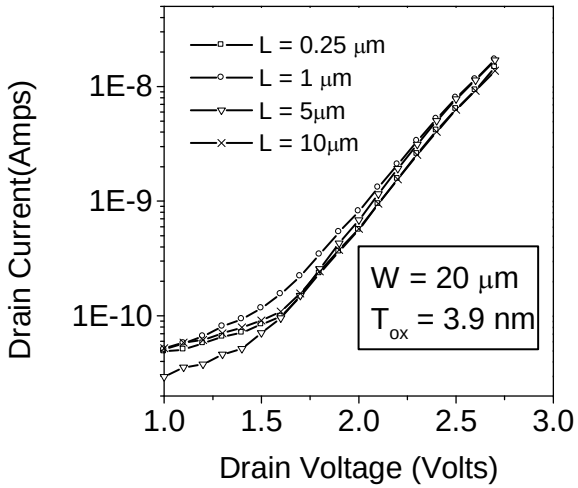


$$I_D = \beta I_{GIDL} + I_{GIDL} = (\beta + 1) I_{GIDL}$$

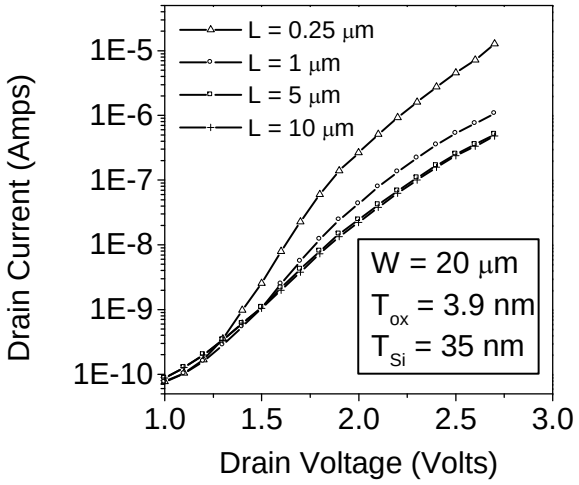
Schematic of current flow in an SOI nMOSFET under GIDL bias

- Origin of GIDL currents same as that in bulk.
- The front channel of device is kept in off state or in accumulation.
- The electrons produced are collected by the drain terminal.
- The holes, however, can't be collected by the substrate due to the buried oxide present.
- The GIDL current serves as the base current for the lateral parasitic bipolar transistor.
- The GIDL current which is independent of channel length is amplified by the parasitic BJT. This amplification is more pronounced in short channel MOSFETs.

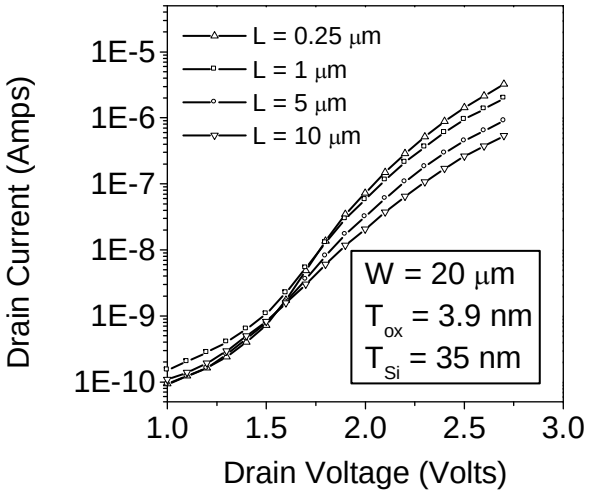
Results obtained from GIDL Studies



Bulk MOSFET



Conv SOI MOSFET



LAC SOI MOSFET

↗ GIDL currents independent of channel lengths for bulk MOSFET as band to band tunneling depends on gate drain overlap region and V_{DG} only.

↗ The base width of parasitic BJT in SOI decreases, with decrease in channel length, causing the current gain, β to increase.

Results from GIDL (cont.)

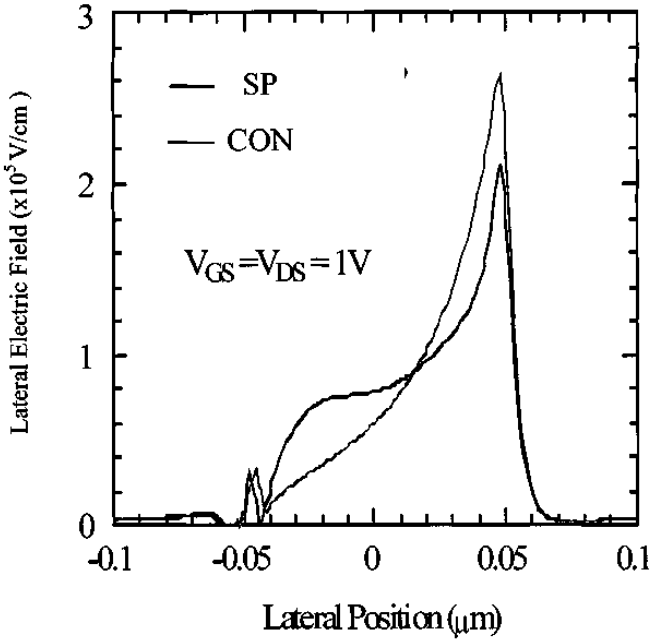
- The current gain, β is small for lower collector current levels. This explains identical currents for small drain biases.

- In conventional SOI MOSFET, GIDL current enhancement takes place for channel length of 0.25 μm for higher drain (collector) current levels. The value of β is estimated to be around 30.

- In LAC SOI MOSFET, there is no enhancement in GIDL currents showing suppression of parasitic bipolar action. The increase in GIDL currents is marginal and the value of β obtained is around 3, which is an order of magnitude lower than that for conventional SOI MOSFETs.

- Thus, LAC SOI MOSFETs show immense promise for alleviation of floating body effects, by reduction of parasitic bipolar gain, β.

Possible Reasons



Electric Field Variation for LAC and conventional SOI MOSFETs

- Lower peak electric field in LAC SOI MOSFET due to lower doping near the drain side, which leads to lower impact ionization and hence, lower hole generation.
- Wider depletion region and lower field across the junction in LAC MOSFETs lead to reduced band-to-band tunneling giving rise to a lower hole current.
- LAC SOI MOSFETs have larger effective channel length as compared to conventional SOI MOSFETs, causing the base width of parasitic BJT to be more in LAC and thus, lower current gain, β.

Interface Characterization in SOI MOSFETs

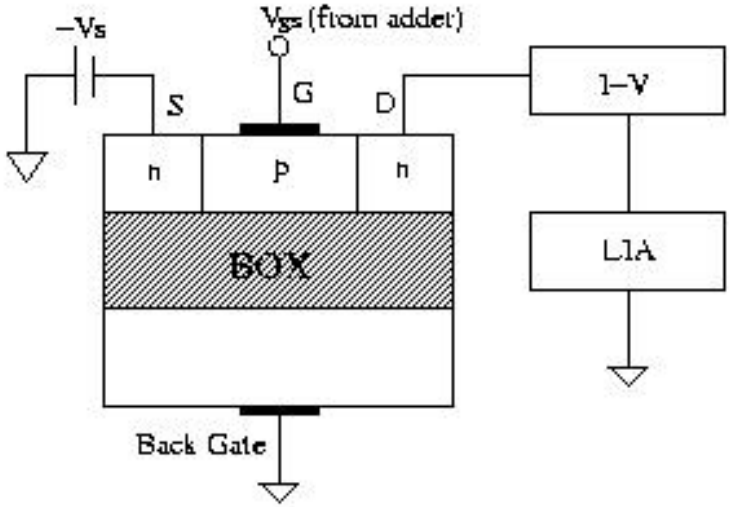
- Techniques developed for bulk-Si technology not directly applicable, due to
  - Lack of substrate contact
  - Complex multi-interface nature of SOI devices (especially effects of the back gate)

- Multi-frequency transconductance technique using a multi-frequency impedance analyzer had been used for large geometry bulk and SOI MOSFETs.

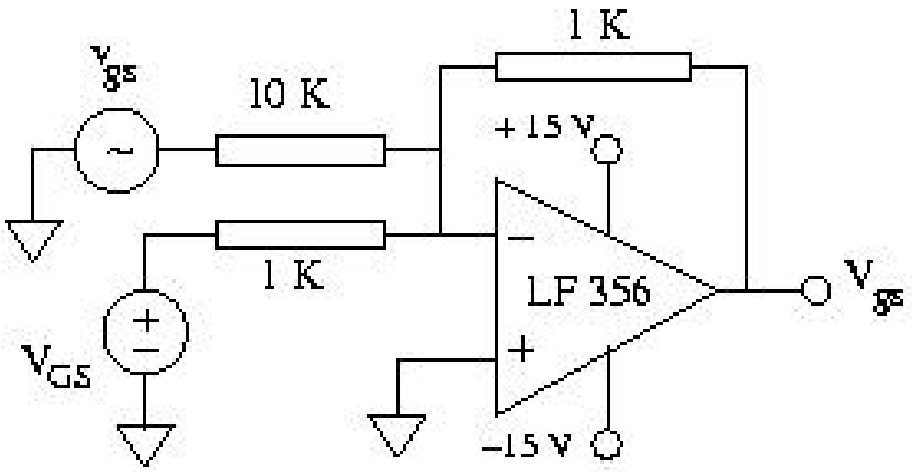
- The above technique can't be extended for small channel length devices as it is difficult to eliminate the effects of parasitics.

- A multi-frequency transconductance technique using lock-in-amplifier has been implemented for small geometry SOI devices and used to study hot-carrier degradation in JVD SOI MNSFETs.

Details of the Technique



Set up schematic



Adder used to superpose AC and DC gate signals

- Transistor biased in weak inversion
- Small signal sinusoidal gate excitation superimposed on DC gate bias
- Lock-in-amplifier measures AC component of drain current

Details of the Technique (cont..)

↗ At low frequencies, interface traps respond; whereas at high frequencies, they don't; and from these measurements interface state density can be obtained as:

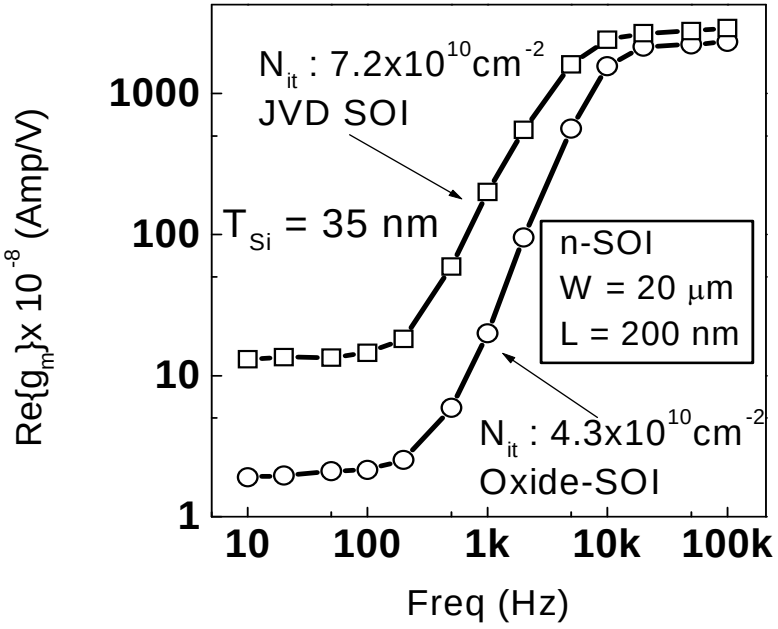
$$D_{it} = \frac{I_D C_{ox}}{kT}\left[\mathrm{Re}\left\{\frac{1}{g^m_{LF}}\right\} - \mathrm{Re}\left\{\frac{1}{g^m_{HF}}\right\}\right]$$

↗ Scanning the frequency from a suitable low value to a large value could help profile trap response distribution.

↗ This small signal measurement essentially probes average D_{it} along the channel.

↗ Method useful for characterizing high K dielectrics as gate leakage currents are high in these devices due to poor interface between the gate dielectric and silicon.

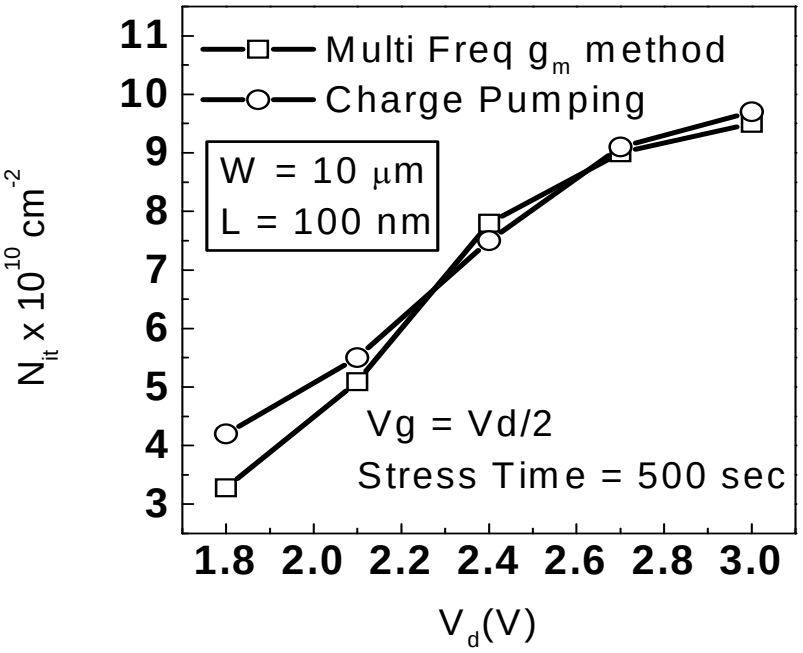
Initial Measurements

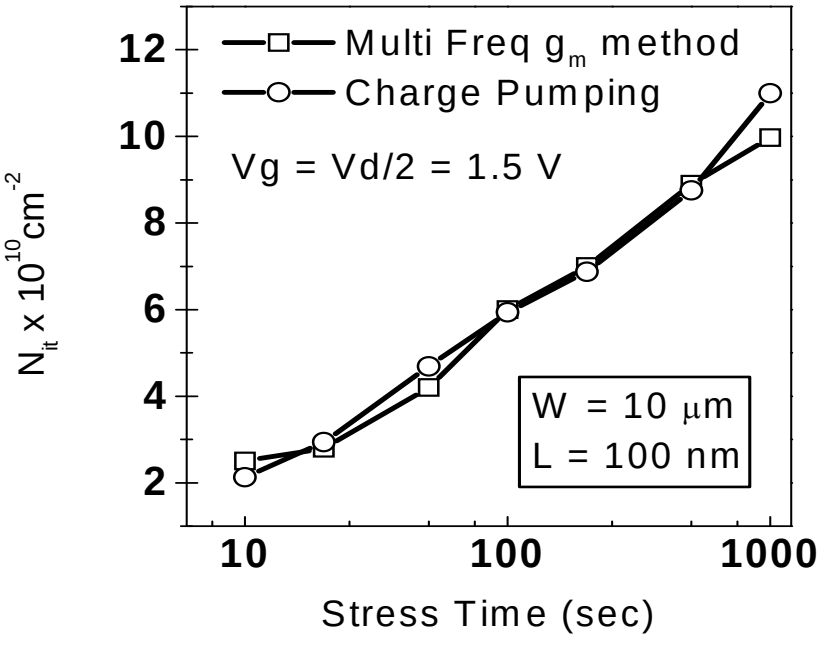


Pre-stress interface state densities obtained by multi-frequency transconductance technique on SOI MOSFETs

- Frequency of sinusoidal gate excitation swept from 10 Hz to 100 kHz
- At low frequencies, interface traps respond whereas at high frequencies, they stop following gate excitation, giving rise to the double plateau curve.
- Though Re{g_m} at lower frequencies is more for JVD SOI MNSFETs, the interface state density turns out to be more than that of conventional SOI MOSFET after taking into account the $I_D C_{ox}$ factor.

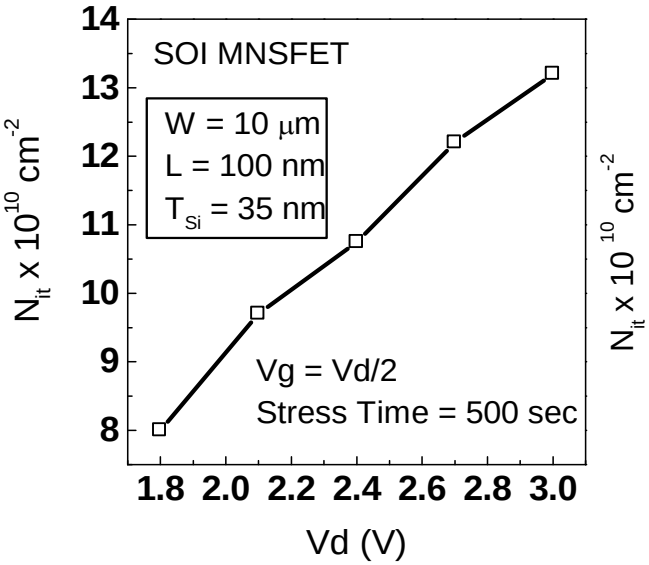
Validation of the Technique

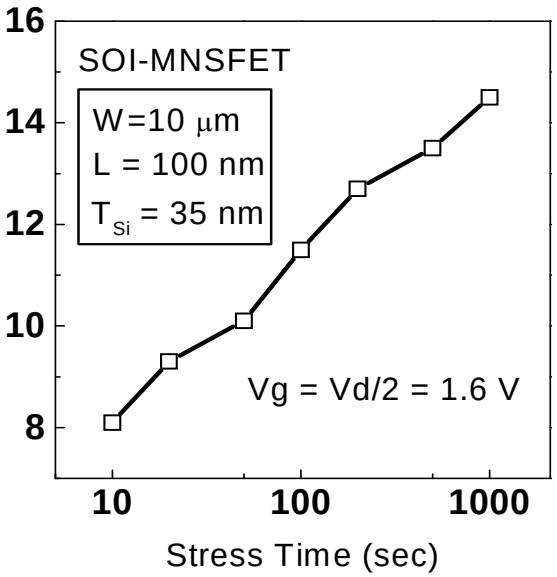


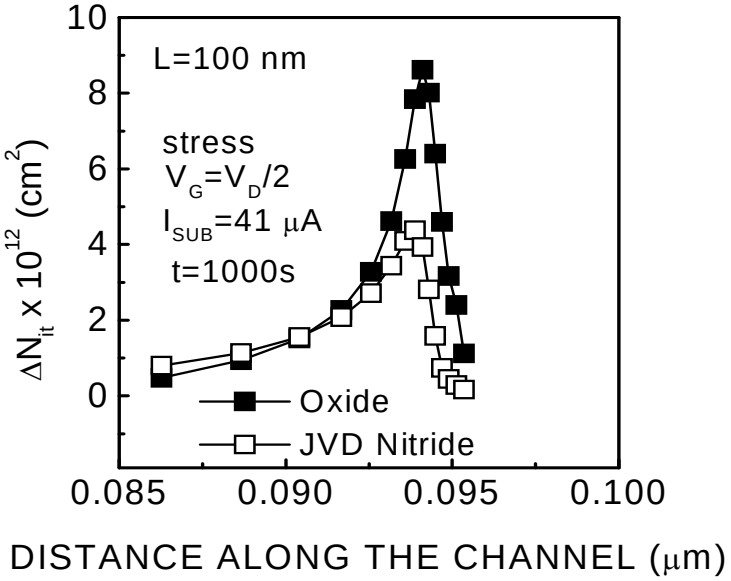


- Hot carrier experiments were performed on small geometry bulk MOSFETs and the evolution of interface state density with stress bias and stress time was measured by charge pumping and the multi-frequency technique.
- An excellent match is obtained between the two methods.

Hot carrier studies on JVD SOI MNSFETs







- In JVD SOI MNSFET, ΔN_{it} after 1000 seconds of stress is found to be 7 x 10^{10} cm^{-2}, obtained by assuming that interface states are generated uniformly in the channel.

- Interface state generation is confined to high field region, which is ~5% of channel region. Scaling up the interface state density, ΔN_{it} works out to be 1.4 x 10^{12} cm^{-2}.

Hot carrier studies on JVD (cont.)

- This is less than ΔN_{it} (~ 3 x 10^{10} cm^{-2}) obtained in identically processed bulk JVD MNSFETs, for similar stress bias conditions and time.

- The SOI JVD MNSFET is working in full depletion mode at the given biasing conditions. Therefore, lower substrate initiated carrier damage in these devices.

- Also, fully depleted SOI MOSFETs have lower electric fields in drain region as compared to identically processed partially depleted SOI or bulk devices. Therefore, less electron-hole pair generation takes place in these devices, leading to lesser hot-carrier degradation.

Conclusions

- Superiority of LAC SOI MOSFETs over conventional SOI MOSFETs established by means of experiments and simulations.
- Gate Induced Drain Leakage (GIDL) current studies show that LAC structure alleviates the floating body effects by suppressing the current gain of parasitic bipolar transistor.
- Multi-frequency transconductance technique used to study hot-carrier degradation effects in JVD SOI MNSFETs. Degradation found to be less severe than identically processed bulk MNSFETs due to lower peak electric fields in FD device as well as absence of substrate initiated hot carrier degradation.