EE410 vs. Advanced CMOS Structures

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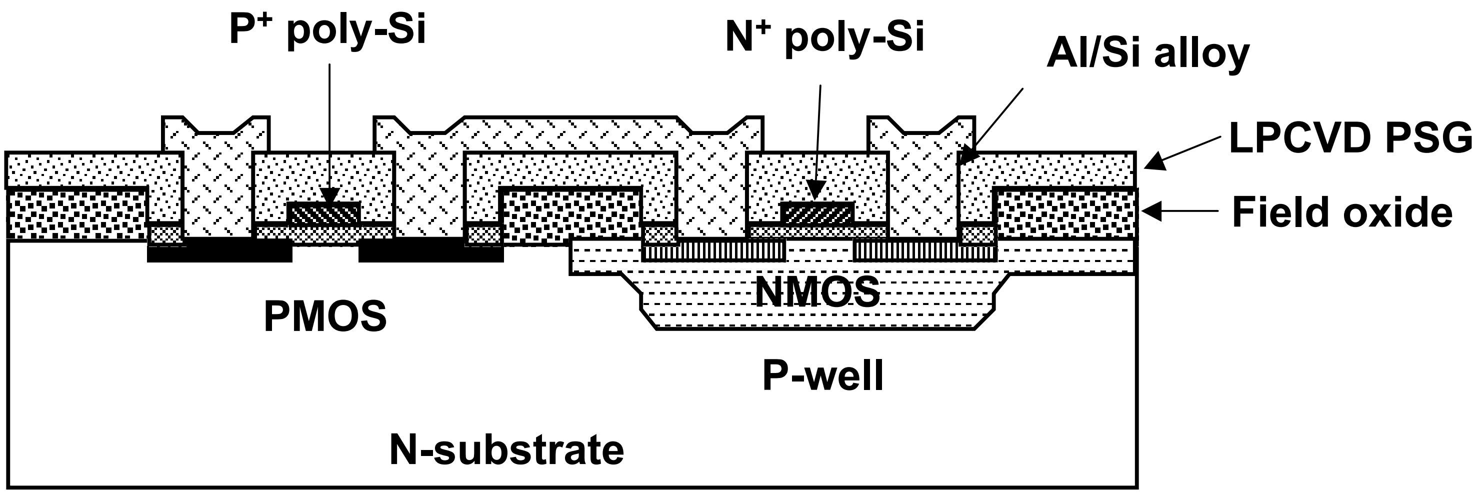
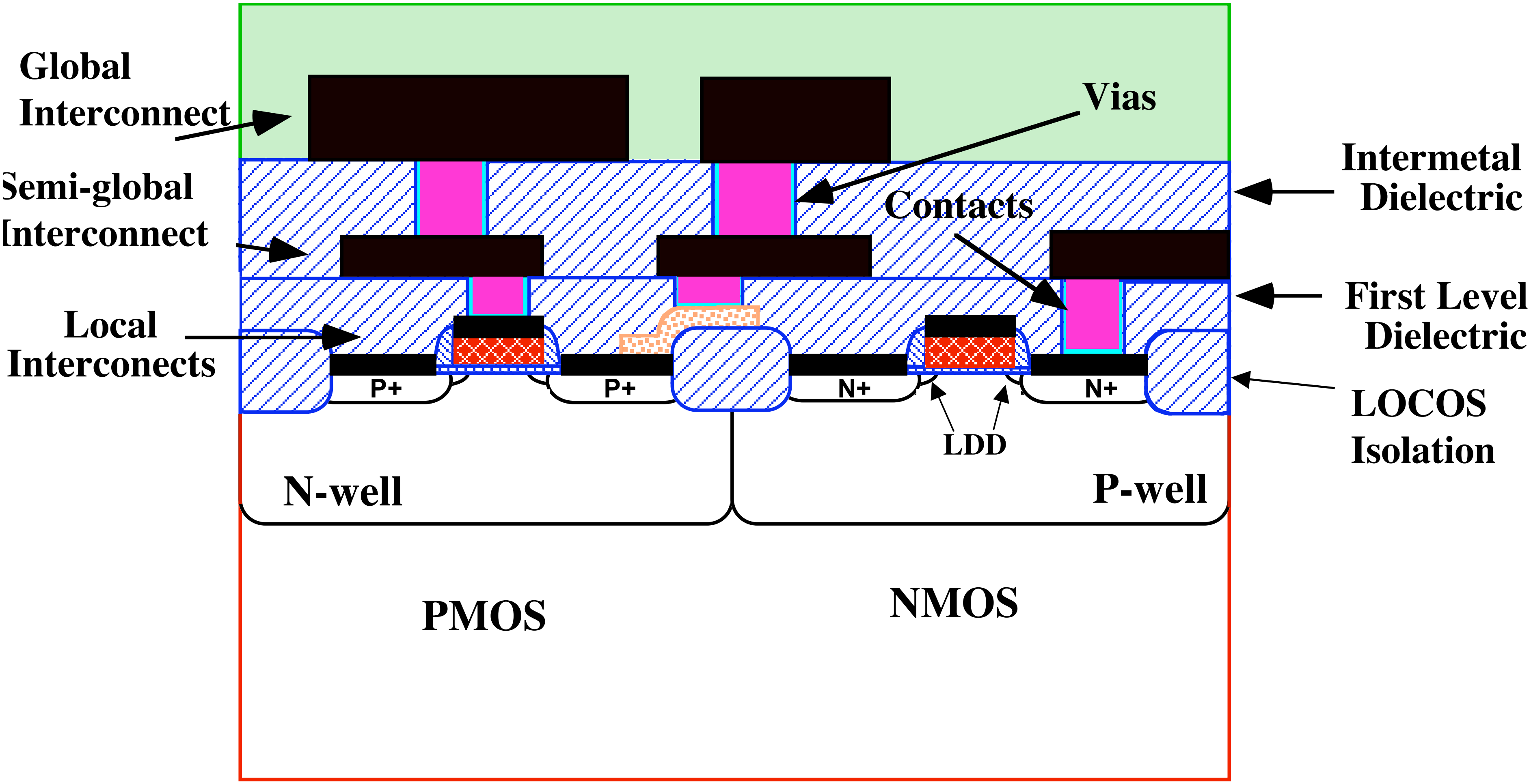
EE410 CMOS Structure



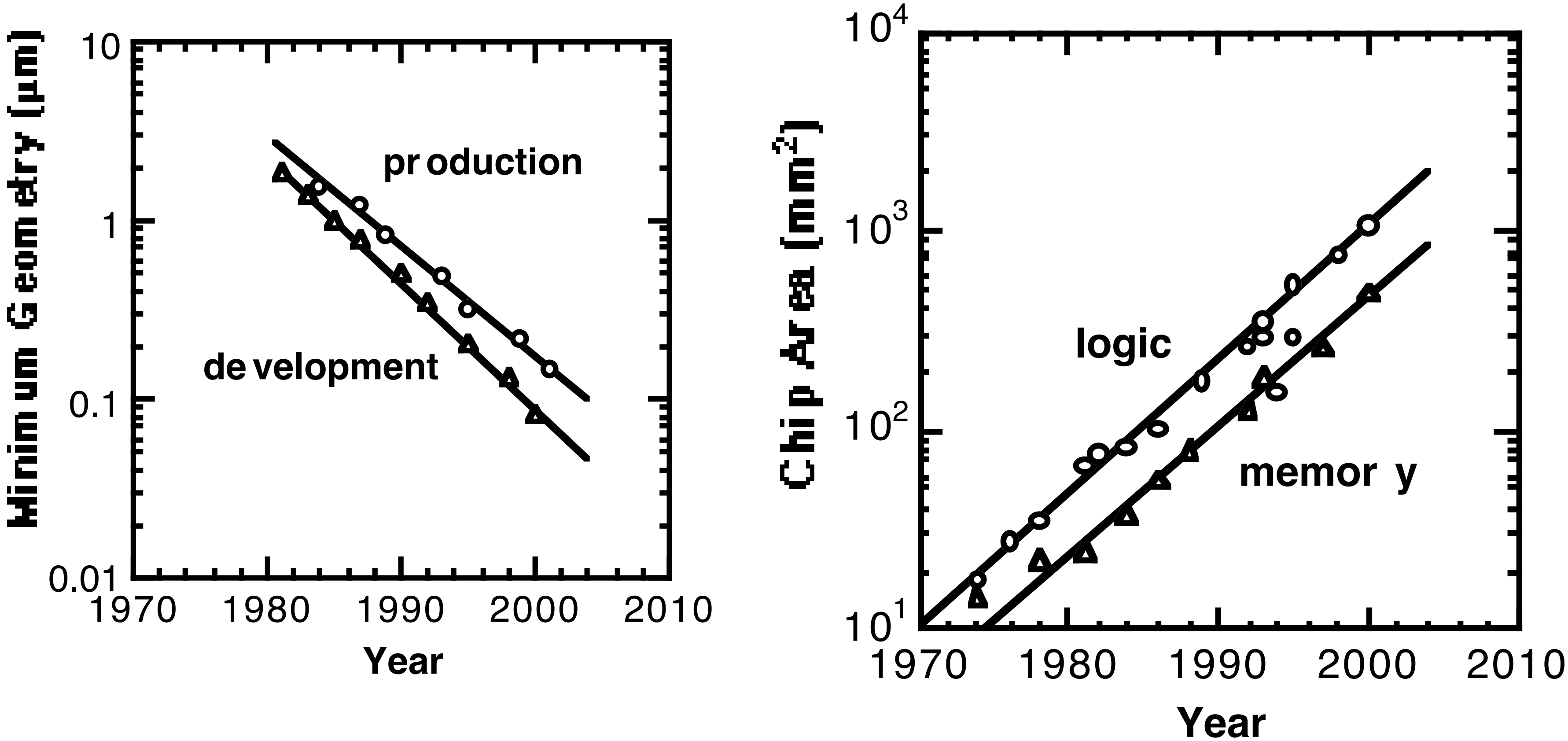
<u>General Features of the EE410 Process</u>

- 6 mask levels (7 including optional pad mask level)
- 1.5µm minimum dimensions
- 500nm field oxide (non-LOCOS isolation)
- 40nm gate oxide
- p+ poly-Si gate for PMOS transistors and n+ poly-Si for NMOS transistors
- single mask n^+ and p^+ source/drain definition (no LDD)
- single level of aluminum/silicon metallization
- phosphosilicate glass (PSG) passivation
- non-silicided contacts (high metal contact resistance to poly and active regions)

Dual Well CMOS Technology



Scaling of Minimum Feature size and Chip Area

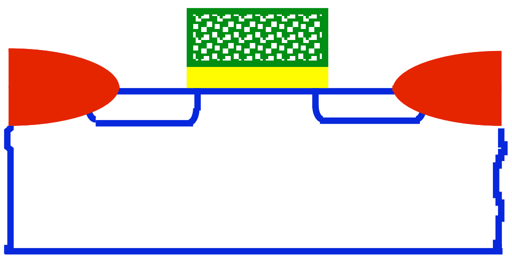


Ref. A. Loke, PhD Thesis, Stanford Univ. 1999

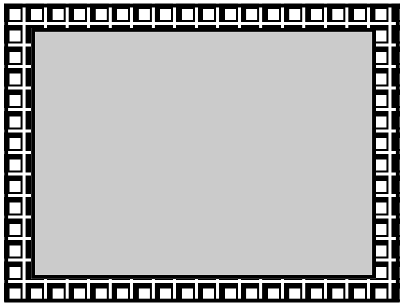
MOS Scaling Requirements from the ITRS roadmap

Year of 1st DRAM Shipment	1997	1999	2003	2006	2009	2012
Min Feature Size	0.25µ	0.18µ	0.13µ	0.10µ	0.07µ	0.05µ
DRAM Bits/Chip	256M	1G	4G	16G	64G	256G
Minimum Supply Voltage (volts)	1.8-2.5	1.5-1.8	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6
Gate Oxide T_{ox} Equivalent (nm)	4-5	3-4	2-3	1.5-2	<1.5	<1.0
Contact x_j (nm)	100-200	70-140	50-100	40-80	15-30	10-20
x_j at Channel (nm)	50-100	36-72	26-52	20-40	15-30	10-20
# of Wiring Levels	6	6-7	7	7-8	8-9	9
Intermetal Insulator Dielectric Constant	3.0-4.1	2.5-3.0	1.5-2.0	1.5-2.0	<1.5	<1.5

MOS Technology in 2010



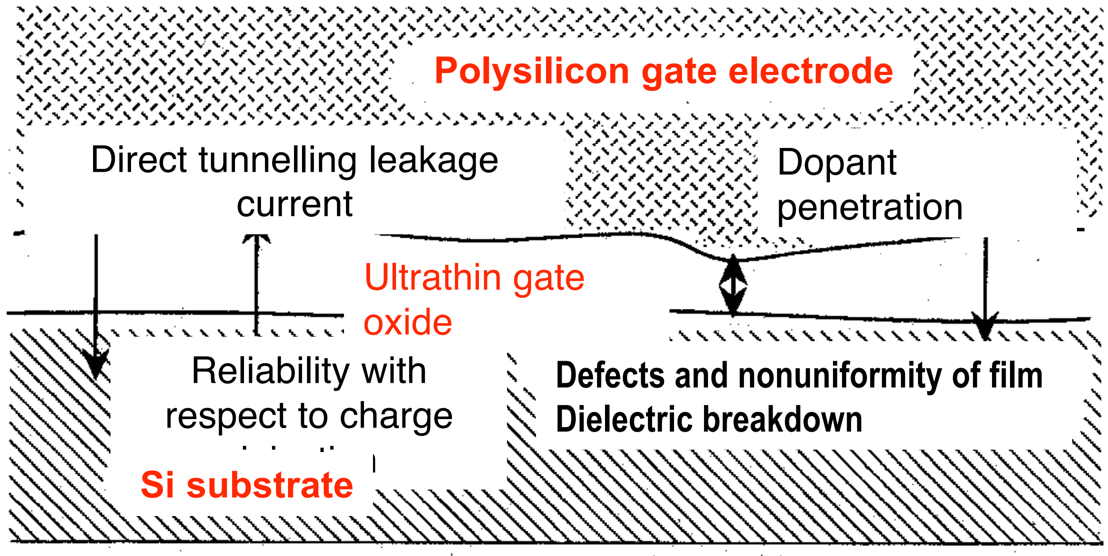
Gate oxide thickness < 10 Å
Channel Length ~ 500 Å
Junction depth ~ 150 Å
Size of an atom ~ 3 - 5Å



In integrated system
10 billion components
10 interconnect layers

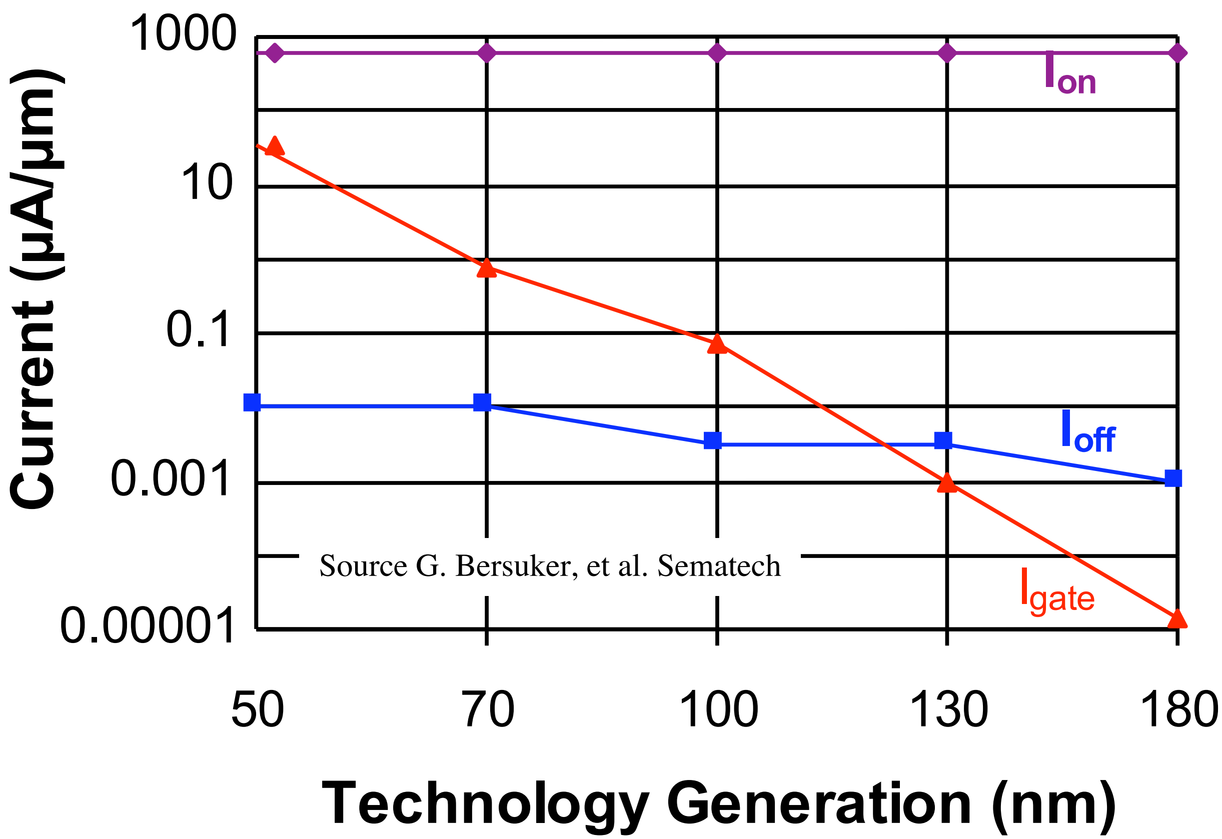
<u>Technological Issues</u>
Gate dielectrics/electrode
Shallow junctions
Isolation
Contacts
Interconnections

Problems in Scaling of Gate Oxide



- Below 20 Å problems with SiO_2
  - Gate leakage => circuit instability, power dissipation
  - Degradation and breakdown
  - Dopant penetration through gate oxide
  - Defects

Gate Oxide Scaling Issues: Leakage

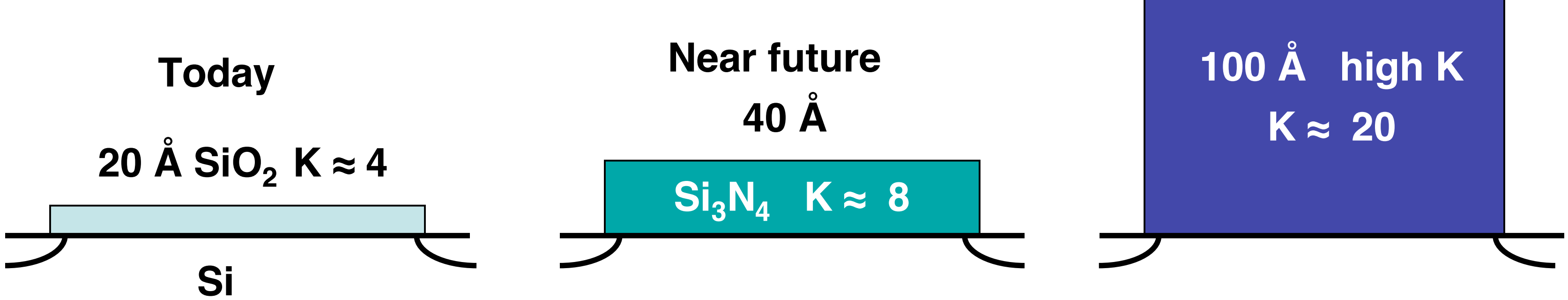


- **Circuit instability**
- **Power dissipation**

High-k Dielectric Technology Evolution

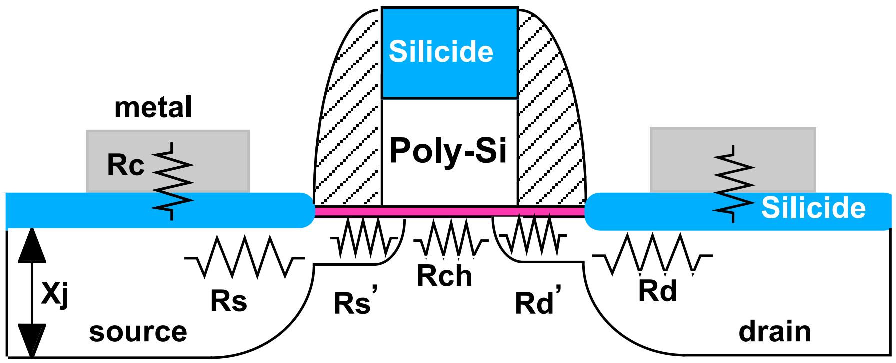
Physical thickness can be increased for MOS gate dielectric operation by using a higher K dielectric

$$I_D \quad g_m \quad \frac{K}{thickness}$$



Higher thickness -> reduced gate leakage

Effect of Scaling of Contacts and Junctions



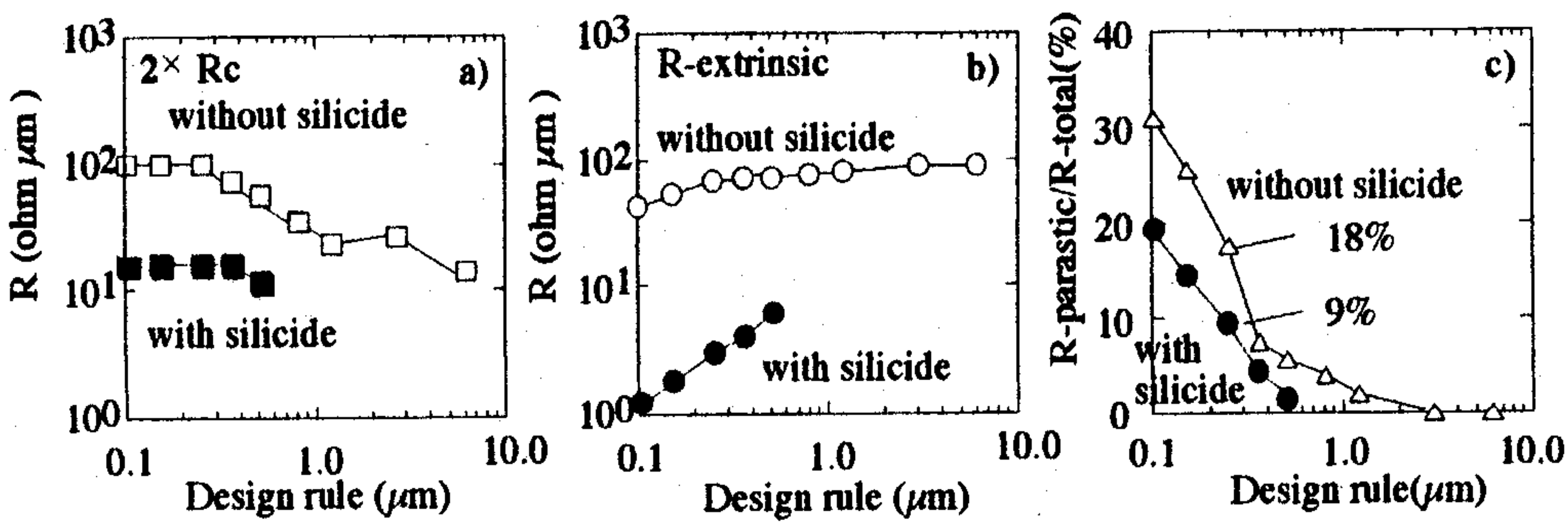
R (total) = Rch + Rparasitic

Rparasitic = Rextension + Rextrinsic

Rextension = Rd' + Rs'

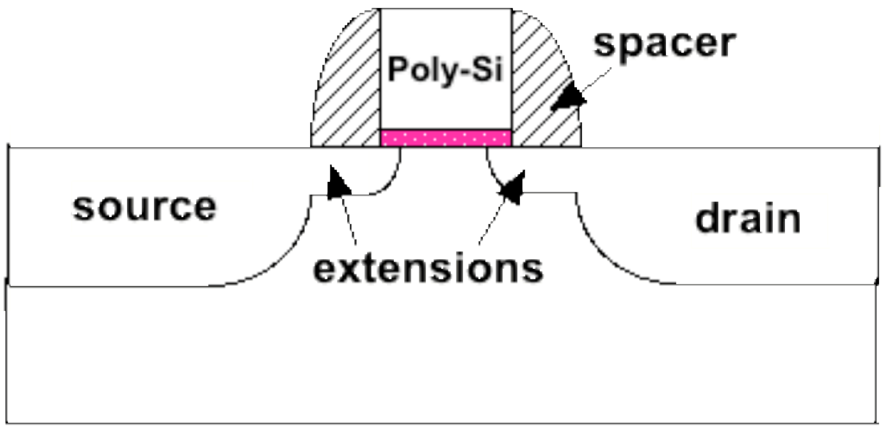
Rextrinsic = Rd + Rs + 2Rc

Ref: Ohguro, et al., ULSI Science and Technology 1997, Electrochemical Soc. Proc., Vol. 97-3

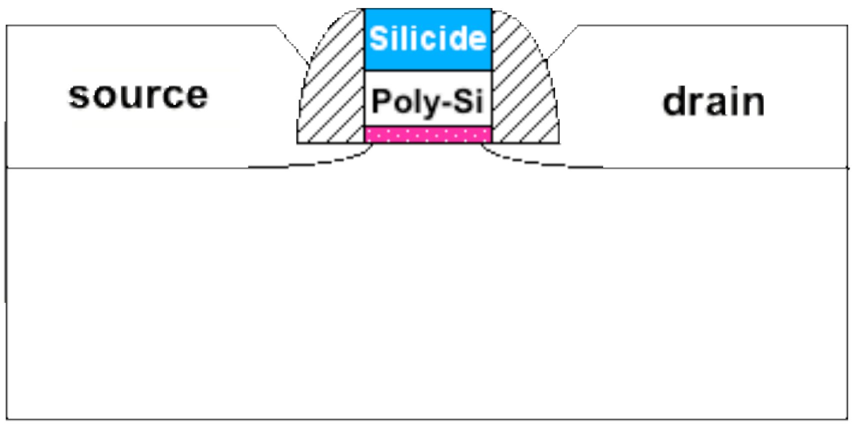


Silicidation of junctions is necessary to minimize the impact of junction parasitic resistance

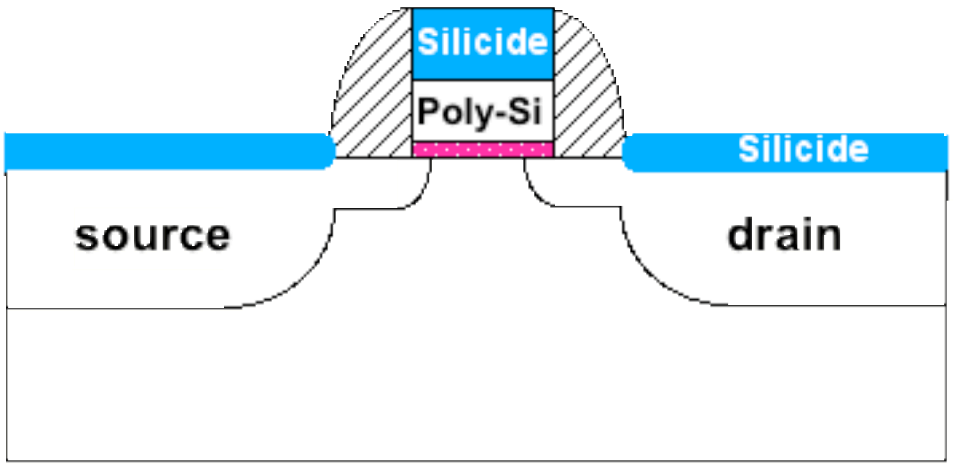
Solutions to Shallow Junction Resistance Problem



Extension implants

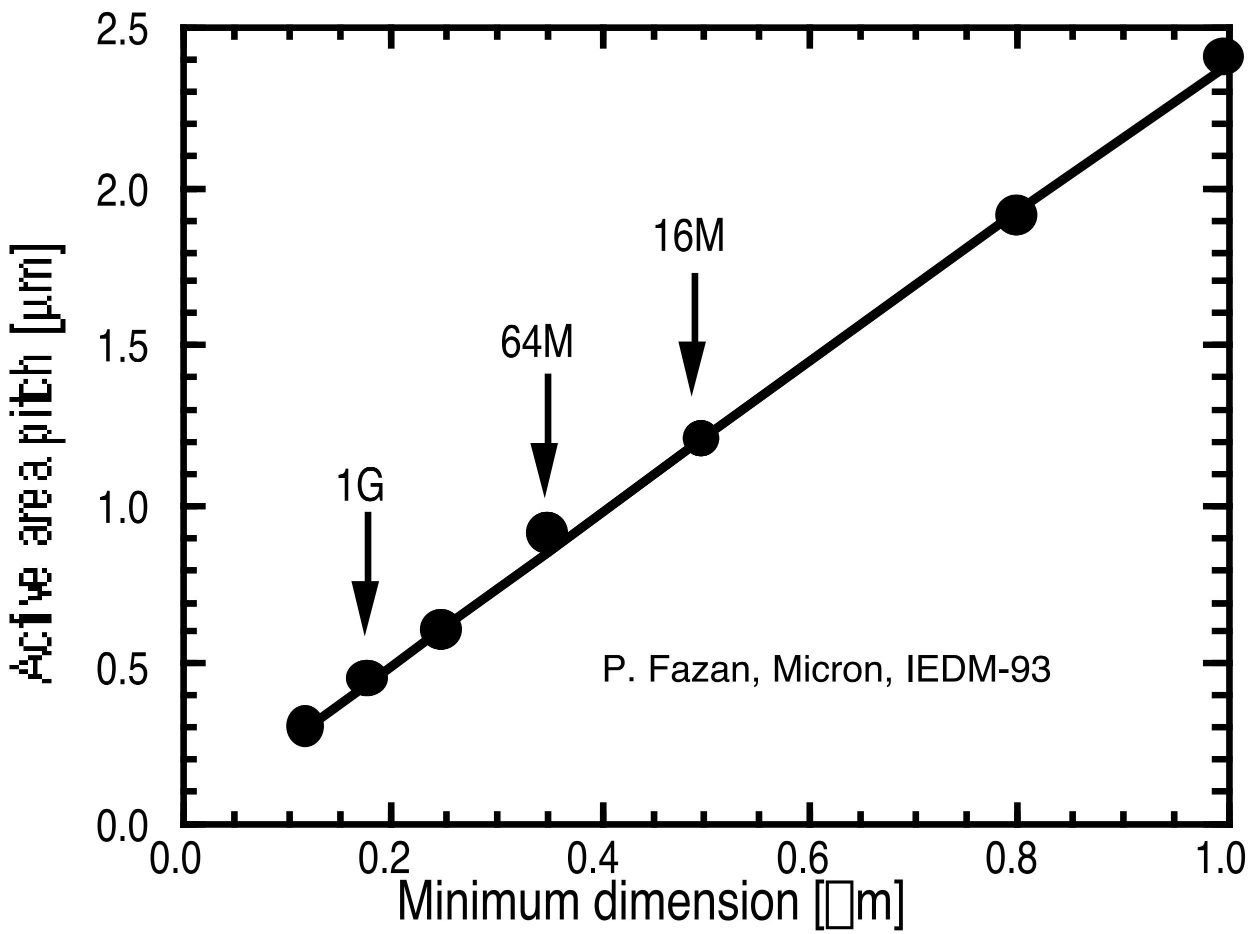


Elevated source/ drain



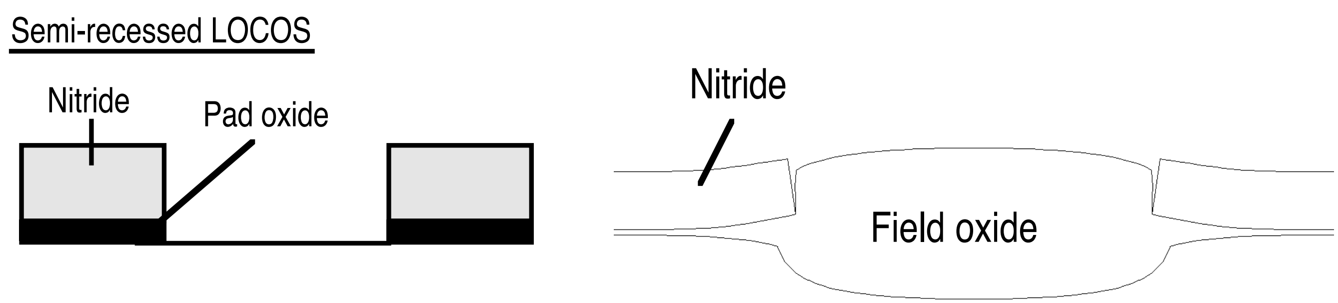
Silicidation

Device Isolation pitch as a function of minimum dimension

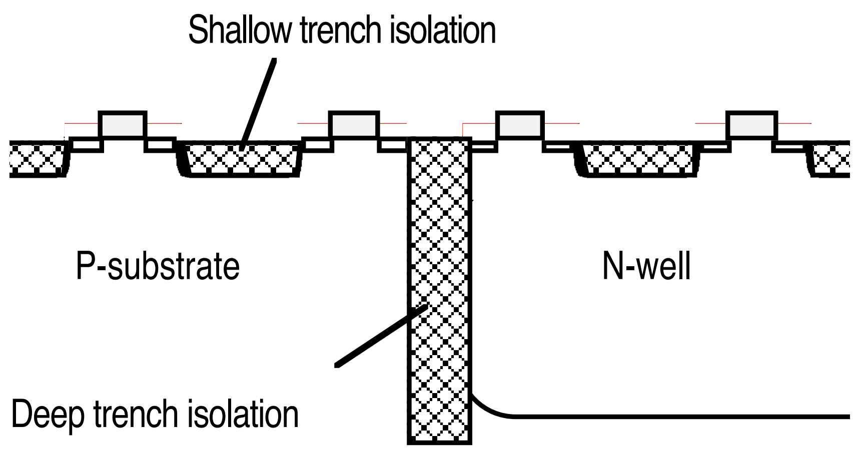


With decreasing feature size the requirement on allowed isolation area becomes stringent.

Scaling of Device Isolation



LOCOS based isolation technologies have serious problems in loss of area due to bird's beak.

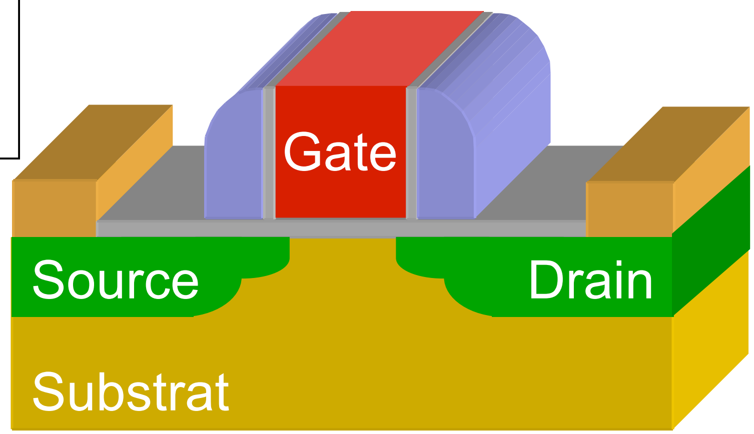


Trench isolation can minimize area loss

Physical Limits in Scaling Si MOSFET

Gate stack
- Tunneling current
- Gate depletion, resistance

Source/Drain
- Contact resistance
- Band-to-band tunneling
- Doping level, abruptness

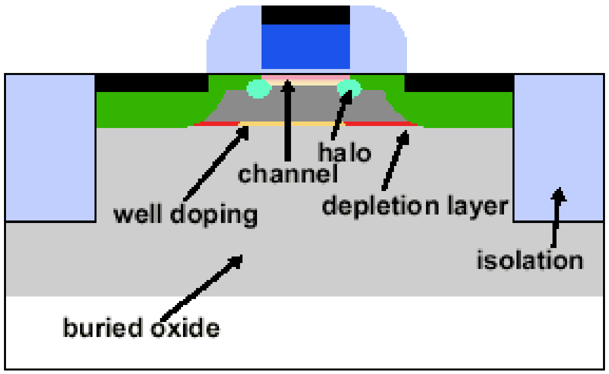


High E-Field
- Mobility degradation
- Reliability

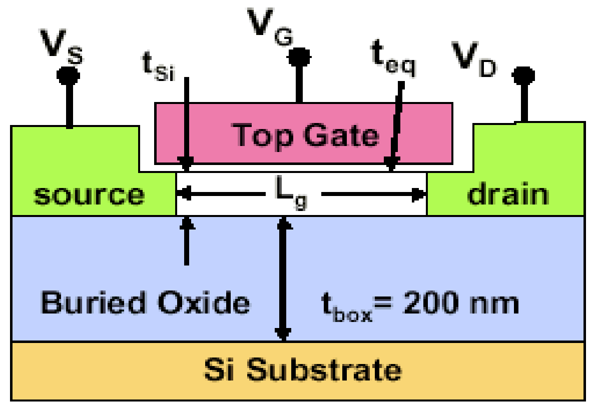
Channel
- Surface scattering - the “universal mobility” tyranny
- Subthreshold slope limited to 60mV/decade (kT/q)
- V_G - V_T decrease
- DIBL □ leakage

<u>Net result:</u> *Bulk-Si CMOS device performance increase <u>commensurate</u> with size scaling is unlikely beyond the 70 nm generation*

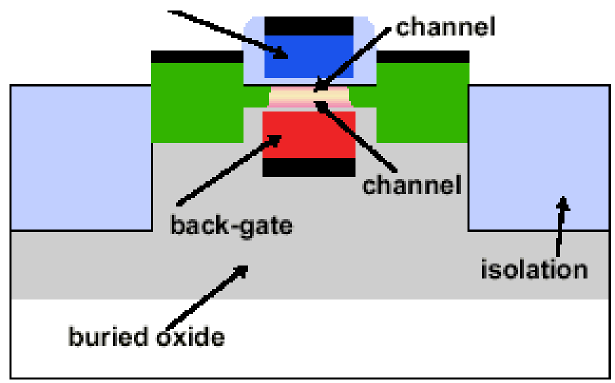
Evolution of Device Structures



Partially depleted SOI
(PD SOI)



Fully depleted SOI with
Back-Gate

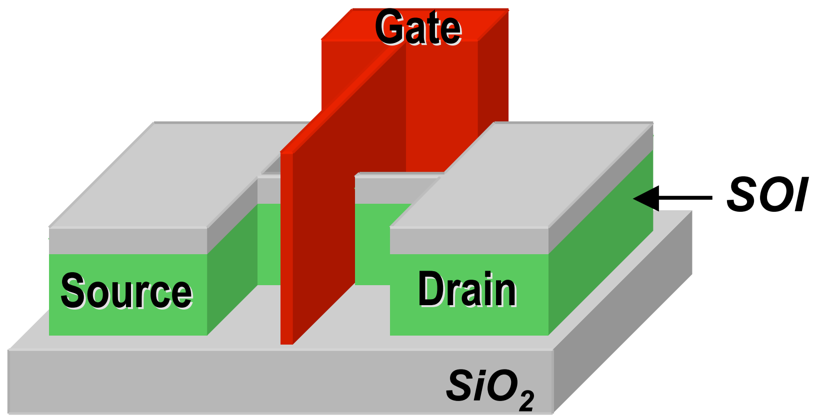


Double-Gate/Back-Gate
CMOS

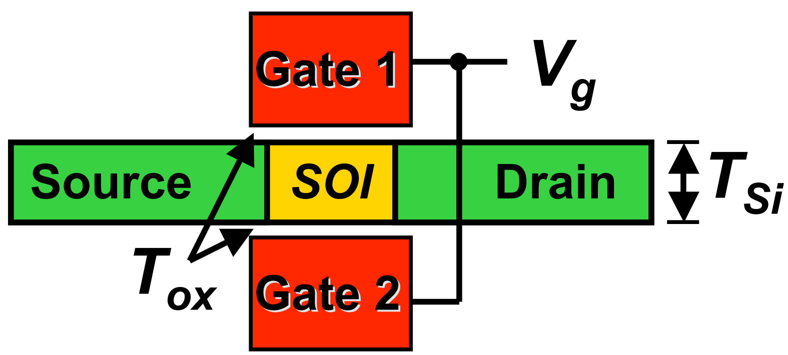
- Short channel effect control by geometry
- Steeper subthreshold slope
- Lower channel doping
  - higher mobility
  - reduced dopant fluctuation

Novel MOS Double Gate Structures

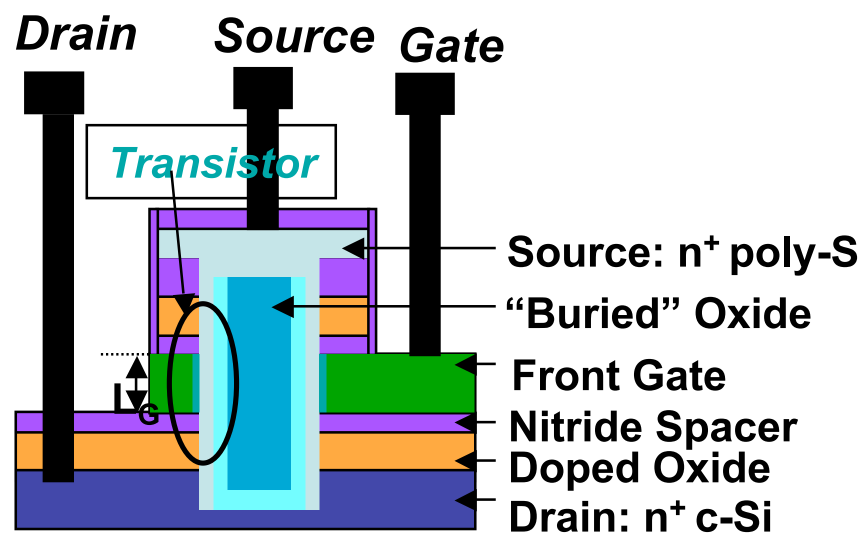
FinFET



Double Gate SOI



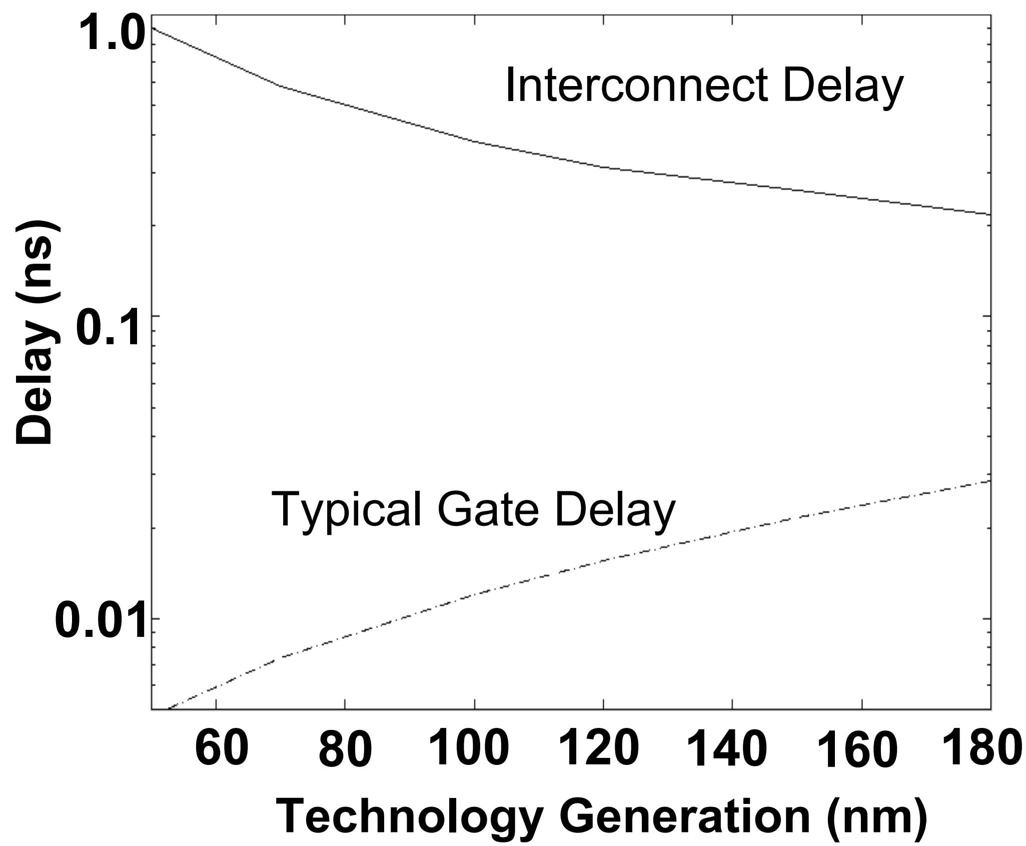
Vertical MOS



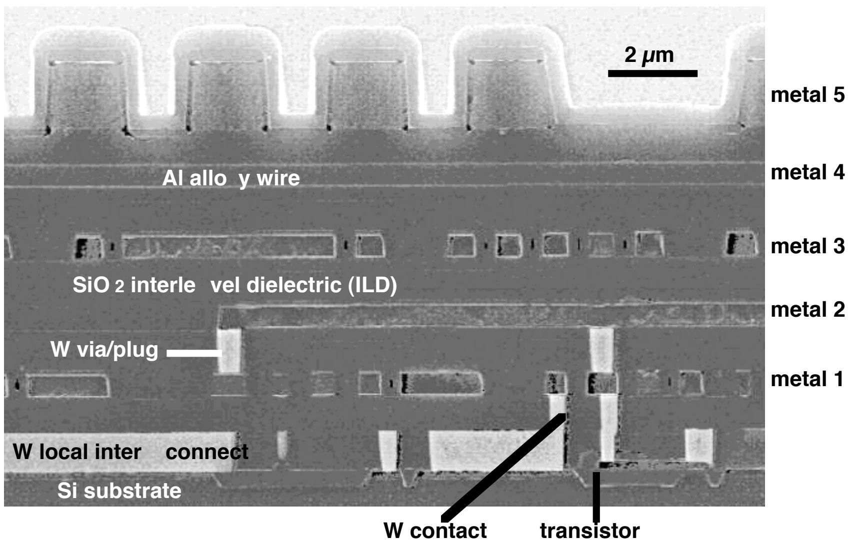
Full advantage of DG require very thin Si films (< 20 nm)

Interconnect Delay Is Increasing

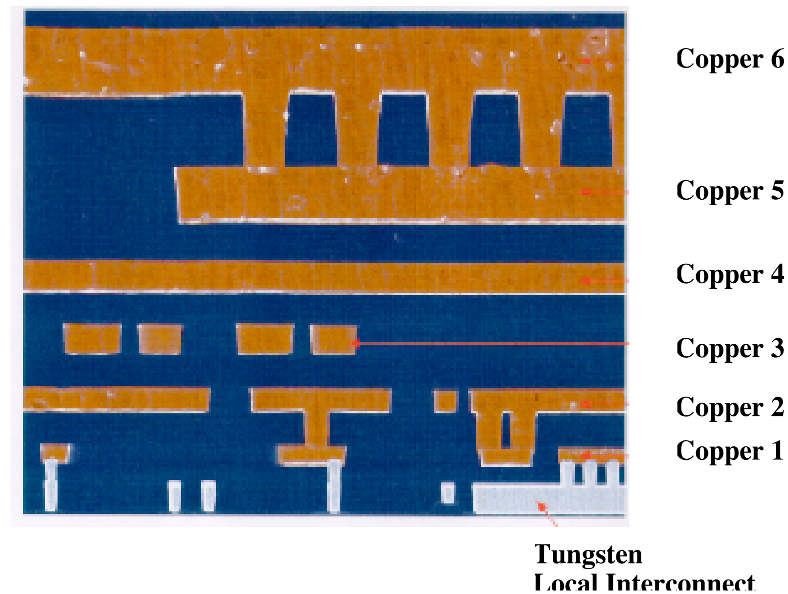
- **Chip size is continually increasing due to increasing complexity**
- **Device performance is improving but interconnect delay is increasing**
- **Chip sizes today are *wire-pitch limited*: Size is determined by amount of wiring required**



Current Interconnect Technologies

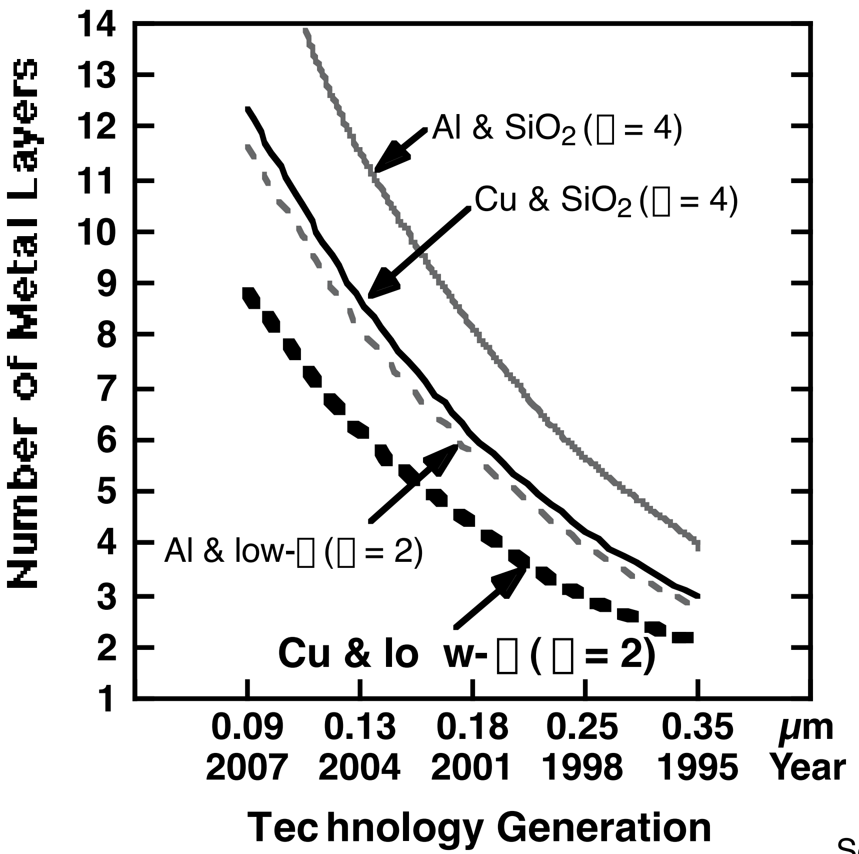


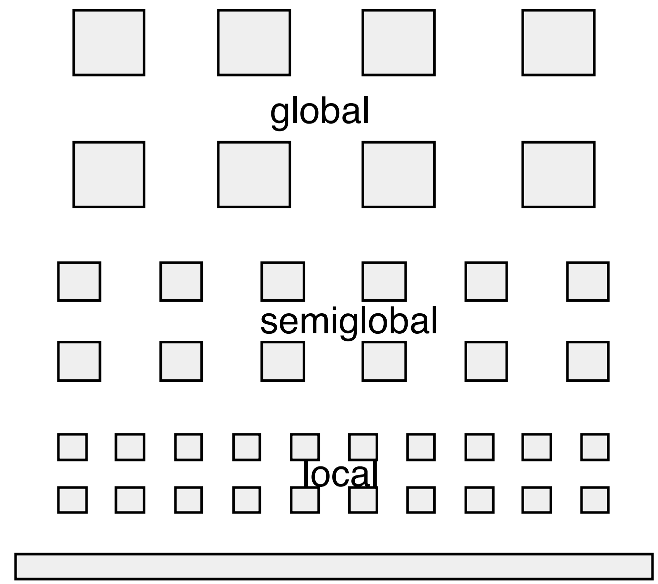
Current Al technology
(Courtesy of Motorola)



Current Cu technology
(Courtesy of IBM)

Why Cu and Low-k Dielectrics?



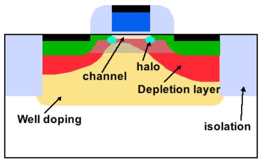


Source: Y.Nishi T.I.

Reduced resistivity and dielectric constant results in reduction in number of metal layers as more wires can by placed in lower levels of metal layers.

Summary: Technology Progression

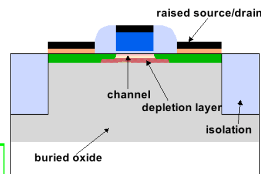
Bulk CMOS



Cu interconnect

Low-*k* ILD

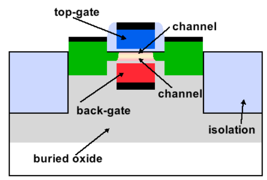
FD SOI CMOS



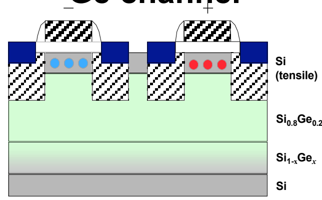
Metal gate

High *k* gate dielectric

Double-Gate CMOS

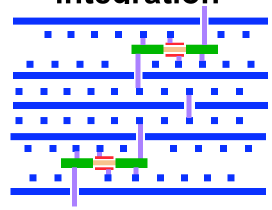


Strained Si
Ge channel

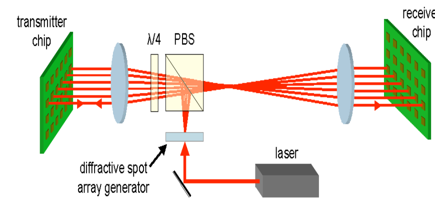


Wafer bonding
Crystallization

3D, heterogeneous integration



Optical interconnect

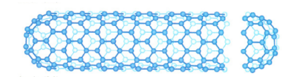


Detectors, lasers, QWM, waveguides

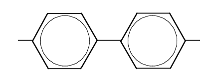
Self-assembly

Interconnects and contacts for nanodevices

Nanotechnology



Nanotube



Molecular devices

100 nm → 2 nm

Feature Size