INTRODUCTION [FROM THE 2001 ITRS]

OVERVIEW

For four decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are shown in Table A with examples of each. Most of these trends have resulted principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. Of course, the most frequently cited trend is in integration level, which is usually expressed as Moore's Law (the number of components per chip doubles every 18 months). The most significant trend for society is the decreasing cost-per-function, which has led to significant improvements of productivity and quality of life through proliferation of computers, electronic communication, and consumer electronics.

Table A Improvement Trends for ICs Enabled by Feature Scaling

TREND	*EXAMPLE*
Integration Level	**Components/chip, Moore's Law**
Cost	**Cost per function**
Speed	**Microprocessor clock rate, GHz**
Power	**Laptop or cell phone battery life**
Compactness	**Small and light-weight products**
Functionality	**Nonvolatile memory, imager**

All of these improvement trends, sometimes called "scaling" trends, have been enabled by large R&D investments. In the last two decades, the growing size of the required investments has motivated industry collaboration and spawned many R&D partnerships, consortia, and other cooperative ventures. *The International Technology Roadmap for Semiconductors (ITRS)* has been an especially successful worldwide cooperation. It presents an industry-wide consensus on the "best current estimate" of the industry's research and development needs out to a 15-year horizon. As such, it provides a guide to the efforts of companies, research organizations, and governments. The *ITRS* has improved the quality of R&D investment decisions made at all levels and has helped channel research efforts to areas that truly need research breakthroughs.

The 2001 edition of the *ITRS* is the result of the continued worldwide consensus building process. The participation of semiconductor experts from Europe, Japan, Korea, Taiwan, and U.S.A. ensures that the *2001 ITRS* continues to be the definitive source of guidance for semiconductor research as we strive to extend the historical advancement of semiconductor technology and the integrated circuit market. This is the second edition of *ITRS* that has had worldwide participation throughout its two-year cycle of creation. The diverse expertise and dedicated efforts that this international effort mobilized have brought the Roadmap to a new level of worldwide consensus about future semiconductor technology requirements.

The complete 2001 ITRS and past editions of the 2000 Update and the 1999 ITRS editions are available for viewing and printing as an electronic document at the internet web site http://public.itrs.net.

MEANING OF *ITRS* TECHNOLOGY REQUIREMENTS

Since its inception in 1992, a basic premise of the Roadmap has been that continued scaling of microelectronics would further reduce the cost per function (averaging ~25% per year) and promote market growth for integrated circuits (averaging ~17% per year). Thus, the Roadmap has been put together in the spirit of a challenge—essentially, "*What technical capabilities need to be developed for the industry to continue to stay on Moore's Law and the other trends?*" More and more of the semiconductor industry's research effort, including consortia and collaboration with suppliers, has been shared in a precompetitive environment. The *ITRS* identifies the principal technology needs to guide the shared research. It does this in the two following ways: (1) showing the "targets" that need to be met by "technology solutions" currently under development, and (2) indicating where there are no "known manufacturable solutions" (of reasonable

confidence) to continued scaling in some aspect of the semiconductor technology. This latter situation is highlighted as red cells in the Roadmap technology requirements tables, and is also referred to as the "Red Brick Wall." The red is officially on the Roadmap to clearly warn where historical trends of progress might end if some real breakthroughs are not achieved in the future. For some Roadmap readers, the red designation may not have adequately served its purpose of highlighting serious and exciting challenges. There can be a tendency to view any number on the Roadmap as "on the road to sure implementation" regardless of its color. To do so would be a serious mistake.

An analysis of "red" usage might classify the red parameters into the following two categories:

1. where the consensus is that the particular value will ultimately be achieved (perhaps late), but for which the industry does not have much confidence in any currently proposed solution(s), or
2. where the consensus is that the value will never be achieved (for example, some "work-around" will render it irrelevant or progress will indeed end).

To achieve the red parameters of the first category, breakthroughs in research are needed. It is hoped that such breakthroughs would result in the "red" turning to "yellow" (defined as "manufacturable solutions are known") and, ultimately, "white" (defined as manufacturable solutions are known and are being optimized") in future editions of *ITRS*. A conservative interpretation might view the red parameters of the second category as effectively "beyond" or "off" the Roadmap.

The *ITRS* time horizon (15 years) provides a limit to what may be considered "on/off the Roadmap." To date, each edition of the *ITRS* has been built around a view toward continued scaling of CMOS (Complementary Metal-Oxide-Silicon) technology. However, with the 2001 edition, we are reaching the point where the horizon of the Roadmap challenges the most optimistic projections for continued scaling of CMOS (for example, MOSFET channel lengths of roughly 9 nm). It is also difficult for most people in the semiconductor industry to imagine how we could continue to afford the historic trends of increase in process equipment and factory costs for another 15 years! Thus, the *2001 ITRS* begins to address post-CMOS devices.

Another constraint by which some items may be on/off the Roadmap is the breadth of technology addressed. The scope of the *2001 ITRS* specifically addresses detailed technology requirements for all CMOS integrated circuits, including mixed-signal products. This group constitutes over 75% of the world's semiconductor consumption. Of course, many of the same technologies used to manufacture CMOS ICs are also used for other products such as compound-semiconductor, discrete, optical, and micro-electromechanical systems (MEMS) devices. Thus, to a large extent, the Roadmap covers many common technology requirements for most IC-technology-based micro/nanotechnologies even though that is not the explicit purpose of the Roadmap.

POSITION ON POTENTIAL SOLUTIONS

The *ITRS* strives to avoid prematurely identifying definite solutions to the future technology challenges. This is difficult, since guidance on the research needs is intended. Despite this need to provide guidance, the Roadmap participants are continually pursuing new ways to prevent the Roadmap from being interpreted as limiting the range of creative approaches to further advance microelectronics technology. One of the resulting compromises has been to only present illustrative examples of potential solutions to selected challenges in the *ITRS*. These are not to be construed even as complete lists of all solutions suggested to date, much less exhaustive lists of what should be explored. A few of the potential technical solutions are listed, where known, only to inform the readers of current thinking and efforts. Furthermore, the listing of a particular potential solution does not constitute an endorsement by the Roadmap process.

It *is* the intent of this document to identify the technological barriers and when the industry will likely run into them. It is *not* the intent of this document to identify the most likely solutions to be adopted, nor to focus attention on those potential solutions currently known at the expense of other new concepts. In fact, it is eagerly hoped that this Roadmap will inspire additional innovative solutions. *The semiconductor industry's future success continues to depend on new ideas.*

OVERALL ROADMAP PROCESS AND STRUCTURE

Each technology-area chapter of the *ITRS* is written by a corresponding International Technology Working Group (ITWG). The ITWGs are of two types: *Focus* ITWGs and *Crosscut* ITWGs. The Focus ITWGs correspond to typical sub-activities that sequentially span the Design/Process/Test/Package product flow for integrated circuits. The Crosscut

ITWGs represent important supporting activities that tend to individually overlap with the "product flow" at multiple critical points.

For the *2001 ITRS*, the Focus ITWGs are the following:

- Design
- Test
- Process Integration, Devices, and Structures
- Front End Processes
- Lithography
- Interconnect
- Factory Integration
- Assembly and Packaging

Crosscut ITWGs are the following:

- Environment, Safety, and Health
- Yield Enhancement
- Metrology
- Modeling and Simulation

Each ITWG receive inputs from the regional Technology Working Groups (TWGs) of the five geographical regions (Europe, Japan, Korea, Taiwan, and the U.S.A.) One-to-two representatives from each regional TWG represent the regional TWG on the corresponding ITWG. The regional TWGs are composed of experts from industry (chip-makers as well as their equipment and materials suppliers), government research organizations, and universities. In 2001, a total of 839 experts volunteered their services in the twelve TWGs in five regions. The composition of the total TWG membership is analyzed in Figure 1. For this edition, three 2-day *ITRS* meetings in Grenoble, France (April, 2001), San Francisco, U.S.A. (July, 2001), and Santa Clara, U.S.A. (November, 2001) provided the main forums for face-to-face discussions among the members of each ITWG and coordination among the different ITWGs. In addition, each of the TWG incorporates feedback gathered from an even larger community through "sub-TWG meetings" and public "Roadmap Workshops." The Roadmap resulting from this broad input is, hopefully, a "best-attempt" at building the widest possible consensus on the future technology needs of the semiconductor industry.

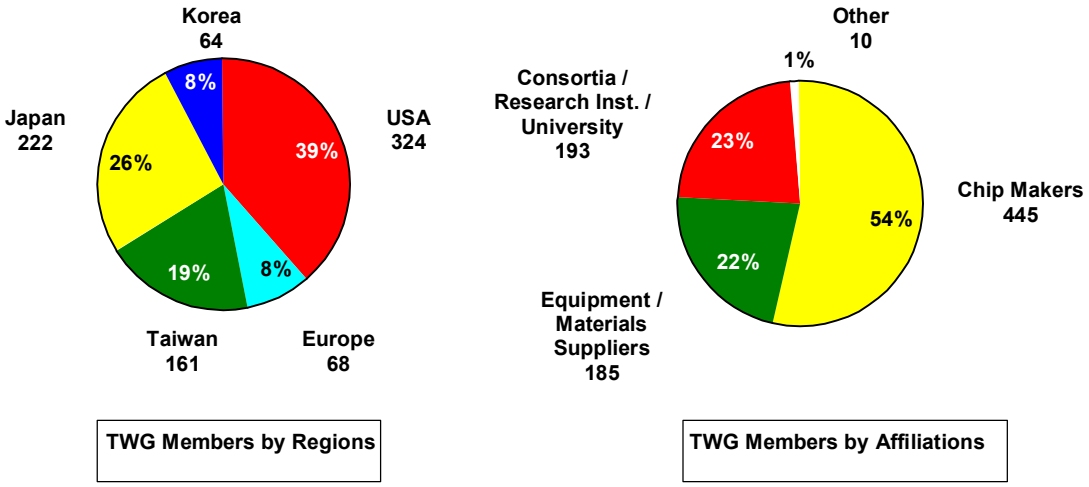


Figure 1 Composition of the Technology Working Group (TWG).

Overall coordination of the *ITRS* process is the responsibility of the International Roadmap Committee (IRC), which has two-to-four members from each region (representing a regional coordinating committee such as the SIA Roadmap Coordinating Group for the U.S.A.). The principal IRC functions include

- Providing guidance/coordination for the ITWGs,
- Hosting the *ITRS* Workshops, and
- Editing the *ITRS*.

TECHNOLOGY CHARACTERISTICS / REQUIREMENTS TABLES

A central part of the IRC guidance/coordination is provided through the initial creation (as well as continued updating) of a set of Overall Roadmap Technology Characteristics (ORTC) tables. These tables summarize key high-level technology requirements, which define the future "technology nodes" and generally establish some common reference points to maintain consistency among the chapters written by individual ITWGs. The high-level targets expressed in the ORTC Tables are based, in part, on the compelling economic strategy of maintaining the historical high rate of advancement in integrated circuit technologies. Thus, the ORTC provide a "top-down business incentive" to balance the tendency for the ITWGs to become conservative in expressing their individual, detailed future requirements.

Each ITWG chapter contains several principal tables. They are individual ITWGs' technology requirements tables patterned after the ORTC tables. For the *2001 ITRS*, the ORTC and technology requirements tables are separated into "Near-term Years" (2001, 2002… through 2007) and "Long-term Years" (2010, 2013, and 2016). This format is illustrated in Tables B, which contains a few key rows from lithography-related ORTC tables.

Table B ITRS Table Structure—Key Lithography-Related Characteristics by Product Type

Near-term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25

Long-term Years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9

The ORTC and technology requirements tables are intended to indicate current best estimates of introduction timing for specific technology requirements. "Production" is defined as when any two companies have reached the production volume of 10k parts per month. Please refer to the Glossary for detailed definitions for Year of Introduction and Year of Production.

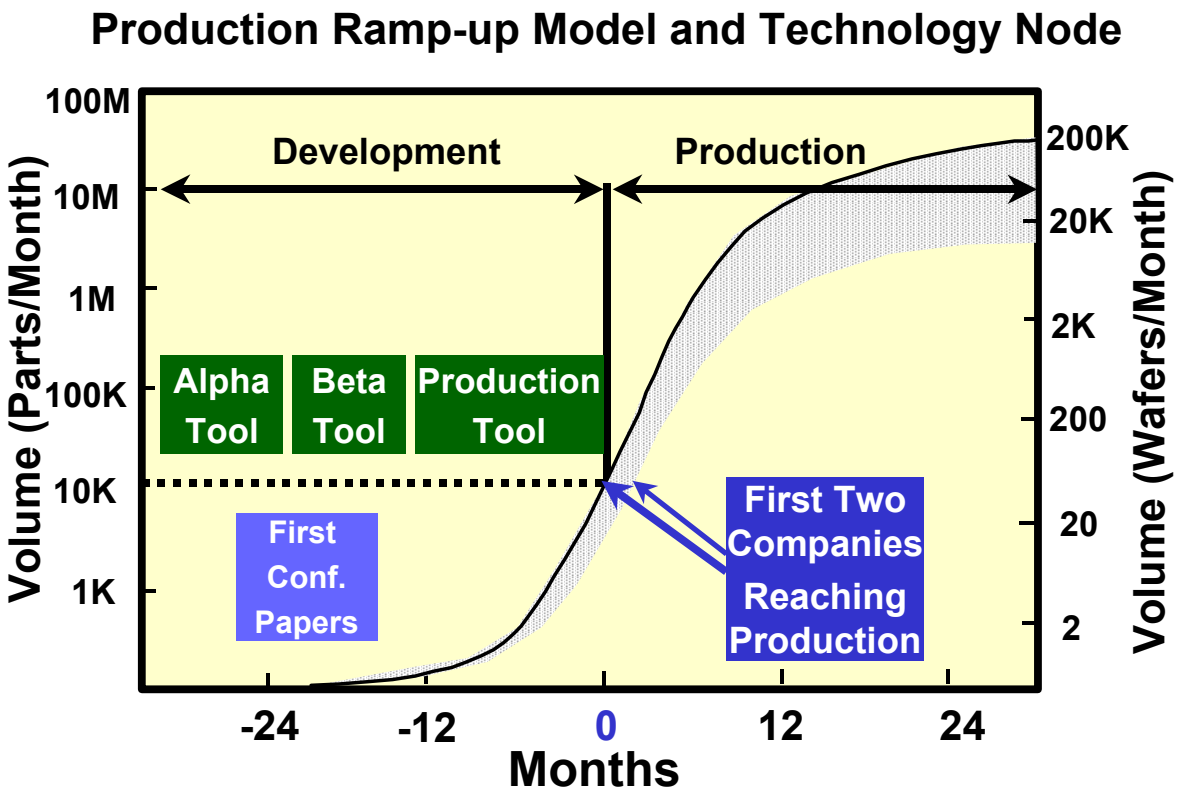


Figure 2 A Typical Production "Ramp" Curve

The ORTC and technology requirements tables are intended to indicate current best estimates of introduction time points for specific technology requirements. Ideally, the Roadmap might show multiple time points along the "research-development-prototyping-manufacturing" cycle for each requirement. However, in the interests of simplicity, usually only one point in time is estimated. The default "time of Introduction" in the *ITRS* is the "Year of Production," which is defined in Figure 2.

The "Production" time in ITRS refers to the time when the first company brings a technology to production and a second company follows within three months. It is noted that the ITRS Roadmap, by its definition, focuses on forecasting the earliest introduction of the leading-edge technologies in respective fields for producing semiconductors.

Therefore it is obvious that many companies, for a variety of reasons, may choose to introduce a technology node later than the earliest introductions, hence that there is a wide variation of the technologies in actual production status from leading-edge to trailing-edge. Figure 3 shows, in horizontal bar-graph, the actual, annual worldwide wafer production capacity distributions over different process feature sizes. The distributions are quite wide-spread while the ITRS Technology Nodes, shown in small blue marks, are located exactly on the leading-edges of each of them.

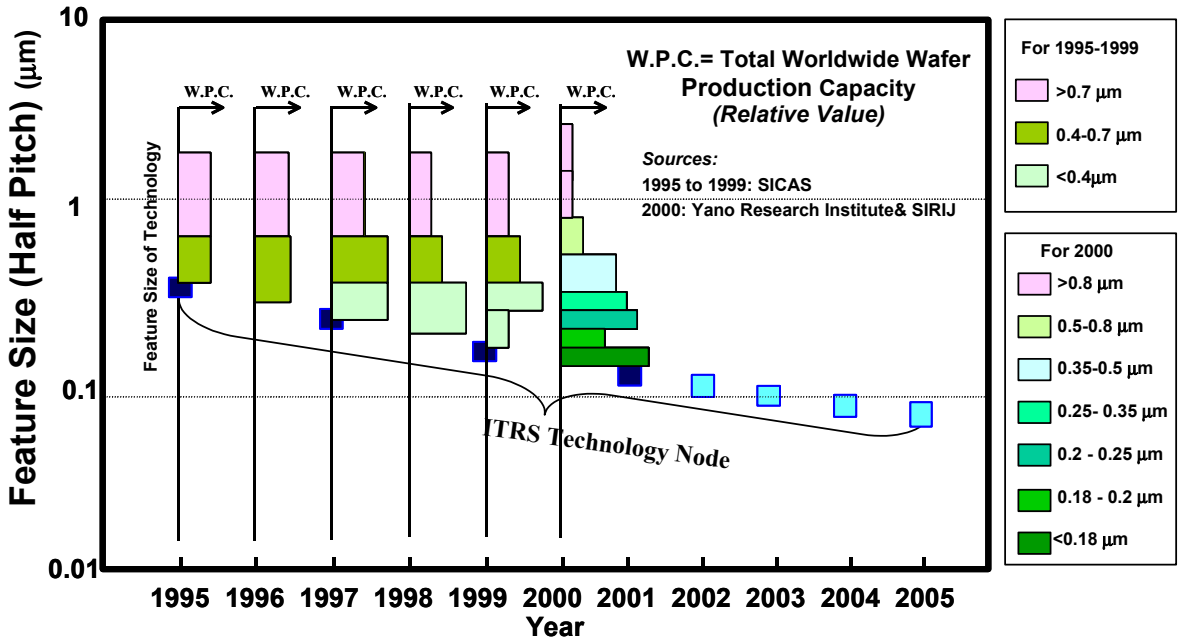
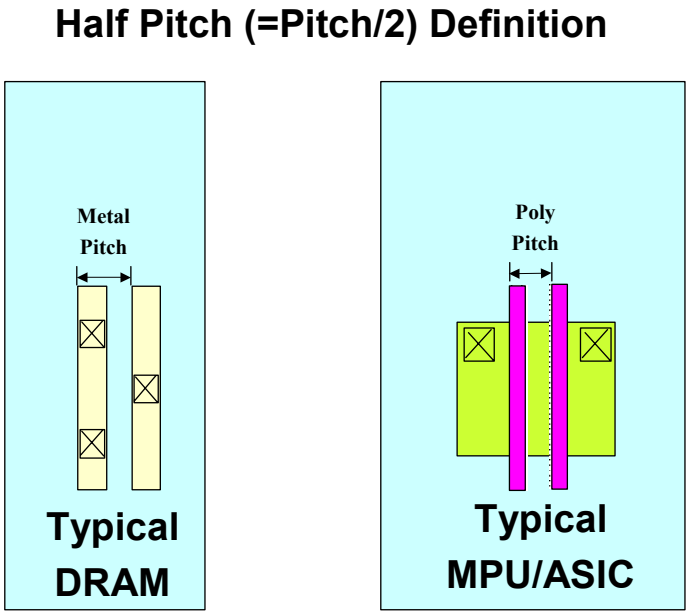


Figure 3 Technology Node Compared to Actual Production Capacity Technology Distribution

Note that some rows in the ORTC and technology requirements tables refer to other timing points, which are defined for each case (e.g., "at sample"). Of course, for the "Long-term Years," for which the table intervals are three years, it is possible for the "best-estimate year of production" to fall in between the selected three-year intervals for some technology requirements. Also note that the "production" ramp in Figure 2 can be viewed as the time to ramp to full production wafer starts. For a fab designed for 20K wafer-starts-per-month (wspm) capacity, the time to ramp from 20 wspm to full capacity can take 9–12 months. This time would correspond to the same time for ramping device unit volume capacity from 6K units to 6M units per month if the chip size were 140 mm^2 (430 gross die per 300 mm wafer × 20K wspm × 70% total yield from wafer starts to finished product = 6M units/month).

TECHNOLOGY NODES

The concept of "technology nodes" used to be quite straightforward to understand as it has historically been linked to the introduction of new Dynamic Random Access Memory (DRAM) generations with a 4× increase in bits/chip between generations. For as long as this cycle strictly followed Moore's Law (three-year cycle for 4×), the technology nodes and DRAM generations were essentially synonymous. However, in recent years, a greater diversity of products serving as technology drivers, faster introduction/optimization of product-specific technology, and the general increase in business and technology complexity are all tending to de-couple the many technology parameters that have traditionally characterized "advance to the next technology node." For example, microprocessor unit (MPU) products have recently driven the reduction of gate length at a faster pace than lithography half-pitch. While DRAM continues to drive the lithography half-pitch, MPU drives the gate length. Even the choice of basic lithography technology has tended to become more product specific (such as "pushing the wavelength as fast as possible" versus "using phase-shift masks"). Following the practice of the *1999 ITRS*, the *2001 ITRS* ORTC tables list the DRAM half-pitch, the MPU half-pitch, and MPU gate length, as shown in Table B. These technology parameters are defined in Figure 4. Any of the four parameters (rows) in Table B may be chosen as the driver for a given technology requirements table of a given ITWG. Nevertheless, for a point of reference, the DRAM half-pitch is still used in the *2001 ITRS* as the designation of the technology node (DRAM still requires the smallest half pitch among all products.). For example, according to Table B, 2003 will be the year of production of the 100 nm node. Again, the "node designation" is defined by DRAM half pitch, not by the transistor gate length or minimum feature size characteristic of that node. Additional (and, in some cases, more precise) definitions related to the *ITRS* tables may be found in the *Glossary*.



** DRAM pitch determines the technology "node" designation*

Figure 4 Definition of the Half Pitch and Gate Length

In recent years the "technology-development cycle" has been closer to two years than three years. On the other hand, the scaling ratio of the minimum feature size of one technology generation to the previous generation may no longer adhere to the historical value of 0.7. For example, 100 nm is not 0.7× of 130 nm. In addition, some companies may choose to introduce a "half node" (for example 150 nm may be considered a half node between the 180 nm node and the 130 nm node) with the intention of introducing the next "full" node at a later time. The *2001 ITRS* acknowledges the validity of these practices and follows the *1999 ITRS* in listing the near-term (2001–2007) technology requirements on yearly intervals and the long-term (2008–2016) requirements on three-year intervals as shown in Table B. Thus, we can say that 2003 is the year of production of the 100 nm node and 2004 is the year of production of the 90 nm node. One may also interpret the long-term three-year interval table as a "challenge" to extend the trend of one major new technology node every three years with scaling ratio of 0.7 between nodes through the "22 nm node" (which include 9 nm transistor gate lengths) in 2016.

DRIVERS FOR ITWG TECHNOLOGY REQUIREMENTS

The particular lithography-related rows selected for Table B from the ORTC tables are special in that any one of them may be designated by an ITWG as a "driver" for any specific row in one of their technology requirements tables. For example, the physical gate length may be the appropriate driver for the gate CD control and the source/drain junction depth. The designation of drivers for technology requirements provides some traceable and supportable assumptions for constructing the ITWG tables. It also provides useful links between the ORTC tables and the ITWG tables. Thus, as the Roadmap is updated in subsequent editions, these links will be used for creating a first-pass version of the new tables. For example, if the requirements in one of these driver rows of the ORTC tables were subsequently pulled-in by one year, it would be assumed that rows in the ITWG technology requirements tables would shift by default along with their designated ORTC driver row.