Long Retention Time of Embedded DRAM Macro with Thin Gate Oxide Film Transistors

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Abstract

This paper describes the advantages of the thin gate oxide transistors with negative word-line (WL) architecture implemented in the embedded DRAM macro. The macros with the negative WL architecture are fabricated as well as the macros with the conventional WL architecture. We found the retention time of the negative WL architecture is longer by more than 5 times than that of the conventional WL architecture.

I. INTRODUCTION

Embedded DRAM macros in application-specific integrated circuit (ASIC) are increasingly used in mobile applications, such as MPEG-4 videophones [1] and personal digital assistants. In these applications, it becomes important to reduce the current that the DRAM macro consumes at the stand-by state. And the refresh cycle extension by improving the retention time of DRAM memory cell is effective. The negative word-line (WL) architecture in which the low level of the word-lines is bellow the ground level (VSS), has been reported [2][3][4]. One of the advantages of the negative WL architecture is reduction in the electric field of the memory cell transistors. Then thinner gate oxide transistors can be used. The subthreshold swing (S-factor) of memory cell transistors is improved by using the thinner gate oxide. Furthermore the negative WL architecture permits use of the lower threshold voltage for the memory cell transistors. As a result, the impurity concentration of the transistor channel decreases and so junction leakage current is reduced. Due to these two advantages, negative WL architecture has promising characteristics for improving the retention time of the DRAM macro.

In order to clarify the effect of the negative WL architecture, we implemented two kinds of DRAM macros. One of them is the negative WL architecture and the other is the conventional WL architecture. We fabricated them by the same process except for the channel impurity concentration and the thickness of the gate oxide. Using these comparison methods, it becomes clear that the thinner gate oxide extends refresh cycle. Therefore the negative WL architecture reduced the stand-by current and is useful for the mobile applications.

II. Measured samples

In order to compare accurately the retention characteristics between the negative WL architecture and the conventional WL architecture, we prepared two kinds of DRAM macros in 0.25um CMOS technology [5][6]. Except for the channel impurity concentration and the thickness of the gate oxide, those macros are fabricated by the same process. Table 1 shows the characteristics of the transistors used in each macro. The gate oxide thickness of the transistors (Tox) and the threshold voltage (Vth) are shown. The macro with the conventional WL architecture is composed of transistors with 5.5nm and 8nm thickness of the gate oxide, while the macro with the negative WL architecture is composed of transistors with 5.5nm thickness of the gate oxide. In spite of this gate oxide thickness change, the Vth of the transistors are maintained except for the memory cell transistors. The Vth of the cell transistors will be described in section III.

Fig.1 shows the row decoder circuits of the two macros. The WL driving architecture is altered by changing only one metal layer mask. VHH is supply voltage for the row decoder circuits and VLL is the low level of the WL. In the macro with the conventional WL VHH is connected to VEXT, that is, to the external voltage source (2.5V), and VLL is connected to VSS (0V). And in the macro with the negative WL architecture, VHH is connected to VAA, that is, to the high level of the bit-line (1.8V), and VLL is connected to VBB, that is, to the back bias voltage of memory cell transistors (-0.5V). So the difference between the layout patterns of these two macros is only the connection of VHH and VLL. The dimensions of the transistors and the layout pattern of the transistors are identical for the two macros.

Table 1 The transistors of measured samples

	Conventional WL		Negative WL	
	Tox	Vth	Tox	Vth
Nch	8nm	0.35V	5.5nm	0.35V
	5.5nm	0.55V	5.5nm	0.55V
Pch	8nm	0.8V	5.5nm	0.8V
	5.5nm	0.65V	5.5nm	0.65V
Cell	8nm	0.9V	5.5nm	0.4V

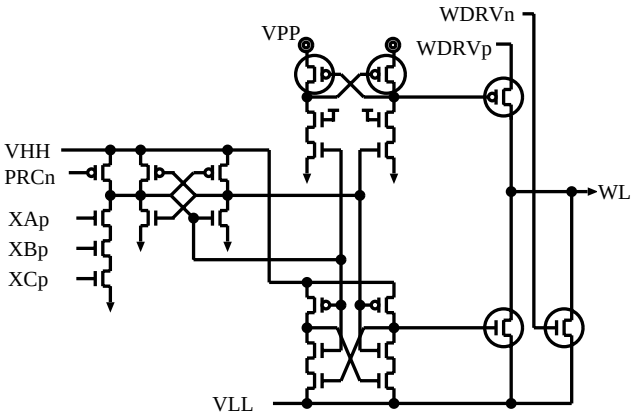

Fig.1 The row decoder circuits of the two macros

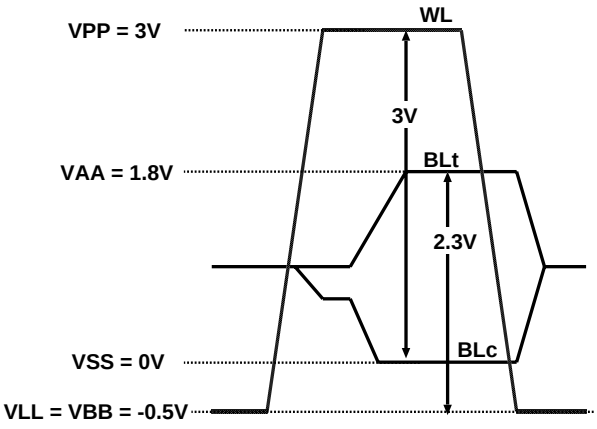

Fig.2 The waveform of the negative WL architecture

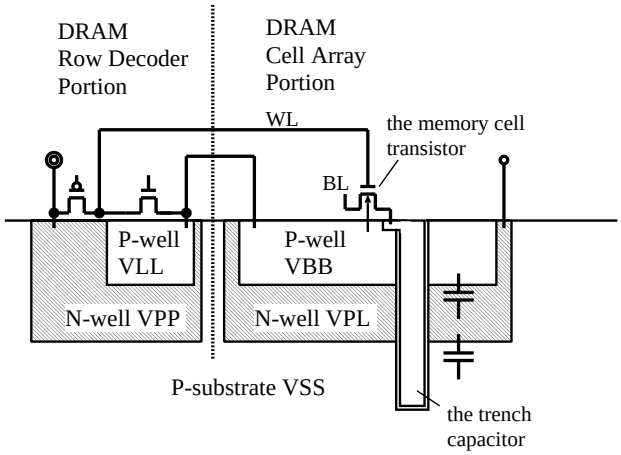

Fig.3 The cross section of the well structure for the negative WL architecture

Table 2 The voltage sources of the two macros

	Conventional WL	Negative WL
VPP	3.5V	3.0V
VEXT	2.5V	2.5V
VHH	VEXT	VAA
VAA	1.8V	1.8V
VPL	0.9V	0.9V
VSS	0V	0V
VLL	VSS	VBB
VBB	-0.5V	-0.5V

Fig.2 shows the waveform of the negative WL architecture. Bit-line (BL) swings from 0V to 1.8V, and WL swings from -0.5V called VLL to 3.0V called VPP. And in this case the voltage applied to the memory cell transistor is 3.0V. Table 2 shows the value of the voltage sources of these two macros.

VLL for the negative WL architecture should be stabilized. Fig. 3 shows the cross section of the well structure for the negative WL architecture. VLL connected to VBB, and VBB is connected to the P-well that is the bulk node of the memory cell transistors. The P-well of VBB is surrounded by the buried N-well of VPL that is the plate node of the trench cell capacitors. The buried N-well couples P-substrate biased VSS. Then VLL and VSS are coupled with large capacitance in the cell array portion.

III. Measurement Results

32Mb DRAM macro is used to compare the two macros. Fig.4 shows the comparison of the retention time of each macro. The measured results of 3 samples of each condition are shown. The x-axis is VBB voltage that is the same as VLL in the macro with the negative WL architecture. The y-axis shows the retention time of the average memory cell. The retention time of the negative WL architecture is longer by more than 5 times than that of the conventional WL architecture.

As Table 2 shows, VLL of the negative WL architecture is 0.5V lower than VLL of the conventional WL architecture. One the other side, Vth of the memory cell transistors with negative WL architecture is 0.5V lower than that of conventional WL architecture as shown in Table 1. So the improvement of the retention time can't be explained. We found this improvement is achieved because the S-factor of the memory cell transistors is reduced. Fig.5 shows the Vg-Id characteristic of the transistors with 8nm oxide film and 5.5nm oxide film at VBB=-0.5V. The S-factor of 5.5nm oxide film transistor is 71 (mV/decade) whereas that of the 8nm oxide film transistor is 84 (mV/decade). So the S-factor is reduced to 85%. The decrease of the thickness of transistor oxide film improves the S-factor. This is the reason that the macro with the negative WL architecture extends retention time.

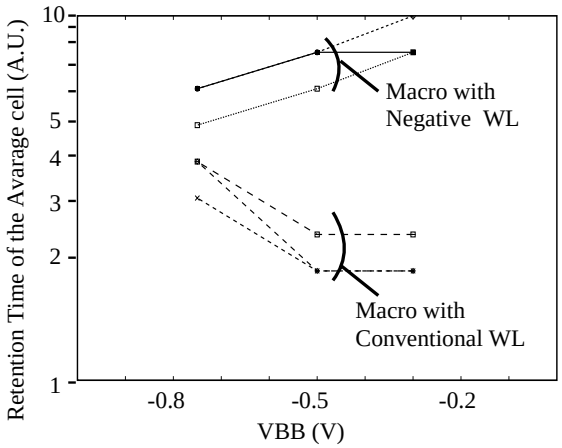

Fig.4 The retention time comparison between the negative WL architecture and the conventional WL architecture

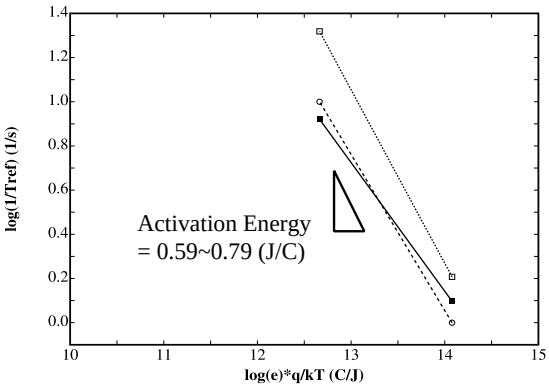

Fig.7 The temperature dependence of the retention time of the negative WL architecture

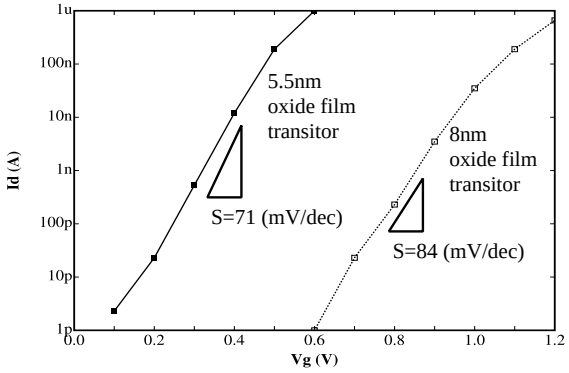

Fig.5 Vg-Id characteristic of the memory cell transistors

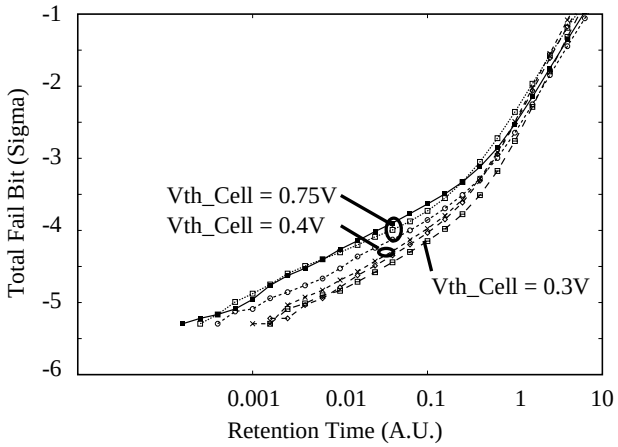

Fig.6 The retention characteristics of the negative WL architecture with the various Vth memory cell transistors

In Fig. 4 the shallower VBB is, the longer the retention time of the negative WL architecture becomes. In order to investigate this characteristic in detail, the macros with the different Vth memory cell transistors were measured. The Vth's of the memory cell transistor varies from 0.3V to 0.75V. And Fig. 6 shows the distribution of the retention time. The samples with lower Vth of the memory cell transistors have the longer retention time. This characteristic may be attributable to the two leakage mechanisms. One of them is the gate induced drain leakage current (GIDL) [7]. The GIDL effect is sensitive to the channel impurity concentration. Since the high Vth transistor needs the high channel impurity concentration, the GIDL effect is enhanced for the higher Vth transistors. The other leakage mechanism is the junction leakage current. The high channel impurity concentration also increases the junction leakage current. The activation energy can determine which mechanism is dominant. So we measured the temperature dependence of the retention time shown in Fig.7. The values of the activation energy of 3 samples are calculated. The Vth of the memory cell transistors of these samples is 0.4V. The values of activation energy are in the range of 0.59 and 0.79 (J/C). They are nearly equal to that of the typical value of the junction leakage current. So the junction leakage current accounts for the retention characteristics of the memory cells.

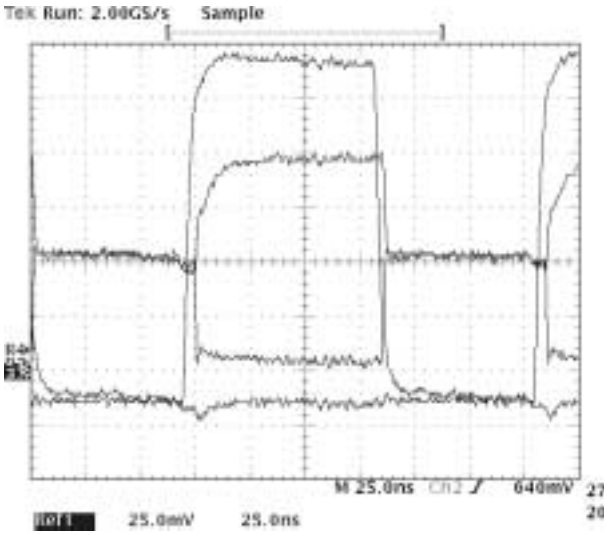

Fig.8 The measured waveform of the negative WL architecture

Fig.8 shows the measured waveform of the macro with the negative WL architecture. The voltage of WL, SAN (the source node of NFET sense amplifier), SAP (the source node of PFET sense amplifier) and VBB (=VLL) are shown. WL operates in 80ns cycles. And the noises of VBB and VSS and other internal voltage sources of the macro are very small. The noise of VBB is less than 0.2V, and the noise of VSS is less than 0.1V. The architecture in which VBB and VLL are shorted contributes this small noise level.

IV. CONCLUSIONS

The retention characteristic of the negative WL architecture has been studied by comparing with the conventional WL architecture. The two types of DRAM macros are fabricated by the same process except for the channel impurity concentration and thickness of gate oxide. We found the retention time of the negative WL architecture to be longer by more than 5 times than that of the conventional WL architecture. This extension of the retention time is caused by the improvement of the S-factor and the reduction of the junction leakage current of the thinner gate oxide low Vth memory cell transistors.

REFERENCES

[1] T.Nishikawa et al., "A 60MHz 240mW MPEG-4 Video-Phone with 16Mb Embedded DRAM," 2000 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, p.p.230-231.

[2] T.Yamagata et al., "Low Voltage Circuit Design Techniques for Battery-Operated And/Or Giga-scale DRAMs," IEEE J. Solid-State Circuits vol.30, no.11 1995, p.p. 1183-1188

[3] H.Yamaguchi et al., "A Circuit Technology for a Self-Refresh 16Mb DRAM with Less Than 0.5uA/MB Data-Retention Current," IEEE J. Solid-State Circuits vol.30, no.11 1995, p.p. 1174-1182

[4] H.Tanaka et al, "A Precise On-chip Voltage Generator for a Gigascale DRAM with a Negative Word-line Scheme," IEEE J. Solid-State Circuits vol.34, no.8 1999, p.p.1084-1090

[5] T.Namekawa et al., “Dynamically Shift-Switched Dataline Redundancy Suitable for DRAM Macro with Wide Data Bus,” 1999 SYMPOSIUM ON VLSI CIRCUIT, Digest of Technical papers, p.p.149-152.

[6] K.Kokubun et al., “New DRAM Macro Technology using Self-aligned Salicide Block (SSB) Process for 0.18um SOC (System On Chip),” 1999 SYMPOSIUM ON VLSI TECHNOLOGY, Digest of Technical Papers, pp155-156.

[7] H.Suzuki et al., “Trap Assisted Leakage Mechanism of ‘worst’ Junction in Giga-bit DRAM Using Negative Word-Line Voltage,” Extended Abstracts of the 1998 International Conference of Solid State Devices and Materials, p.p.32-33.